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Electronic Circuit Design and Application

2nd ed. 2022
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https://doi.org/10.1007/978-3-030-79375-3

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S.J.G. Gift dedicates the book to his parents, his wife Sandra, and two sons Allister and Christopher.
Preface to the First Edition

Electronics is one of the most exciting areas of technology today. The semiconductor or microelectronics revolution that started with the invention of the transistor in 1947 and followed later by the introduction of the integrated circuit comprising many transistors on a single chip continues unabated. This most remarkable technology has resulted in the introduction of the microprocessor, the personal computer, cell phone, and MP3 player as well as the GPS, smart phone, the Internet, and the self-driving car. New and amazing electronic systems and sub-systems are introduced annually and the consumer is exposed to a dazzling array of truly amazing gadgets and devices.

This wonderful inventiveness has been fueled by unprecedented levels of transistor integration density with the number of transistors on a single chip growing from a few thousand in the early 1970s to over 10 billion in 2020. Moore’s law, which holds that transistor IC density will double every 2 years, still has relevance some 50 years after it was first proposed. Thus, extremely powerful ICs are available that carry out a vast range of important functions.

The world in which we live is an analog one with signals generally being continuous over time. However, computers are digital devices that represent information in discrete forms. With the extensive use of computers and other digital systems, the need for analog systems that interface the analog world and the digital computer has become increasingly important. A smart phone, for example, has many analog sensors that interface with the advanced processor within. The internet of things that enables the wide collection and processing of large amounts of real-time data has spawned an array of sensors and ICs, many of which must be interconnected using analog circuits. There is an increasing demand for analog modules in these and other systems that carry out a multiplicity of functions. There is therefore a critical need for the development of skills in analog electronic circuit design and application.

Text Philosophy
This book treats with the design and application of a broad range of analog electronic circuits in a comprehensive and clear manner. The discussion of design and application in the text, we believe, brings out the inherently interesting nature of electronics. There are several books on the market that deal extensively with analog electronic circuits, but most tend to give theory, explanations, and analysis of circuit behavior and generally do not enable the reader to design complete real-world functioning circuits or systems. This text addresses this shortcoming while treating comprehensively with the subject. It first provides a foundation in the theory and operation of basic electronic devices including the diode, the bipolar junction transistor, the field effect transistor, and the operational amplifier. It then presents detailed instruction on the design of working real-world electronic circuits of varying levels of complexity including feedback amplifiers, power amplifiers, regulated power supplies, filters, oscillators, and waveform generators. Upon completion of the book, the reader will understand the operation of and be able to confidently design a broad range of functioning analog electronic circuits and systems.

With the proliferation of electronic systems today, the need for electronic design engineers is greater than before, and this book we believe fills an important niche in the world of analog electronics. It is intended primarily as an undergraduate text for University and College students enrolled in electrical, electronic, and computer engineering programs. It should also prove useful for graduate students and practicing engineers who need to design practical systems to meet research or real-world needs.

**Text Features**

This book enables the reader to analyze a variety of circuits, to develop a deep understanding of their operation, and to design and optimize a range of working circuits and systems. Many examples help the reader to quickly become familiar with key design parameters and design methodology for each class of circuits. Each chapter starts with fundamental ideas and develops them step by step into a broad range of applications of real-world circuits and systems. Each chapter ends with several circuit applications with a full discussion of design methods.
Also, at the end of each chapter, there are research projects that are intended to stimulate the interests of the reader and encourage varying levels of investigation and experiment.

The attractive features of the book include the following:

- It comprehensively presents the design of working real-world analog electronic circuits for key systems and sub-systems.
- The material is clearly written and easily understood.
- Many worked examples of functioning circuits are presented.
- Design applications begin from the very first chapter and continue throughout the text.
- Research projects to stimulate and encourage further investigation are included at the end of each chapter.
- Ideas for further exploration are also included with these applications and research projects.
- Some simulations are used to demonstrate the functionality of the designed circuits.
- Upon completion of the text, the reader will be able to confidently design important analog electronic circuits.

Text Overview
The book contains 14 chapters with content as follows:

1. *Semiconductor Diode*—Provides a sound introduction to semiconductor diodes and their use in several circuits. Applications and research projects are presented.

2. *Bipolar Junction Transistor*—Introduces the binary junction transistor, its theory of operation, and its various configurations. The use of the device in the design of single-stage amplifier circuits is fully discussed. Applications and research projects are presented.

3. *Field Effect Transistor*—Introduces the field effect transistor, its theory of operation, and its various configurations. The use of the device in the design of single-stage amplifier circuits is thoroughly discussed. Applications and research projects are presented.

*BJT and FET Models*—Explores electrical circuit models for
representing the BJT and FET in accurately analyzing the behavior of circuits containing these devices. Applications and research projects are presented.

5. **Multiple-Transistor and Special Circuits**—Presents a comprehensive discussion of multiple-transistor circuits including several special circuit configurations. Applications and research projects are presented.

6. **Frequency Response of Transistor Amplifiers**—Discusses the frequency behavior of single-stage and multiple-stage transistor circuits. Several important configurations are analyzed. Applications are presented.

7. **Feedback Amplifiers**—Introduces the concept of negative feedback, distortion, and frequency performance in amplifier systems and presents full discussion of its application in amplifier design. Applications and research projects are presented.

8. **Operational Amplifiers**—Presents the operational amplifier in its various configurations and discusses numerous applications of this versatile circuit element. Applications and research projects are presented.

9. **Power Amplifiers**—Thoroughly explores power amplifiers and the various classes and configurations with numerous design examples from low-power to high-power systems. Applications and research projects are presented.

10. **Power Supplies**—Provides a comprehensive discussion of unregulated and regulated power supplies, their operation and design using discrete and integrated components. Applications and research projects are presented.

11. **Active Filters**—Presents a full discussion on the theory and design of low-pass, high-pass, band-pass, band-stop, and all-pass filters using operational amplifiers. The Bessel, Butterworth, and Chebyshev filter responses are considered. Applications and
research projects are presented.

12. *Oscillators*—Presents a full discussion of positive feedback and the Barkhausen criterion in oscillator systems and explores the design of numerous oscillator types including Wien bridge, phase shift, LC, and crystal oscillators. Applications and research projects are presented.

13. *Waveform Generators and Nonlinear Circuits*—Presents the theory of operation and design of a full range of waveform generators and nonlinear circuits including comparators, triangular wave generators, astable multivibrators, and precision rectifiers. Applications and research projects are presented.

14. *Special Devices*—This final chapter introduces the theory of operation and the circuit implementation of several special devices including photosensitive devices, opto-isolators, silicon controlled rectifier, triac, Shockley diode, diac, unijunction transistor, and the programmable unijunction transistor. Several design examples are presented and applications and research projects are discussed.

**Closing Remarks**

We have prepared a text which we believe enables the reader to enjoy the wonderful world of electronics while learning and applying design rules that lead to practical working electronic systems. We have included many interesting ideas and research projects throughout the text that will hopefully excite the reader. We hope this book will satisfy most of the electronic circuit design and application needs of students and practicing engineers and invite feedback regarding its contents.

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Preface to the Second Edition

In this second edition of our textbook *Electronic Circuit Design and Application*, we have maintained the focus on the design of working real-world electronic circuits for a range of applications. We have added materials in all but two chapters (Chaps. 4 and 6) that consist mainly of new circuits for consideration by the reader. However, Chap. 11 on active filters has been expanded to include information on biquadratic filters. Many errors in the first edition have been corrected and the labeling in some diagrams improved. We again commend our textbook to students and researchers at colleges and universities in electrical, electronic and computer engineering as well as practicing engineers and electronics enthusiasts. Please send any comments, corrections or suggestions about our book to stephangift@hotmail.com.

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Acknowledgments
We would like to express our sincere thanks to our students who provided useful feedback over the years while using this material in classroom instruction and to our Universities for providing the support that enabled the preparation of this text. We wish to also thank Mr. Itanie Gordon for drawing most of the diagrams in the text and Dr. Fasil Muddeen who reviewed the manuscript.
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A diode is referred to as the simplest electronic device. It consists essentially of two different materials in contact so that electric charge flows easily in one direction but is impeded in the other. Despite its simplicity, it performs an important role in electronic systems varying from simple to complex tasks. In this chapter, we will discuss the nature and characteristics of the solid-state diode (i.e., one based on semiconductor material) as well as employ it in the design of modern electronic systems.

Firstly, the basic physical concepts of semiconductors are presented. Then the basic diode is analyzed and its behavior is discussed. It is then applied in several designs to illustrate its implementation. At the end of this chapter, the reader will be able to:

- Understand the makeup and properties of intrinsic semiconductor material, n-type and p-type semiconductor material, and the action of drift and diffusion currents.
- Understand the general characteristics of various types of diodes including Zener diodes, light-emitting diodes, Schottky diodes, varactors, tunnel diodes, and photodiodes.
- Analyze diode circuits of moderate complexity.
- Design diode circuits of moderate complexity.
- Design circuits with various types of diodes.
1.1 Theory of Semiconductors

Most electronic devices are constructed using solid-state material, i.e., conductors, semiconductors, and insulators. It is important, therefore, that we understand the physics of these materials. All materials (matter) consist of atoms, which are the smallest unit of matter. Each atom comprises three basic particles: the proton, the neutron, and the electron. The positively charged proton and uncharged neutron form the nucleus at the center of the atom, while the negatively charged electron revolves around the nucleus in elliptical paths called shells. The outermost shell is called the valence shell, and the electrons that occupy this shell are called valence electrons. The Bohr models of hydrogen and helium, the two simplest atoms, are shown in Fig. 1.1.

![Hydrogen and helium atoms](image)

*Fig. 1.1* Hydrogen and helium atoms

The atom of hydrogen consists of a single proton and an electron moving around it. The helium atom consists of a nucleus containing two protons and two neutrons with two electrons moving around it. Each atom is built up from one other atom by adding electrons, protons, and neutrons with the number of protons always being equal to the number of electrons so that the atom is electrically neutral. The number of protons is known as the atomic number, and the number of neutrons is called the neutron number. Protons and neutrons are called nucleons, and the number of nucleons is called the mass number.
All elements are organized according to properties in a chart referred to as the periodic table. The difference between the atoms of the various elements making up this table lies in the number and arrangement of the constituent electrons, protons, and neutrons. Each atom is made up of energy levels or shells lettered K, L, M, N, O... containing orbiting electrons as shown in Fig. 1.2. Each electron must possess a certain discrete quantity of energy in order to occupy a certain shell, the inner most shell requiring the electron to have the lowest energy. Hence, the shells are said to be at certain levels of energy. The electron can move to a higher energy level by increasing its discrete amount of energy (such as by absorbing thermal energy) to the level associated with another energy level.

![Energy level of atom](Image)

Once there, it will only return to the lower level if it loses the required amount of energy that will allow it to occupy a lower energy level. Thus, the electron can only absorb or lose energy in discrete amounts. These energy levels are numbered first, second, third... and higher. Therefore, it follows that the electron shells lettered K, L, M, N,... correspond to the energy levels numbered 1, 2, 3, 4,..., respectively, each energy level represented by n. Each electronic shell comprises
sublevels, the number of sublevels being equal to the number of the energy level. Thus, the K shell or first energy level has one sublevel referred to as the s sublevel, the L shell or second energy level has two sublevels referred to as the s and p sublevels, and the M shell or third energy level has three sublevels, namely, s, p, and d sublevels, while the N shell or fourth energy level has four sublevels which are s, p, d, and f. Each sublevel in a shell has a slightly different energy level. Finally, each sublevel is made up of orbitals, each containing at most two electrons. The s sublevel has one orbital which is spherical, the p sublevel has three orbitals which are elliptical, the d sublevel has five orbitals, and the f sublevel has seven orbitals. The orbitals take the name of the sublevel in which they occur.

The electrons in the outermost shell, referred to as valence electrons, determine the chemical properties of the element. This number is equal to the number of the group in the periodic table of elements to which the atom belongs. Thus, lithium with atomic number 3, sodium with atomic number 11, and potassium with atomic number 19 all have one valence electron and, therefore, belong to Group I in the periodic table.

1.1.1 Energy Levels

In a material, the valence electrons are bound in a crystalline structure. However, it may be possible in some materials to break free of these inter-atomic or inter-molecular bonds and be capable of moving about in a conduction mode if sufficient energy is applied for these electrons. Thus, these electrons can move from the valence band where they are bound to the conduction band where they are free. These two bands may or may not overlap.

When the bands overlap as in Fig. 1.3, there is no energy gap between the valence electrons and the conduction or free electrons, and hence in materials where this occurs, the valence electrons are loosely bound to the nucleus and can freely move about the structure. This movement of valence/conduction electrons, usually under the influence of an applied electric potential, is conduction, and such materials are referred to as conductors. The electric attraction between the electron cloud of conduction electrons and the atomic nuclei in the structure constitutes the metallic bond. Examples of conductors include
metals such as silver, gold, copper, zinc, aluminum, and lead in which the valence electrons are freely available for conduction.

When the conduction band and the valence band do not overlap as in Fig. 1.4, an energy gap or forbidden band exists between them. In this case, a discrete amount of energy is required to move the valence electron from its band in the structure into the conduction band. If the gap is narrow (requiring a relatively small amount of energy to overcome atomic attraction as provided, e.g., by ambient light and heat), then the material in which this occurs is called a semiconductor. Examples of semiconductors and the required energy for the generation of free carriers are germanium with a gap energy $E_g = 0.67$ eV, silicon with $E_g = 1.11$ eV, gallium(III) arsenide (GaAs) with $E_g = 1.43$ eV, and cadmium sulfide (CdS) with $E_g = 1.73$ eV. Some
electrons are, therefore, available for conduction through excitation though not as many as in conductors.

![Diagram of energy bands in a semiconductor](image)

**Fig. 1.4** Separation of valence and conduction bands in a semiconductor

When the conduction band and the valence band are widely separated as in Fig. 1.5, the energy gap is large with $E_g \gg 1$. An extremely large amount of energy is required to move the valence electron from its band in the crystal structure into the conduction band. Such materials do not therefore normally conduct, as no conduction electrons are available, and are called insulators. Examples of such materials are mica, glass, porcelain, and rubber.
Fig. 1.5 Separation of valence and conduction bands in an insulator

If the temperature is raised in a conductor, the lattice vibrates and this results in more collisions with electrons. Such increased collisions manifest themselves as increasing resistance in the conductor. Conductors are therefore said to have a positive temperature coefficient of resistance. On the other hand, increased temperature in the semiconductor results in a greater number of electrons moving from the valence band to the conduction band, thereby increasing the conductivity of the semiconductor. Semiconductors therefore have a negative temperature coefficient of resistance.

Materials that are insulators at room temperature can become conductors at a suitably high temperature. The increased temperature would result in bonds being broken and electrons becoming free for conduction. The bond in semiconductors and insulators is called a
covalent bond and involves sharing of electrons from different atoms. In the germanium atom, there are 32 orbiting electrons, while silicon has 14 orbiting electrons. Both belong to Group IV of the periodic table, which means each has four electrons in the valence shell (and hence the ionization energy required to remove any one of these electrons is lower than other electrons within the atoms). Therefore, in silicon (Fig. 1.6) or germanium, the atoms are bound in a lattice structure in which each atom shares its four valence electrons with four neighboring atoms so that stable electron octets are formed in each atomic or valence shell. This sharing mechanism results in inter-atomic forces that bind the atoms in a crystalline structure. These bonds are called covalent bonds. While the valence electrons are bound tightly in the crystalline structure of the material, it is possible for them to absorb enough energy from ambient light or heat energy to break the covalent bond and become free for conduction. This corresponds to overcoming the energy gap $E_g$ as shown in Fig. 1.4. The closer the atomic spacing in the materials, the greater are the inter-atomic forces and hence, the greater is the energy gap.
**1.1.2 Intrinsic (Pure) Semiconductor**

The two main semiconductor materials used in the manufacture of semiconductor devices are germanium and silicon. An atom of either substance may be represented by a central core of positive charge $4e^+$ surrounded by four orbiting electrons each having a negative charge $e^-$. In the solid-state structure, silicon and germanium form a lattice in which all the atoms are equidistant from their immediate neighbors as shown in Fig. 1.6. Each atom having four neighbors meets this
equidistant requirement. In the crystal lattice, each atom forms a covalent bond with its four neighbors, each bond involving two valence electrons, one from each atom. Thus, each bond pair traverses an orbit around both the parent atom and the neighboring atom; thus enabling each atom to have effectively a stable state of eight electrons in its valence shell. This arrangement provides the lattice with a strong, stable, and regular structure.

Despite the strength of the bonds, energy from ambient light and heat is sufficient to overcome the energy gap $E_g$ and to cause some of the bonds to be broken and the electrons to be free. When a covalent bond is broken, a hole–electron pair is created, and both the hole and the free electron are known as charge carriers. They can thereafter move under the action of an applied electric field and contribute to electrical conduction. If the temperature of the material increases, thermal energy causes the breaking of additional covalent bonds and the consequent release of additional electrons. As a result, the conductivity of the crystal increases. This means that as indicated earlier, semiconductor material has a negative temperature coefficient of resistance.

When an electron escapes from a covalent bond, there is an absence of an electron, which since this constitutes a missing negative charge $e^-$, is equivalent to a positive charge $e^+$. Such an area in the crystal lattice is called a hole. A hole exerts an attractive force on an electron, and it can be filled by an electron that has been thermally liberated from a covalent bond. This process is called recombination, and it causes a continual loss of holes and free electrons. At a given temperature, a dynamic equilibrium is reached such that the rate of generation of electrons and holes is equal to the rate of recombination, thus resulting in a constant number of holes and free electrons. Both the hole and the electron are known as charge carriers, though the electron conduction (electron current) is different from hole conduction (hole current). The motion of holes is in a direction opposite to the motion of electrons, and the holes behave as positively charged particles. Holes and electrons move through a crystal by either diffusion or drift. Under normal circumstances, thermal energy causes random electron movement in a semiconductor with no net flow of charge. However, if an increased concentration of electron or holes occurs at one end of the
semiconductor by some mechanism, this gives rise to a net flow referred to as a diffusion current away from that area. Drift occurs when there is net charge movement under the action of an externally applied electric field. The velocity of the movement is called drift velocity, and this movement of holes and electrons through the crystal lattice is referred to as drift current. The electrons travel faster than the holes since while the electrons undergo direct translation due to the field, the movement of the holes in the opposite direction of the electrons involves a series of discontinuous electron movements into and out of covalent bonds. Conduction of current in a pure semiconductor is known as intrinsic conduction. Since the charge carriers are thermally generated, the concentration of these carriers increases with temperature. As a result, the conductivity of intrinsic semiconductors increases with temperature at the approximate rate of 5% per degree Celsius for germanium and 7% per degree Celsius for silicon.

1.1.3 Extrinsic (Impure) Semiconductor
The electrical characteristics of intrinsic semiconductor material can be significantly changed by the introduction of a small number (1 in 10^7) of certain atoms of impurity into the semiconductor material. This process of introducing impurity atoms into pure semiconductor crystal is called doping. A treated crystal is said to be doped and is called extrinsic material. Since the number of impurity atoms is much smaller than the number of atoms of the crystal, the crystal lattice is essentially undisturbed, and four crystal atoms surround each impurity atom. Two types of extrinsic materials of great importance in semiconductor device fabrication are n-type and p-type. Both types are formed by the addition of a specific amount of impurity atoms into a silicon or germanium base.

1.1.3.1 n-Type Material
The n-type material shown in Fig. 1.7 is formed by the addition of impurity atoms of elements from Group 5 of the periodic table which have five valence electrons. Examples of these elements are arsenic, antimony, and phosphorus. In a silicon crystal, each of the impurity atoms, for example, phosphorus, will take the place of one of the silicon atoms in the crystal lattice, and because the number of impurity atoms
is small, the crystal lattice will be essentially undisturbed. As a result, four silicon atoms surround each impurity atom, and each phosphorus atom will establish covalent bonds with the four neighboring silicon atoms. This means that one valence electron in the phosphorus atom is unused. This surplus electron is only loosely bound to its parent atom. It easily breaks free and is available for conduction. The impurity atom has, therefore, donated a conduction electron to the crystal lattice. A free electron is created in the silicon crystal lattice without the creation of a corresponding hole. (A positive charge does remain in the parent atom, but since no bond is broken, the attraction of this charge for free electrons is not as great as when a bond is broken.) Hole-electron pairs are however still produced by thermal energy. Because of the impurity, the number of the free electrons in the lattice greatly exceeds the number of holes, and therefore, the crystal is called n-type. The impurity atom is called a donor atom because it donates a free electron to the crystal lattice. In n-type material, electrons are the majority charge carriers and holes are the minority charge carriers. The above discussion also holds for a germanium crystal lattice. Note that the crystal is still neutral overall. The effect of the doping process on the crystal conductivity can be described using the energy band diagram. As a result of the doping, a donor energy level appears in the forbidden band with gap energy $E_g$ significantly less than that possessed by the intrinsic material. Thermal energy is sufficient at room temperature to move these electrons into the conduction band, thereby increasing the conductivity of the semiconductor. At room temperature in intrinsic silicon, there is approximately one free electron for every $10^{12}$ atoms (1–$10^7$ for germanium). For a doping level of 1 donor atom in every $10^7$ silicon atoms, the ratio $10^{12}:10^7$ indicates an increase in free electrons by a ratio 100,000:1.
1.1.3.2 p-Type Material

The p-type material shown in Fig. 1.8 is formed by the addition of impurity atoms of the elements from Group 3 instead of Group 5 of the periodic table. These have three valence electrons. Examples of these elements are boron, gallium, and indium. When boron impurity atoms are introduced into the silicon crystal lattice, each boron atom will again take the place of a silicon atom in the lattice with its three valence electrons. It will form covalent bonds with three of the four neighboring...
silicon atoms. Since only three bonds are formed, one hole (position for bond formation) is introduced into the lattice for each impurity atom. This hole is free to conduct as thermally generated holes, which continue to be produced. Because of the impurity, the number of free holes in the crystal lattice is much greater than the electrons, and hence the material is called p-type. The impurity atoms are called acceptor atoms. Again the p-type material is electrically neutral. Holes are the majority charge carriers, and electrons are the minority charge carriers in p-type semiconductor material.
1.2 Current Flow in Semiconductor Diodes

Consider p-type and n-type semiconductor materials that are brought into contact, forming a junction between them as shown in Fig. 1.9. Recall that both regions contain charge carriers of either sign though in the n-type region electrons are the majority carriers and in the p-type region holes are the majority carriers. Such an arrangement of p-type and n-type material in contact is referred to as a semiconductor diode. The symbol for the diode is shown in Fig. 1.10, with the arrow pointing in the direction p to n. The terminal on the p side is referred to as the anode, while that on the n side is referred to as the cathode. An external voltage applied to the two terminals is referred to as a bias. Below we consider the situations of zero bias (where the external voltage is zero), reverse bias (where the external voltage is applied such that the anode is negative relative to the cathode) and forward bias (where the external voltage is such that the anode is positive relative to the cathode).

Fig. 1.9  p-Type and n-type material in contact forming a semiconductor diode

1.2.1 Zero Bias
Consider the case where the externally applied voltage is zero as shown in Fig. 1.11. In both the regions, there is a high probability that the minority charge carriers will meet and recombine with majority charge carriers and as a result, the lifetime of the minority charge carriers is short. While there is random movement of free electrons and holes in the lattice, the initial high concentration of electrons in the n-type and holes in the p-type results in a net movement of electrons from n-type to p-type and holes from p-type to n-type. This process is known as diffusion and it indicates the tendency for charge carriers to move away from areas of higher concentration to lower concentration areas.

As the n-type region loses negative charge carriers and gains positive charge carriers, and the p-type region loses positive charge carriers and gains negative charge carriers, the n-type region close to the junction is depleted of electrons and becomes positively charged, and the p-type region close to the junction is depleted of holes and becomes negatively charged. The region in the vicinity of the junction, therefore, becomes depleted of majority carriers and is called the depletion region. It has a relatively high resistivity and is of the order of 0.001 mm wide. The migration also causes a buildup of positive charges in the n-type region close to the junction and negative charges in the p-type close to the junction. This results in a potential across the junction called a barrier potential. It is directed such that further majority
change diffusion across the junction is reduced though majority carriers with sufficient energy are able to overcome the barrier potential and migrate to the other side. Minority charge carriers (electrons in the p-type material and holes in the n-type material) that enter the depletion region are swept across the junction to the other side by the action of the barrier potential. A dynamic equilibrium is reached so that the majority charge carrier or diffusion current and minority charge currents are equal, and hence the net current across the junction is zero. It should be noted that the crystal is electrically neutral both before and after diffusion. The net flow of charge in any direction for a semiconductor diode is zero when the externally applied voltage is zero.

1.2.2 Reverse-Biased Diode
The reverse bias condition exists when an external voltage, $V_D$, is applied across the p–n junction with the positive potential being connected to the n-type material and the negative potential being connected to the p-type material. This is shown in Fig. 1.12. Under the action of this potential, majority charge carriers are attracted away from the junction, thereby further depleting this region. This increases both the magnitude of the potential barrier and the width of the depletion region. Fewer majority carriers have sufficient energy to break through the barrier potential, and hence the majority charge current decreases eventually going to zero with increasing reverse bias. The minority charge current, which was aided by the barrier potential, increases quickly reaching its maximum value where all the minority charges which are thermally generated are swept across the junction. This current is called the reverse saturation current and flows from n to p in Fig. 1.12, according to conventional current flow. (Note that this current comprises holes flowing from n to p and electrons flowing from p to n.) The reverse saturation current for germanium is typically 1–2 $\mu$A at room temperature, while that for silicon is much lower at 10–20 nA. This current approximately doubles in value for every 10 °C rise in temperature.
1.2.3 Forward-Biased Diode

The forward-biased condition exists when an external voltage $V_D$ is applied across the p–n junction with the negative potential being connected to the n-type material and the positive potential being connected to the p-type material. This is shown in Fig. 1.13. Under these conditions, holes (majority carriers) are repelled from the p-type material toward the junction, and electrons (majority carriers) are repelled from the n-type material toward the junction. This movement of holes and electrons toward the junction results in a reduction of the width of the depletion layer and consequently the magnitude of the potential barrier.
Majority carriers from each material can now cross the junction under the action of the electric field. Even though the minority charge current flow remained constant, the increase in majority current flow results in a net increase in conventional current across the junction from p-type material to n-type material (holes from p to n and electrons from n to p). This current increases rapidly with an increase in the forward bias $V_D$ according to an exponential curve as shown in Fig. 1.14. The curve shows a sharp corner at about $V_D = 0.7$ V for silicon and $V_D = 0.3$ V for germanium. Below this voltage, the current through the diode is quite small, while above this voltage, there is a large current flow. This voltage can, therefore, be viewed as a threshold voltage above which the diode is on and $V_D$ is constant and below which the diode is off.
1.3 General Characteristic of a Diode

From solid-state physics, the relationship between diode voltage $V_D$ and diode current $I_D$ is given by

$$I_D = I_o \left( e^{\frac{qV_D}{nkT}} - 1 \right)$$

where:

$I_o$ = reverse saturation current,
\( q \) = electron charge \((1.6 \times 10^{-19} \text{ Coulombs})\),
\( k \) = Boltzmann’s constant \((1.38 \times 10^{-23} \text{ J/K})\),
\( T \) = absolute temperature in degrees Kelvin,
\( m \) = an empirical constant between 1 and 2.

If we let \( V_T \) be the thermal voltage given by \( V_T = \frac{kT}{q} \), then Eq. (1.1) becomes

\[
I_D = I_o \left( e^{\frac{V_D}{mV_T}} - 1 \right)
\]

Equation (1.2) approximately represents the diode characteristic shown in Fig. 1.14. It can be written as

\[
I_D = I_o e^{\frac{V_D}{mV_T}} - I_o
\]

Thus for positive values of \( V_D \) (forward bias), \( I_D \gg I_o \) in which case

\[
I_D \approx I_o e^{\frac{V_D}{mV_T}}
\]

The reverse saturation current \( I_o \) depends on the level of doping and diode geometry. The empirical constant \( m \) is a function of diode construction and can vary according to voltage and current levels. For germanium diodes, \( m = 1 \), while for silicon diodes, \( m = 1 \) for values of current above that corresponding to the threshold voltage (for \( m = 1 \), \( mV_T = 26 \text{ mV at} \ 25 \degree C \)).

The DC or static resistance of a diode corresponds to the ratio \( V_d/I_d \) where \( V_d \) and \( I_d \) are the operating DC voltage and current. This parameter is of less significance than the AC or dynamic resistance. At a particular operating point, we can evaluate the AC or dynamic resistance \( r_d = \Delta V_d/\Delta I_d \) of the diode where \( \Delta \) indicates a small change in the relevant quantity. \( \Delta V_d/\Delta I_d \) represents the inverse slope of the diode characteristic at a particular operating point as shown in Fig. 1.15. Thus, differentiating \( I_D \) in Eq. (1.4) with respect to \( V_D \) gives
Fig. 1.15  Silicon diode characteristic showing dynamic resistance

Hence,

$$r_d = \frac{dV_D}{dI_D} = \frac{mV_T}{I_D} = \frac{26 \text{ mV}}{I_D (\text{mA})}$$  \hspace{1cm} (1.6)
Example 1.1  Determine the dynamic resistance of a semiconductor diode for 1 mA current through the diode.

Solution  Using Eq. (1.6), the dynamic resistance for a 1 mA current flow is given by 
\[ r_D = \frac{26 \text{ mV}}{1 \text{ mA}} = 26 \ \Omega. \]

In addition to the dynamic resistance, there are the resistance of the semiconductor material and the resistance between the diode material (body resistance) and the external metallic conductor (contact resistance). We use the designation \( r_F \) to denote the diode forward resistance comprising \( r_D \), body resistance, and contact resistance.

1.3.1 Breakdown Region
If the reverse bias voltage across a diode is increased beyond a certain value, the reverse current increases rapidly, and the junction is said to have broken down as shown in Fig. 1.16. This critical voltage is called the breakdown voltage of the junction. Two effects cause this breakdown:

(a)  The Zener effect occurs when the electric field across the junction is strong enough to break covalent bonds in the lattice and thereby generate carriers. This effect occurs primarily at low levels of breakdown voltage or Zener voltage \( V_Z \) corresponding to high doping levels in the p- and n-type materials.

(b)  The avalanche effect occurs when the charge carriers are accelerated by the electric field of the reverse bias to the extent where they create carriers by collision.
For voltages less than about 5 V, the Zener breakdown mechanism prevails, while for voltages above 5 V, the avalanche breakdown mechanism is dominant. While the Zener breakdown mechanism is a significant contributor to the breakdown process only at low levels of $V_Z$, the breakdown region is called the Zener region, and diodes designed to operate in this part of the p–n junction characteristic are
called Zener diodes (see Sect. 1.5.1). Such diodes exploit the steep characteristic gradient to maintain a constant voltage even with changing reverse diode current. In general, the Zener region of the semiconductor diode must be avoided if the diode is not to be destroyed. For Zener diodes designed to operate in this region, current limiting must be introduced (usually by the inclusion of a resistor) in order to prevent diode failure. The maximum reverse bias potential that can be applied before breakdown is called the peak inverse voltage (PIV) or the peak reverse voltage (PRV).

1.3.2 Diode Specifications

The data defining the characteristics of a diode are supplied by the manufacturer and include the following:

1. Forward voltage $V_F$ (at a specified current and temperature).
2. Maximum forward current $I_F$ (at a specified temperature).
3. Reverse saturation current $I_R$ (at a specified voltage).
4. PIV rating (or PRV).
5. Maximum power dissipation.
6. Operating temperature range.
7. Reverse recovery time.
8. Capacitance.

Diodes are often rated according to their power handling capability. The physical construction of the diode determines its rating, and this information is included in the manufacturer’s specification. Another diode rating is the current carrying capacity or forward current. The instantaneous power dissipated by a diode is given by the relation

$$P_D = I_D V_D.$$
1.4 Diode Types

There is a variety of diodes available for electronic circuit design and application. These include Zener diodes, signal diodes, power diodes, varactor diodes, light-emitting diodes, photodiodes, PIN diodes, and Schottky diodes. Each of these is briefly discussed in the following sections.

1.4.1 Zener Diodes

The Zener diode is a diode designed to be operated in the Zener region as shown in Fig. 1.18. Its symbol is shown in Fig. 1.17, and it exploits the steep slope of the diode characteristic in the reverse bias region. As can be seen from the diode characteristic in Fig. 1.18, the voltage in this region is almost constant for varying current. The actual Zener voltage $V_Z$ is determined by the doping levels in the Zener diode with increased doping resulting in the reduction of $V_Z$. Zener diode voltages $V_Z$ vary from 1.8 V to about 200 V with a tolerance of about ±5% and power ratings from $\frac{1}{4}$ W to about 50 W. Silicon is usually preferred in the manufacture of Zener diodes due to its higher current and temperature capability.

![Fig. 1.17 Symbol for Zener diode](image)
In the on state, Zener diodes have a low dynamic resistance $r_Z$, which is the reciprocal of the slope of the Zener curve given by $r_Z = \Delta V_Z/\Delta I_Z$, and the equivalent circuit may be shown as a battery of voltage $V_Z$ in series with $r_Z$. In most applications, however, $r_Z$ is quite small as compared with other circuit resistance, and hence can be ignored. This resistance is current dependent and decreases with
increased current. $V_Z$ is itself temperature dependent. Its value may increase or decrease with changes in temperature. The temperature coefficient $T_C$ is an indicator of this and is given by

$$
T_C = \frac{\Delta V_Z}{V_Z(T_1 - T_0)} \times 100\% / ^\circ C
$$

(1.7)

where $\Delta V_Z$ is the change in Zener voltage $V_Z$ resulting from the temperature change from $T_0$ to $T_1$. $T_C$ can be positive or negative reflecting an increase of $V_Z$ with temperature or a decrease of $V_Z$ with temperature, respectively. It turns out that the temperature coefficient associated with the avalanche breakdown mechanism is positive, while that for the Zener breakdown diodes is negative. The result is that Zener diodes at the 5 V mark tend to have very low temperature coefficients and are, therefore, best suited for use as stable reference voltages.

**Example 1.2** A Zener diode has $V_Z = 8.2$ V at 25 °C. If the diode has $T_C = 0.05\% / ^\circ C$, determine the Zener voltage at 75 °C.

**Solution** Using Eq. (1.7),

$$
\Delta V_Z = \frac{V_Z}{100} T_C (T_1 - T_0) = \frac{8.2}{100} \times 0.05 \times (75 - 25) = 0.205V,
$$

Therefore, $V_Z$ at 75 °C is $V_Z (75 °C) = V_Z + 0.205 = 8.2 + 0.205 = 8.405$ V.

In operating the Zener diode, the reverse current through the device must not fall below a minimum value $I_{Zmn}$ as shown in Fig. 1.18 in order that the Zener voltage does not fall below its operating value $V_Z$. Also, the reverse current must not exceed the maximum value $I_{Zmx}$ set by the Zener power rating.

**Example 1.3** If the 8.2V Zener used in Example 1.2 has a power rating of 500 mW, determine the maximum reverse current $I_{Zmx}$ 25 °C.

**Solution** The power $P_D$ dissipated in a Zener diode is given by

$$
P_D = V_Z I_Z
$$

where $V_Z$ is the Zener voltage and $I_Z$ is the Zener current.
Therefore, the maximum Zener current $I_{Zmx}$ is given by

$$I_{Zmx} = \frac{P_D}{V_Z} = 500 \text{ mW}/8.2 \text{ V} = 61 \text{ mA}.$$  

The standard Zener voltages available are listed in Table 1.1.

<table>
<thead>
<tr>
<th>Table 1.1</th>
<th>Standard Zener diode voltages</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.0</td>
<td>2.2</td>
</tr>
<tr>
<td>3.6</td>
<td>3.9</td>
</tr>
<tr>
<td>6.2</td>
<td>6.8</td>
</tr>
<tr>
<td>11</td>
<td></td>
</tr>
<tr>
<td>2.4</td>
<td>2.7</td>
</tr>
<tr>
<td>4.3</td>
<td>4.7</td>
</tr>
<tr>
<td>7.5</td>
<td>8.2</td>
</tr>
<tr>
<td>12</td>
<td>13</td>
</tr>
<tr>
<td>3.0</td>
<td>3.3</td>
</tr>
<tr>
<td>4.7</td>
<td>5.1</td>
</tr>
<tr>
<td>8.2</td>
<td>9.1</td>
</tr>
<tr>
<td>15</td>
<td>16</td>
</tr>
<tr>
<td>3.3</td>
<td>5.6</td>
</tr>
<tr>
<td>9.1</td>
<td>10</td>
</tr>
<tr>
<td>16</td>
<td>18</td>
</tr>
</tbody>
</table>

Zener diodes whose voltages are a factor of ten times the values in the table are available up to 150 V.

### 1.4.2 Signal Diodes

Signal diodes are diodes designed to process voltages and currents of small value. Such devices are used in telecommunications, electronic signal processing, and computer switching circuits. The characteristics of this class of diodes include low forward resistance and junction capacitance. The PIV rating is moderately high (25–250 V), and the forward current rating is in the range 40–250 mA. These diodes are available singly or in arrays for convenience of implementation. One popular example is the 1N4148. This diode has a PIV of 100 V, a forward current of 300 mA, a power dissipation of 500 mW, and a diode capacitance of 4 pF.

### 1.4.3 Power Diodes

This class of diodes is important in signal rectification, which is converting AC to DC for power applications. These include the half-wave rectifier and the full-wave rectifier discussed in Sects. 1.6.4, 1.6.5, and 1.6.6, circuits that find wide application in a range of electronic systems. The important parameters are the PIV, which is typically 50–1000 V, the forward current that is of the order of 1–100 A, and the low forward resistance of less than 1 Ω. Power diodes come in single units and in packages of four for bridge applications. The 1N4001 series is a family of general purpose diodes rated at 1 A, while the 1N5400 series
is rated up to 3 A. The PIV for both series varies between 50 and 1000 V.

### 1.4.4 Varactor Diodes

A varactor diode is a p-n junction diode designed to have a significant junction capacitance that can be varied by varying the reverse voltage on the junction. All p-n junctions comprise p-n semiconductor material bounding a region of high resistance called the depletion layer. This arrangement constitutes a capacitor whose value $C$ given by

$$C = \frac{\varepsilon A}{W}$$

where $\varepsilon$ is the permittivity of the material constituting the capacitor, $A$ is the junction area, and $W$ is the width of the depletion layer. The width increases with an increase in the applied reverse potential with the result that the junction capacitance of the diode decreases. The typical capacitance of these diodes is in the range 100–500 pF. These diodes are used for electronic tuning of a variety of circuits including tuners, oscillators, and filters. The symbol for the varactor diode is shown in Fig. 1.19.

![Varactor diode](image)

**Fig. 1.19** Varactor diode

### 1.4.5 Light-Emitting Diodes

A light-emitting diode or LED is a diode that emits light as a result of the passage of current through the diode. The current flow excites electrons within the semiconductor material of the LED to higher energy levels after which they fall back to lower levels, thereby releasing energy in the form of light. The material of the LED determines the specific color of the light as well as its turn-on voltage. LEDs are constructed from gallium phosphide (GaP), silicon carbide (SiC), and gallium arsenide phosphide (GaAsP).

The typical current rating of these devices is between 10 and 50 mA. The color and associated forward voltage drops for several LED types are given Table 1.2. Its symbol is shown in Fig. 1.20.

**Table 1.2** Light-emitting diodes
<table>
<thead>
<tr>
<th>Material</th>
<th>Color</th>
<th>Forward voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaAsP</td>
<td>Red</td>
<td>1.8</td>
</tr>
<tr>
<td>GaP</td>
<td>Green</td>
<td>2.1</td>
</tr>
<tr>
<td>GaAsP</td>
<td>Yellow</td>
<td>2.0</td>
</tr>
<tr>
<td>GaAsP</td>
<td>Orange</td>
<td>2.0</td>
</tr>
<tr>
<td>SiC</td>
<td>Blue</td>
<td>3.0</td>
</tr>
<tr>
<td>GaN</td>
<td>White</td>
<td>4.1</td>
</tr>
</tbody>
</table>

**Fig. 1.20** Symbol for light-emitting diode (LED)

The forward voltage drop during turn-on is higher than for ordinary silicon diodes. Moreover, the PIV rating is substantially lower and is typically between 3 and 5 V. These devices must, therefore, not be subjected to large reverse voltages and can be protected by the inclusion of an ordinary diode $D_2$ in parallel with the LED as shown in Fig. 1.21. A series resistor $R_1$ is required to limit the forward current. The LED is a very efficient device and radiates very little heat during operation. It is unaffected by shock or vibration, and there is no surge current at turn-on. As a result, the device has a long life.

**Fig. 1.21** Method of protection for LED
Thus if the peak value of $V_{ac}$ is 15 V, then if $D_1$ is a green LED with forward voltage 2.1 V, allowing a peak current of 10 mA, it follows that $R_1 = (15 - 2.1)/10 \text{ mA} = 1.3 \text{ k}$. Essentially, the same calculation is used to determine the limiting resistor for a DC voltage source. In that case, the protection diode $D_2$ would not be necessary.

**Example 1.4** For the circuit shown in Fig. 1.22, determine the value of $R_1$ if the LED $D_1$ is red.

**Solution** Since a red LED has a forward voltage of 1.8 V, for an LED current of 15 mA, the value of $R_1$ is given by $R_1 = (12 - 1.8)/15 \text{ mA} = 680 \Omega$.

**1.4.6 Photodiodes**
A photodiode is a diode that responds to light. The case of the diode is constructed with a transparent area so that the incident light can fall on the p–n junction within. This energy generates additional holes and electrons from the crystal lattice, which are then swept away from the junction by an impressed reverse bias. The resulting current flow adds to the existing reverse saturation current, thereby increasing its value. Thus, light falling on a photodiode increases its reverse saturation current, and a typical family of curves corresponding to varying reverse bias voltages and reverse saturation current for various light intensities
is shown in Fig. 1.23. As can be seen, for incident light at some fixed intensity, there is very little change in the current as the reverse bias is increased. In order to reduce the current to zero, the reverse bias must be reduced to zero and changed to a forward bias of typically 0.3 V at which point the current begins to drop. It falls to zero when the forward reaches about 0.5 V. The current that flows with no incident light is referred to as dark current. The change of current with light intensity corresponds to a change in diode resistance. The symbol for the photodiode is shown in Fig. 1.24.

**Fig. 1.23** Current (I) vs voltage (V) characteristics for a photodiode
1.4.7 PIN Diodes

The PIN diode shown in Fig. 1.25 is a diode designed for low capacitance. It comprises heavily doped p and n regions separated by a layer of intrinsic silicon (hence PIN). Because of its construction, the diode has a very low forward resistance, an extremely high reverse resistance, a high PIV rating, and a low reverse capacitance. This low capacitance enables the diode to be employed in high-frequency switching applications.

1.4.8 Schottky Diodes

The Schottky or hot carrier diode is a semiconductor diode with a low forward voltage drop and fast switching action. It is constructed by fusing a metal region, e.g., platinum, to an n-type region. The resulting diode has virtually no charge storage and, therefore, has a short reverse recovery time. It is therefore useful in high-speed switching applications involving large forward currents. During forward bias, electrons move from the n-type region where they predominate to the metal region. The Schottky diode voltage–current characteristic is similar to that of a power diode. It, however, has a lower threshold voltage of about 0.3 V. As the reverse breakdown voltage increases for this diode, the forward voltage also increases. The symbol for this diode is shown in Fig. 1.26.
1.5 Diode Circuits
Having discussed the various types of diodes and their characteristics, in this section we examine the operation and design of several applications of these devices.

1.5.1 DC Circuits
In general, a diode is in the “ON” state if the current established by the applied source is such that its direction matches that of the arrow in the diode symbol. This generally corresponds to $V_D \geq 0.7$ V for silicon and $V_D \geq 0.3$ V for germanium. Analyzing diode circuits with DC inputs is quite simple and involves applying standard circuit laws.

Example 1.5 In the circuit shown in Fig. 1.27, find the current $I$ flowing through the resistor.

Solution In the circuit shown, the voltage drop across the diode is 0.7 V, and hence the voltage across the resistor is $(9 - 0.7)$ V. Therefore, the current $I$ in the circuit is given by $I = (9 - 0.7)/4.7$ k = 1.8 mA. If $D_1$ is a red LED with forward voltage 1.8 V, then $I = (9 - 1.8)/4.7$ k = 1.5 mA.
1.5.2 Clippers

There is a class of diode networks called clipper circuits that have the ability to “clip” off a portion of a signal without affecting the remaining part of the alternating waveform. Such circuits are useful in protecting electronic equipment against voltage surges. The basic circuit of the clipper is shown in Fig. 1.28.

![Clipper circuit](image)

**Fig. 1.28** Clipper circuit

As the input voltage goes more positive than the reference voltage $V_{\text{ref}}$, the diode $D_1$ turns on. Current then flows from the input signal source through the diode and causes a voltage drop across $R_1$ so that the excess input voltage is reduced. The result is that the output voltage is limited to a maximum value equal to $(V_{\text{ref}} + V_D)$. For an input voltage that is less positive than $V_{\text{ref}}$ or of negative polarity, diode $D_1$ turns off, and the full input signal waveform appears at the output terminals of the circuit. Figure 1.29 shows the clipped output waveform for an input sinusoidal voltage waveform.

![Clipped voltage waveform](image)

**Fig. 1.29** Waveform of “clipped” voltage signal
If the diode and the polarity of the reference voltage are reversed, the input voltage signal will be clipped on the negative rather than the positive half-cycle. If bi-directional diodes are placed in parallel as shown in Fig. 1.30, then both the positive and the negative half-cycles of the input waveform will be clipped as shown in Fig. 1.31. The result is that the amplitude of the input signal waveform can be restricted to a maximum value on both half-cycles. The two reference voltages can be of different magnitude. If they are both set to zero as shown in Fig. 1.32, the output amplitude is limited to ±0.7 V. This circuit is used to protect some electronic circuits. The circuit can be further modified with the inclusion of Zener diodes to replace the reference voltages.

Fig. 1.30  Double polarity clipping circuit

Fig. 1.31  Waveform of voltage signal "clipped" for negative and positive half-cycles
### Example 1.6

Sketch the output waveform of the circuit shown in Fig. 1.33. The input is a symmetrical square wave input signal of amplitude $\pm 12$ V.

**Solution**

For the circuit in Fig. 1.33, as the input voltage goes to $+12$ V, the forward voltage of the diode and the battery voltage are both exceeded, and conduction through the diode occurs. The output voltage $V_o$ is then $V_o = 3 + 0.7 = 3.7$ V. When the input voltage goes to $-12$ V, the diode turns off, and hence there is no conduction. The output voltage is then $-12$ V. The output waveform is shown in Fig. 1.34.
Example 1.7  Sketch the output waveform of the circuit shown in Fig. 1.35. The input is a symmetrical square wave input signal of amplitude ±12 V.

Solution  For the circuit in Fig. 1.35, as the input voltage goes to +12 V, the forward voltage of the diode, and the reverse voltage of the Zener
are both exceeded and conduction through both devices occurs.

The output voltage $V_o$ is then $V_o = 6.8 + 0.7 = 7.5$ V. When the input voltage goes to $-12$ V, the normal diode turns off and so does the Zener. The output voltage is then $-12$ V. The output waveform is shown Fig. 1.36.

![Output Waveform](image1)

**Fig. 1.36** Solution waveform for Example 1.7

**Example 1.8** Sketch the output waveform of the circuit shown in Fig. 1.37. The input is a sine wave input signal of peak amplitude ±10 V.

![Input Waveform and Circuit Diagram](image2)

**Fig. 1.37** Circuit and input waveform for Example 1.8
Solution For the circuit in Fig. 1.37, on the positive half-cycle as the input voltage amplitude increases, the forward voltage of the Zener diode is exceeded, and conduction through the device occurs. The peak output voltage $V_o$ is limited to 0.7 V. On the negative half-cycle of the input sine wave, as the amplitude increases negatively, the reverse voltage of the Zener is exceeded, and conduction in the reverse direction through the device occurs. The peak output voltage $V_o$ is limited to −4.7 V. The resulting clipped waveform is shown Fig. 1.38.

![Clipped Waveform](image)

*Fig. 1.38* Solution waveform for Example 1.8

There is another group of clippers in which the diode is in series with the output. The basic version to be considered here is shown in Fig. 1.39. For a positive going input waveform, the output signal assumes the value $V_{\text{ref}}$ when the input signal amplitude is less than $V_{\text{ref}}$ since then diode $D_1$ is off. However, $D_1$ conducts when the input amplitude exceeds $V_{\text{ref}}$. The output voltage amplitude is then the input amplitude less than the diode voltage drop. The resulting waveform is shown in Fig. 1.40. If the diode and the reference voltage are reversed, then the waveform is also reversed. The most popular version of this is when $V_{\text{ref}} = 0$ which is called a rectifier. This will be dealt with in Sect. 1.6.4.
The clamping network is one that will “clamp” a signal to a different DC level. It effectively shifts the level of the signal without changing the signal shape as in the clipping circuits. Two basic clamping circuits are
shown in Figs. 1.41 and 1.42. The time constant $CR$ of the circuit must be longer than the periodic time $T$ of the input waveform, i.e., $CR \gg T$. This ensures that the voltage across the capacitor does not discharge significantly during the interval that the diode is non-conducting. In the circuit in Fig. 1.41, the diode is OFF when the input voltage is positive. When the input voltage is negative, the diode turns ON, and the output voltage is then equal to the small voltage drop $V_D$ across the diode. The current flowing through the diode charges up the capacitor, and a voltage is developed across it, which is equal to the peak input voltage minus the diode voltage. When the next positive half-cycle arrives, the voltage across the output is equal to the sum of the applied input voltage and the voltage across the capacitor. (The capacitor attains its maximum voltage after a few cycles of the input waveform.) The result is that the output waveform has shifted in the positive direction by an amount equal to the capacitor voltage and the least positive value is clamped to just below $0$ V (diode voltage). The most positive part of the output voltage is then equal to twice the peak input voltage minus the diode voltage drop, i.e., $(2V - V_D)$ V. If the diode connection is reversed as in Fig. 1.42, the positive peak of the input voltage is clamped to just above $0$ V. The output voltage waveforms for a square wave input voltage are shown in Figs. 1.41 and 1.42.

![Clamping circuit with positive shift](image)

*Fig. 1.41* Clamping circuit with positive shift
If a reference voltage source $V_{ref}$ is connected in series with the diode, an input voltage can be clamped to that voltage instead of 0 V (approx.). The diagram in Fig. 1.43 shows a clamping circuit that includes a reference voltage $V_{ref}$. If the polarities of the diode and the reference voltage are reversed, then the input voltage will be clamped to $-V_{ref}$ instead of 0 V. It is interesting to note that the waveform is shifted in the direction of the diode and that amplitude above the zero reference is $(V_{ref} + V_D)$.

**Example 1.9** Sketch the output waveform for the circuit shown in Fig. 1.44. The input is a symmetrical square wave signal of amplitude $\pm 12$ V.
Solution  For the circuit in Fig. 1.44, as the input voltage goes to +12 V, the capacitor charges to \( V_C = 12 - 4 - 0.7 = 7.3 \) V through the forward-biased diode. The output voltage \( V_o \) is across the series battery-diode connection giving \( V_o = 4.7 \) V. When the input voltage goes to −12 V, the normal diode turns off, and the input voltage is in series with the voltage across the capacitor. This results in an output voltage of \( V_o = -12 - 7.3 = -19.3 \) V. The effect is that the output waveform is shifted negative by 7.3 V while still preserving the original waveform shape (Fig. 1.45).
1.5.4 Half-Wave Rectifier
The basic half-wave rectifier consists of a diode $D_1$ in series with an AC supply from a transformer and the load as shown in Fig. 1.46 where $V_s$ is the rms voltage. On the half-cycle in which the AC signal $V_s$ goes positive making the anode of the diode positive relative to its cathode, the diode conducts and current flows into the load in the direction of the diode. A DC voltage $V_{DC}$ is developed across the load. On the negative half-cycle of the input voltage, diode $D_1$ is reverse biased as its cathode is made more positive than its anode. There is, therefore, no current flow through the diode into the load, and the output voltage across the load is zero. The voltage output consists of a series of half sine wave pulses as shown in Fig. 1.47. When the diode is off, the peak voltage across it is equal to $\sqrt{2}V_s$, the peak voltage of the transformer voltage, and hence the PIV rating of the diode must exceed this value.
The problem with this arrangement is that there is considerable variation in the output voltage. Such a waveform is only suitable for applications such as battery charging where only the unidirectional nature of the voltage is important. In most equipment operated from such a supply, however, the voltage variations will appear as hum and noise at the output of the equipment. In general, the DC output of a rectifier is required to have little variation and a minimum of ripple.

One method of achieving this is to connect a reservoir capacitor $C$ across the output of the rectifier. The resulting supply shown in Fig. 1.48 is referred to as half-wave unregulated DC power supply. Each time $V_S$ goes sufficiently positive, the diode conducts, and the voltage across the capacitor increases to $V_{pk} = \sqrt{2}V_S$. This corresponds to point A in Fig. 1.49. When $V_S$ falls below the capacitor voltage, the diode turns off, and the capacitor discharges into the load at a rate determined by the time constant $CR_L$ seconds where $R_L$ is the load resistance. As the discharge occurs, the capacitor voltage $V_{DC}$ is
represented by the curve AB in Fig. 1.49. As \( V_S \) rises above the capacitor voltage at point B, the voltage at the anode of the diode exceeds the cathode voltage causing the diode to conduct. The capacitor is recharged and the cycle is repeated. The charging current \( I_D \) through diode \( D_1 \) takes the form of large pulses as shown in Fig. 1.49, which the diode must be able to handle.

![Diagram of half-wave unregulated DC supply](image)

**Fig. 1.48** Half-wave unregulated DC supply

For small load currents, the capacitor discharge between charging pulses is small, and hence the average output voltage is only slightly less than \( V_{DC} = \sqrt{2}V_S \). Since the capacitor voltage adds to the transformer voltage when the diode turns off, the PIV is increased to
twice the peak secondary voltage, i.e., \( 2\sqrt{2}V_s \). A large load current causes \( C \) to discharge more rapidly, and this results in a greater variation in the output voltage. Although increasing \( C \) will reduce this variation, the maximum value of capacitance that can be employed is limited since as the capacitance value is increased, an increasing current is required to recharge the capacitor. This means that the amplitude of the current pulses in Fig. 1.49 will increase and appropriately rated diodes will have to be employed to handle this larger forward current. The fluctuating unidirectional voltage appearing across the load may be regarded as a DC voltage with an AC voltage component. This AC voltage is known as the ripple voltage.

To calculate the peak-to-peak value \( \Delta V \) of the output ripple and the average output voltage, certain approximations need to be made. Specifically, from Fig. 1.49 for the half-wave rectifier, the diode is off for most of the period \( T \). During this time, the capacitor delivers a load current \( I_{DC} \) and, therefore, discharges in the process. The decay is exponential but can be approximated as a linear decay. Also, the load current is assumed to be approximately constant during the discharge. For a capacitor, the relationship \( I = C\frac{dV}{dt} \) holds. This can be approximated by \( I \approx \frac{\Delta V}{\Delta t} \) where \( \Delta V \) is a small change in capacitor voltage and \( \Delta t \) is the associated small time interval over which this voltage change occurs. For the half-wave rectifier,

\[
I_{DC} = C\frac{\Delta V}{\Delta t} = C\frac{\Delta V}{T_H}
\]

where \( \Delta V \) is the change in voltage of the reservoir capacitor and \( T_H \approx \Delta t \) is the period of the half-wave rectified waveform. From this, the peak-to-peak output ripple is given by

\[
\Delta V = \frac{I_{DC}T_H}{C} = \frac{I_{DC}}{Cf}
\]

where \( f = 1/T_H \) is the frequency of the input voltage. From this, the average DC output voltage is

\[
V_{DC} = V_{pk} - \Delta V/2
\]
Example 1.10  Design a half-wave unregulated power supply delivering 12 V DC at 1 A with less than 2.5 V peak-to-peak ripple.

Solution  Since the peak transformer voltage is greater than the root mean square value by a factor of 1.414, it is reasonable to choose the transformer voltage $V_{rms}$ to be equal to the required DC output voltage, i.e., $V_{rms} = V_{DC} = 12$ V. Also, to prevent transformer heating, the transformer secondary current rating should be larger than the maximum load current by at least a factor of 1.5, i.e., $I_{rms}(s) = 1.5I_{DC}(max) = 1.5$ A. Choose a diode with $I_{AV} \geq I_{DC}(max) = 1$ A and

$$P IV > V_{pk} = 12\sqrt{2} = 16.8 \text{ V.}$$

Capacitor $C$ is given by

$$C = \frac{I_{pc}}{f\Delta V} = \frac{1}{60 \times 2.5} = 6666 \text{ } \mu F.$$  where $f = 60$ Hz. A rough indication of the output voltage under full-load conditions is given by

$$V_{DC} = V_{pk} - \Delta V/2 = 16.8 - 2.5/2 \approx 16.$$

1.5.5 Full-Wave Rectifier

In a full-wave rectifier, both half-cycles of the input waveform are used to produce a unidirectional load current. The basic circuit is shown in Fig. 1.50 and can be viewed as two half-wave rectifiers connected in parallel across the load. It utilizes a center-tapped transformer having equal voltages $V_S$ with diodes $D_1$ and $D_2$ connected to the load as shown. During the half-cycle of the input waveform where point A is made positive with respect to G and point B is made negative with respect to G, diode $D_1$ conducts, while $D_2$ is reverse biased. As a result, current flows through A and $D_1$ from the transformer winding into the load resulting in the polarity across the load as shown (Fig. 1.50).
Similarly, when the input signal is such that point B is positive with respect to G and point A is negative relative to G, diode $D_2$ is now forward biased, while $D_1$ is reverse biased. Therefore, in the load, the current flows through B and $D_2$ in the same direction as before. The waveform of the output voltage is shown in Fig. 1.51. During the conduction of either diode, the full transformer voltage is applied across the other, and therefore, the PIV is again $2\sqrt{2}V_S$. 

*Fig. 1.50* Full-wave rectifier using a center-tapped transformer
The peak load voltage is $\sqrt{2} V_s$. The inclusion of a reservoir capacitor as shown in Fig. 1.52 reduces the ripple as shown in Fig. 1.53. It functions in the same way as in the half-wave rectifier. However, since two half-wave rectifiers operating over alternate half-cycles are involved, the capacitor is recharged twice per input cycle instead of one. The result is that this circuit has fewer ripples than the half-wave rectifier. It, however, requires a center-tapped transformer and two diodes for its implementation. For a full-wave rectifier, the period $T_F \approx \Delta t$ of the rectified waveform is half that of the half-wave rectifier, and therefore, $T_F = 1/2 f$. Hence for the full-wave rectifier, the peak-to-peak output ripple is given by

$$\Delta V = \frac{I_{DC} \Delta t}{C} = \frac{I_{DC} T_F}{C} = \frac{I_{DC}}{2fC}$$  \hspace{1cm} (1.11)
Example 1.11  Design a full-wave unregulated power supply delivering 15 V DC at 1 A with less than 1.5 V peak-to-peak ripple. Use a center-tapped transformer.
Solution  Since the peak transformer voltage is greater than the root mean square value by a factor of 1.414, it is reasonable to choose the transformer voltage $V_{rms}$ to be equal to the required DC output voltage, i.e., $V_{rms} = V_{DC} = 15$ V. Also, to prevent transformer heating, the transformer secondary current rating should be larger than the maximum load current by at least a factor of 1.5, i.e., $I_{rms} (sec) = 1.5I_{DC} (max) = 1.5 \times 1$ A. Choose a diode with $I_{AV} \geq I_{DC} (max) = 1$ A and 

$PIV > V_{pk} = 15 \sqrt{2} = 21.2$ V. Capacitor $C$ is given by 

$$C = \frac{I_{DC}}{2fAV} = \frac{1}{2 \times 60 \times 1.5} = 5555 \ \mu F.$$ 

A rough indication of the output voltage under full-load conditions is given by 

$$V_{DC} = V_{pk} - \Delta V/2 = 16.8 - 2.5/2 \approx 16.$$ 

### 1.5.6 Bridge Rectifier

Full-wave rectification can be accomplished by an alternative circuit called a bridge rectifier shown in Fig. 1.54. The bridge rectifier circuit uses four diodes in a bridge arrangement that obviates the need for a center-tapped transformer. During those half-cycles of the input that make point A positive with respect to point B, diodes $D_2$ and $D_4$ conduct, while $D_1$ and $D_3$ are nonconducting. Current, therefore, flows from point A to point B via $D_2$, the load and $D_4$. When A is negative relative to B, $D_1$ and $D_3$ conduct, and $D_2$ and $D_4$ do not conduct. Current then flows from point B to point A via $D_3$, the load and $D_1$. The resulting current flows in the same direction through the load resulting in a fluctuating, unidirectional voltage across the load with a peak value $\sqrt{2}V_S$. This variation can again be reduced by the inclusion of a filter capacitor across the load. The output voltage waveform is essentially the same as in the previous full-wave rectifier. However, the PIV of each diode is only $V_S$ and no center-tapped transformer is required. Figure 1.55 shows the bridge rectifier with a filter capacitor.
Both the half-wave and full-wave rectifiers discussed above produce unregulated outputs when capacitive filtering is employed. An unregulated DC output suffers from several disadvantages including ripple and variation of output voltage with load current and supply voltage. The reverse bias characteristic of the Zener diode can be used to realize a regulated DC voltage output for use in low-power applications. The basic system consists of the Zener diode $D$ being supplied current through a resistor $R$ from a supply voltage $V_i$ as shown in Fig. 1.56. The system develops a regulated voltage $V_{DC}$ equal to the Zener voltage across the connected load. It functions as follows: The Zener diode $D$ is operated in reverse bias mode with the resistor $R$ providing the necessary bias current from the supply $V_i$. The breakdown voltage $V_Z$ of the Zener appears across its terminals, the rest of $V_i$ being dropped across $R$. In the breakdown region, the diode characteristic has a very steep slope such that large changes in current...
through the Zener are accompanied by only small changes in the voltage across the Zener.

\[ V_{Z} \]

**Fig. 1.56** Zener diode regulator

Thus, when a load is connected, the Zener voltage \( V_{Z} \) appears across the load, and the current is diverted from the Zener into the load. Because of the steep diode characteristic, no change in \( V_{Z} \) accompanies this change in current through the Zener. Similarly, a reduction of current into the load forces an increased current into the Zener with no change in the Zener voltage. The maximum current that can be delivered by the supply is set by the minimum current \( I_{Zmn} \) that must be maintained through the Zener for it to maintain its terminal voltage. If the supply voltage changes, the current through the Zener again changes while still maintaining its terminal voltage.

### 1.5.7.1 Fixed Supply Voltage and Variable Load

Consider the situation in Fig. 1.56 in which the supply voltage \( V_i \) is fixed and the load current \( I_L \) varies. The current \( I_i \) flowing through \( R \) supplies both \( I_Z \) into the Zener and \( I_L \) into the load. Should the load current fall to zero, the current through the Zener will increase by \( I_L \) to \( I_{Zmx} \), and therefore, the Zener must be able to dissipate the associated energy. Hence the maximum Zener current is set by

\[
P_D \geq V_Z I_{Zmx}
\]

where \( P_D \) is the power rating of the Zener. This yields a value of \( R \) given by
The maximum load current $I_{Lmx}$ is set by the minimum Zener current $I_{Zmn}$ below which the Zener voltage begins to fall and is given by

$$I_{Lmx} = I_{Zmx} - I_{Zmn}$$  \hfill (1.14)

**Example 1.12** A voltage regulator is being designed using a 6.3V Zener diode that has a minimum current requirement of 5 mA and $\frac{1}{2}$ Watt power rating. The system shown in Fig. 1.57 will be powered from a 22-V supply, and the load is variable. Calculate the required series resistance and the maximum current available from the regulator.

![Circuit for Example 1.12](image)

**Solution** Using Eq. (1.12), the maximum current that can be passed by the Zener is given by $P_D = V_Z I_{Zmx}$. This gives

$$I_{Zmx} = \frac{P_D}{V_Z} = \frac{0.5}{6.3} = 79.4 \text{ mA}.$$  From Eq. (1.13), $R = \frac{22 - 6.3}{79.4 \text{ mA}} = 198 \text{ Ω}$. 

Therefore, the maximum available load current is from Eq. (1.14) given by $I_{Lmx} = I_{Zmx} - I_{Zmn} = 79.4 - 5 = 74.4 \text{ mA}$. In practice, the need for a safety margin will require $R$ to be greater than 198 Ω such that the power dissipated in the Zener is substantially less than the rated value. This will of course result in the maximum load current being less than 74.4 mA.
Example 1.13  A 5V Zener diode with a minimum current requirement of 10 mA is to be used in a voltage regulator. The supply voltage is 18 V, and the variable load current has a maximum value of 25 mA. Calculate the minimum power rating of the Zener diode, the required series resistance and the minimum load resistance that can be connected to the regulator.

Solution  Since the load current is variable, the Zener must be able to accommodate the maximum load current (should the load resistor be removed) along with the minimum Zener current. This gives a maximum Zener current of \( I_{Zmx} = I_{Lmx} + I_{Zmn} = 25 + 10 = 35 \) mA. Hence the minimum power rating \( P_{Dmn} \) of the Zener is

\[
P_{Dmn} = V_Z I_{Zmx} = 5 V \times 35 mA = 175 \text{ mW.}
\]

The series resistor is given by

\[
R = \frac{18 - 5}{35 \text{ mA}} = 371 \Omega.
\]

Finally, the minimum load resistor that can be connected to the regulator is given by

\[
R_{Lmn} = \frac{5}{I_{Lmx}} = \frac{5}{25} = 200 \Omega.
\]

1.5.7.2  Variable Supply Voltage and Fixed Load

We now consider the case involving a fixed load and a variable supply voltage. In this situation, the varying input voltage causes a corresponding variation in the current through the associated resistor and the Zener diode. Note that since \( V_Z \) is constant, the load current does not experience any change. When the input voltage falls, the current through the Zener also falls but must not be allowed to fall below the minimum Zener current that enables it to function on the steep part of the slope of the breakdown characteristic, and thereby maintain a constant voltage. This means that \( R \) must be selected such that the minimum (or greater) Zener current \( I_{Zmn} \) and the load current \( I_L \) flow with the input voltage at its minimum \( V_{imn} \). Thus

\[
R = \frac{V_{imn} - V_Z}{I_{Zmn} + I_L}
\]

(1.15)

When the supply voltage is at its maximum, the Zener current will also be at its maximum, and therefore, the Zener power rating must exceed the maximum dissipation that will occur, i.e.,
\[ P_D \geq V_Z I_{Z\text{max}} \]  \hfill (1.16)

**Example 1.14**  A 5V Zener diode has a minimum current requirement of 5 mA and is to be used in a voltage regulator. The supply voltage is 25 V ± 10%, and the fixed load current is 20 mA. Calculate the series resistance required, the minimum power rating of the Zener diode and the minimum instantaneous power dissipated in the Zener.

**Solution**  The minimum value of the input voltage is \( V_i = 22.5 \text{ V} \). Therefore, Eq. (1.15) gives

\[ R = \frac{V_{\text{imn}}-V_Z}{I_{Z\text{mn}}+I_L} = \frac{22.5-5}{5+20} = \frac{17.5}{25} = 0.7 \text{ mA} = 700 \Omega. \]

The maximum value of the input voltage is \( V_i = 27.5 \text{ V} \). This produces the maximum current \( I_{R\text{mx}} \) through the series resistor given by

\[ I_{R\text{mx}} = \frac{27.5-5}{700} = \frac{22.5}{700} = 0.032 \text{ mA}. \]

Since 20 mA flows into the fixed load, the maximum Zener current corresponding to the maximum input voltage is \( I_{Z\text{mx}} = 32 - 20 = 12 \text{ mA} \). The minimum power rating of the Zener is then \( P_{D\text{mn}} = V_Z I_{Z\text{mx}} = 5 \times 12 = 60 \text{ mW} \). The minimum instantaneous power dissipated in the Zener occurs when the input voltage is at its minimum. This corresponds to the minimum Zener current flow \( I_{Z\text{mn}} = 5 \text{ mA} \). Hence, the minimum instantaneous power dissipated in the Zener is \( V_Z I_{Z\text{mn}} = 5 \times 5 = 25 \text{ mW} \).

**1.5.7.3 Variable Supply Voltage and Load**

For the situation in which there is varying load and varying supply voltage, the current \( I_i \) flowing through \( R \) supplies both \( I_Z \geq I_{Z\text{mn}} \) into the Zener and \( I_L \) into the load. In the event, the load current falls to zero, all of \( I_L \) will flow through the Zener whose current will increase. Since the input voltage is variable, this will cause a corresponding variation in the current through the associated resistor, and hence the Zener diode. When the input voltage falls, the current through the Zener also falls but must not be allowed to fall below \( I_{Z\text{mn}} \). This means that \( R \) must be selected such that the minimum Zener current \( I_{Z\text{mn}} \) and the load current \( I_L \) flow with the input voltage at its minimum \( V_{\text{imn}} \). Thus
When the supply voltage rises to its maximum, the Zener current will also be at its maximum $I_{Z_{mx}}$, and therefore, the Zener power rating must exceed the maximum dissipation that will occur, i.e.,

$$P_D \geq V_Z I_{Z_{mx}}$$  \hspace{1cm} (1.18)

This is discussed in the example that follows.

**Example 1.15**  Design a Zener diode regulator to provide a maximum current of 10 mA at 9V using a half-wave unregulated supply. This system is to be used to replace the 9V battery used to power many small systems.

**Solution** The system configuration for the regulated supply is shown in Fig. 1.58. A transformer is used to drive a rectifying diode $D_1$ and a filter capacitor $C_1$. These components constitute an unregulated supply. The output then drives resistor $R_1$ which supplies the Zener diode $D_2$. In order to deliver 9 V, this Zener voltage must be 9 V. Capacitor $C_2$ provides extra filtering to remove high-frequency noise. In order to provide a sufficiently high supply voltage to ensure that the Zener diode is properly reverse biased, a 12-V transformer is used. A current rating of 100 mA is more than adequate to deliver the load and the Zener currents. The peak voltage on capacitor $C_1$ after rectification by $D_1$ is $12 \sqrt{2} - 0.7 = 16.3$ V. Hence, the minimum PIV rating of diode $D_1$ is $2 \times 16.3 = 32.6$ V. A diode with a PIV rating of 100 V is a good choice. With a load current of 10 mA and allowing for a Zener current of 10 mA, the value of capacitor $C_1$ required to produce no more than a 1 V change in the voltage across this capacitor is $C = I / \Delta V_f = 20 \times 10^{-3} / 60 = 333 \mu F$. A value of 500 $\mu F$ is chosen with a working voltage of 50 V to ensure safe operation. Here, $f = 60$ Hz is the frequency of the mains supply. The minimum voltage across $C_1$ is $16.3 - 1 = 15.3$ V. Allowing for transformer resistance, we use 15 V. Since resistor $R_1$ must allow a total of 20 mA to flow, its value is given by

$$R = \frac{V_{in} - V_Z}{I_{Z_{mn}} + I_L}$$  \hspace{1cm} (1.17)
\( R_1 = (15 - 9)/20 \text{ mA} = 300 \Omega \). The maximum input voltage is 
\[
12 \sqrt{2} - 0.7 = 16.3 \text{ V}.
\]
Hence the maximum current through the Zener is 
\[
(16.3 - 9)/300 \Omega = 24.3 \text{ mA}.
\]
Hence the maximum power dissipation in the Zener is 
\[
9 \text{ V} \times 24.3 \text{ mA} = 218.7 \text{ mW}.
\]
A 500-mW Zener will provide a good safety margin. This circuit is inherently short-circuit protected because of \( R_1 \). Thus, in the event of a short circuit at the output, the full voltage of capacitor \( C_1 \) will be applied across \( R_1 \) which will now be in parallel with \( C_1 \). Under this condition, the maximum current through this resistor will be 
\[
16.3 \text{ V}/300 \Omega = 54.3 \text{ mA}.
\]
The maximum power that will be dissipated in this resistor is, therefore, 
\[
16.3 \text{ V} \times 54.3 \text{ mA} = 886 \text{ mW}.
\]
A 2 W resistor for \( R_1 \) will provide an adequate safety margin. The LED \( D_3 \) will indicate when the system is on and together with \( R_2 \) will discharge capacitor \( C_1 \) when the system is off. Using a green LED for \( D_3 \) and a LED current of 10 mA, resistor 
\[
R_2 = (15 - 2.1)/10 \text{ mA} = 1.3 \text{ k}.
\]
Finally, capacitor \( C_2 \) is used to remove high-frequency noise from the supply output, and a value of 0.1 \( \mu \text{F} \) will have a low reactance at frequencies of 10 kHz and above.

---

**Fig. 1.58** Zener diode regulator

### 1.6 Applications

The circuits below are some simple applications of diodes in real-world systems that can be easily designed and implemented.

#### 1.6.1 1.3V Supply from 5V
The circuit shown in Fig. 1.59 operates in a manner similar to a Zener diode regulator. It provides 1.3 V from the widely available 5-V supply as a replacement for small low-voltage cells. The resistor $R_1$ limits the current in the green LED $D_1$ to a few milliamps of say 10 mA which results in a diode voltage of about 2 V across $D_1$. This gives $R_1 = (5 - 2)/10 \text{ mA} = 300 \, \Omega$. In order to reduce this 2 V to the desired 1.3 V, a signal diode $D_2$ such as the 1N4148 is included in the circuit as shown. A small capacitor $C_1 = 10 \, \mu\text{F}$ is placed at the output in order to provide some basic filtering for noise signals above about 1 kHz. At this frequency, the reactance of the capacitor is given by $\frac{1}{2\pi f C} = \frac{1}{2\pi} \times 10^3 \times 10 \times 10^{-6} = 16 \, \Omega$ which short-circuits signals above this frequency.

1.6.2 9V Supply from 12V

There are many portable devices that require 9 V for their operation. The circuit in Fig. 1.60 converts the 12V available from the cigarette lighter in an automobile to 9V. Each of the four silicon diodes $D_1$ to $D_4$ drops 0.7V resulting in an output of just over 9V.
Ideas for Exploration: (i) Modify the circuit in order to reduce the output of a 9V battery to 5V.

1.6.3 Battery Charger

A 12V battery charger circuit is shown in Fig. 1.61. The circuit involves a 24V center-tapped 5A transformer operating into a full-wave rectifier whose output is filtered by a 2000μF capacitor C. The final circuit output is delivered to the battery under charge through a series 10Ω variable power resistor $VR_1$ and an ammeter. At the start of charging, the variable resistor is adjusted in order to limit the charge current to about 2 A. The peak capacitor voltage is $12\sqrt{2} = 17$ V, and the peak voltage change is $\Delta V = I/2Cf = 2/2 \times 2000 \times 10^{-6} \times 60 = 8.3$ V. Hence the average output voltage is $17 - (8.3/2) = 12.8$ V. Therefore, as the battery is charged, the current decreases and should drop to almost zero when the battery is fully charged.
Ideas for Exploration: (i) Introduce reverse polarity protection to prevent incorrect battery connection by including a diode with suitable current rating in series with the positive output of the charger: positive output to anode and output at cathode to positive terminal of battery.

1.6.4 Polarity Indicator
The circuit in Fig. 1.62 is a polarity indicator. The resistor $R_1$ is chosen to limit the current in the diodes to a few milliamperes. The green LED lights when terminal 1 is at a positive potential relative to terminal 2. The red LED lights when the reverse is true. Diodes $D_1$ and $D_2$ ensure that the LEDs are protected from reverse voltage. A resistor value of $R_1 = 1 \text{kO}$ would allow the testing of voltages between 1 and approximately 15. The value would need to be increased to test the polarity of higher voltages.

1.6.5 Light Meter
BPW34 is an example of a photodiode from Vishay Semiconductors. It is a high-speed device with high sensitivity in a miniature flat plastic package. Because of its water-clear epoxy construction, this diode is sensitive to radiation from the visible and the infrared regions of the electromagnetic spectrum. Using this device, a simple light meter is shown in Fig. 1.63. As light falls on the diode, the increase in current flows through the resistor, thereby resulting in a voltage drop across it.
For the 10 k resistor, the relationship between the light intensity (lumens per square meter or lux) and voltage output is given by \( \text{lux} = 1333 \ V_o \). For example, a voltage from 0 to 0.75 V will correspond to light intensity of 0–1000 lux. Hence, the voltmeter \( V \) connected across the resistor can be calibrated to read light intensity.

**Fig. 1.63** Simple light meter

*Ideas for Exploration*: (i) Use a simple analog multimeter as the voltmeter and calibrate the scale to read light intensity in units of lux.

### 1.6.6 Blown Fuse Indicator

The circuit in Fig. 1.64 indicates when a fuse is blown. During normal operation, the green LED is on, and the voltage across this device is insufficient to turn on the red LED in series with a normal signal diode.
Therefore, the red LED remains off. The current through the green LED is limited by resistor $R_1$ which can be of the order of kilo-ohms depending on the supply voltage. For example, for a current of 10 mA, an input voltage of 12 V will require $R_1 = (12 - 2)/10 \text{ mA} = 1 \text{ k}$. Here, we have used an approximate LED voltage of 2 V. A blown fuse disconnects the supply from the load and the green LED which goes off. This results in the full supply voltage being applied across the red LED in series with the signal diode, thereby causing this LED to turn on.

![Blown fuse indicator](image)

**Fig. 1.64** Blown fuse indicator

### 1.6.7 Diode Tester

This circuit, shown in Fig. 1.65, enables the polarity of unmarked semiconductor diodes to be determined. It is powered by a low-voltage transformer $T_1$. Resistor $R_1$ limits the current flowing through the diodes. When the diode under test is connected with the anode at A and the cathode at B, it will allow current to flow from A to B and through
diodes $D_1$ and $D_2$ causing the green LED $D_1$ to light. If the test diode is connected in the reverse, then current will flow from terminal B to A and through diodes $D_3$ and $D_4$ causing the red LED $D_4$ to light. A short circuit exists if both LEDs light and an open circuit exists if neither LED lights. With a 12-V transformer, allowing about 10 mA, then the resistor $R_1$ can be found using $R_1 = (12 - 0.7 - 0.7 - 2)/10$ mA = 860 Ω.

![Diode tester diagram](image)

**Fig. 1.65** Diode tester

*Ideas for Exploration:* (i) Re-design the system for portable operation by replacing the transformer with a 9V battery and re-calculating $R_1$.

### 1.6.8 Emergency Phone-Line Light

This circuit, shown in Fig. 1.66, will provide light in a power outage situation. It utilizes the 48 V DC available on a telephone line when on hook. It comprises 10 white LEDs $D_1$ to $D_{10}$ connected in series with a current limiting resistor $R_1$ and a diode $D_{11}$ to protect the LEDs from reverse voltage when the circuit is connected to the telephone tip (+ve) and ring (−ve). Since each LED has an on voltage of about 3.3 V, then noting that $D_{11}$ has a voltage drop of 0.7 V, the voltage drop across $R_1$ is $(48 - 0.7 - (10 \times 3.3)) = 14.3$ V. The central office of the telephone system will detect currents on the telephone line in the range 6–25 mA.
as indicating a telephone off-hook condition. Therefore, resistor $R_1$ must be chosen such that the current drawn from the telephone line is less than 5 mA. Using $4 \text{ mA}$, then $R_1 = \frac{14.3}{4} \text{ mA} = 3.6 \text{ k}$. 

**Fig. 1.66** Emergency telephone line light

### 1.6.9 Phone Alert

The circuit in Fig. 1.67 is designed to indicate when the telephone is in use. It is made up of a diode bridge $D_1$ to $D_4$ that ensures unidirectional current flow through the LED $D_5$. The circuit is connected between the telephone line terminals and the telephone instrument. When the telephone is on hook, the phone line is open. Hence, no current flows and the LED is off. When the telephone goes off-hook, the telephone line is looped. As a result, current flows through the LED which lights, thereby indicating the off-hook condition. The telephone line resistance which is about $1 \text{ k}$ limits the current.
1.6.10 Lead-Acid Battery Monitor

The circuit in Fig. 1.68 enables the monitoring of the voltage of a lead-acid battery under charge. Diode $D_1$ ensures that the battery is connected with the correct polarity in which case the red LED $D_2$ will light. Resistor $R_2$ limits the current into this LED. A value of 1 k will limit the current to about 12 mA. In the discharge state, the battery voltage will not be sufficient to enable conduction of the diode string comprising the green LED $D_3$ (1.8 V), the Zener diode $D_4$ (12 V) and diode $D_5$ (0.7 V), and hence the green LED will be off. As the battery voltage rises above about 13.5 V, conduction in the diode string will begin, and the green LED will also start to glow. Resistor $R_1$ limits this current. Since most of the battery voltage will be dropped across the diodes in the diode string, a value of 100 Ω for $R_1$ is sufficient as only the voltage above the diode voltages will be dropped across $R_1$. 

*Fig. 1.67* Phone indicator
Ideas for Exploration: (i) Use this circuit to monitor the output voltage of the battery charger circuit discussed earlier.

1.6.11 Zener Diode Regulator Using a Voltage Doubler

The circuit in Fig. 1.69 is that of Zener diode voltage regulator that produces 12V DC at 25 mA from a 6V transformer. It operates using two half-wave rectifiers whose outputs are connected in series. Thus, during the half-cycle in which the transformer terminal A is positive with respect to transformer terminal B, diode $D_1$ turns on and charges capacitor $C_1$ to $6\sqrt{2} = 8.5$ V with the polarity shown. During this
time, diode $D_2$ is reverse biased, and therefore, off. During the half-cycle when terminal A is negative with respect to terminal B, diode $D_2$ turns on charging capacitor $C_2$ to $\frac{6\sqrt{2}}{\pi} \approx 8.5$ V. Diode $D_1$ turns off during this time. The result is that the voltage across terminals C and D is $2 \times \frac{6\sqrt{2}}{\pi} \approx 17$ V. For a supply current of 25 mA, allowing a minimum Zener current of 5 mA, then the total Zener current must be 30 mA. For 30 mA into the 12 V Zener $D_3$, allowing a 1 V voltage drop on each capacitor, each capacitor must be $C = \frac{I}{f \Delta V} = \frac{30 \text{ mA}}{60 \times 1} = 500 \mu\text{F}$. With this 1 V voltage drop on each capacitor, the value of $R_1$ that allows the flow of 30 mA into the 12V Zener diode $D_3$ is given by $R_1 = \frac{(17 - 1 - 1 - 12)}{30 \text{ mA}} = 100 \Omega$. The maximum current into the Zener is $(17 - 12)/100 = 50$ mA, and therefore, the maximum power dissipated in the Zener diode is $P_D = 12 \times 50 \text{ mA} = 600 \text{ mW}$. Hence a 1W Zener is chosen for safe operation.

![Fig. 1.69 Zener diode regulator using voltage doubler](image)

**Ideas for Exploration:** (i) Implement an LED “ON” indicator at the output of the system using an LED and a series resistor. (ii) Re-design the system to deliver 9V at the output by changing $D_3$ and $R_1$. 
1.6.12 Regulated Supply Using the TL431A

The TL431A integrated circuit \( (D_2) \) is a three-terminal device that functions as a programmable Zener diode whose effective voltage \( V_Z \) can be varied from 2.5 to 36 V using two external resistors \( R_1 \) and \( R_2 \) as shown in Fig. 1.70. The Zener voltage is given by

\[
V_Z = \left(1 + \frac{R_1}{R_2}\right) V_{ref}
\]

where \( V_{ref} = 2.5 \) V. The Zener current range is 1–100 mA, and the typical dynamic resistance is 0.22 Ω. The temperature coefficient is a low 0.4%/°C at room temperature. Figure 1.70 shows the application of the device in a regulated power supply delivering 20 V at a current of 50 mA. A 24-volt transformer is used to ensure adequate voltage drop across the resistor \( R_3 \). Using a current of 55 mA into the Zener and allowing for a 2-volt drop in the voltage across the reservoir capacitor \( C_1 \), the capacitor value is given by \( C_1 = 55 \text{ mA} / (2 \times 60) = 458 \mu\text{F} \). A value of 500 μF is used. The minimum value of the input voltage is

\[
24 \sqrt{2} - 2 = 32 \text{ V}
\]

Hence \( R_3 = (32 - 20) / 55 \text{ mA} = 218 \Omega \). For a 20-volt output, \( 20 = (1 + R_1 / R_2) \times 2.5 \). Using \( R_2 = 2 \text{ k} \), then \( R_1 = 14 \text{ k} \). Capacitor \( C_2 = 1 \mu\text{F} \) removes any high-frequency noise and residual ripple.

![Fig. 1.70 Regulated supply using TL431A](image)
Ideas for Exploration: (i) Redesign the circuit to allow for a higher Zener current. This enables the system to supply more current to an external load.

1.6.13 Research Project 1

This research project involves the use of a germanium diode in the design and implementation of a simple radio receiver for the reception of amplitude-modulated (AM) broadcasts in the medium wave band (540–1600 kHz). The basic circuit is shown in Fig. 1.71. It comprises a coil (inductor) $L_1$ and variable capacitor $VC_1$ connected in parallel to form a tuning circuit. One end of the coil is connected to an antenna, while the other end is grounded to an external earth. The output of the parallel LC or tank circuit goes to diode $D_1$ that is a germanium diode. This semiconductor device has a turn-on voltage of 0.3 V that is much lower than the 0.7 V of a silicon diode. The diode output is connected to a high impedance piezoelectric earphone.

![Crystal radio circuit diagram](image)

Fig. 1.71 Crystal radio

The system works in the following manner: An amplitude-modulated radio-frequency broadcast signal is an electromagnetic wave (carrier) whose frequency is in the radio-frequency band and whose amplitude is modulated by a superimposed audio frequency signal. The passage of such a wave induces an electrical signal in the antenna that flows into the inductor–capacitor tank circuit to the
ground. For a signal whose frequency is at the resonant frequency 
\[ f = \frac{1}{2\pi \sqrt{LC}} \]
of the LC circuit, there is resonance such that a large potential difference develops across the tank circuit. This signal is rectified by the germanium diode, and the carrier component of the signal is filtered out by the capacitor associated with the piezoelectric earphones. The remaining signal is the original audio component, which drives the high-impedance earphones.

The coil and the variable capacitor must enable changing the resonant frequency across the full medium wave band. A 365-pF variable capacitor and a 300-μH inductor are suitable. The coil can be constructed using a ferrite rod with 100 turns of no 26SWG (25AWG) enameled copper wire. The germanium diode 1N34A is suitable for the detection stage as its turn-on voltage is only 0.3 V. The piezoelectric earphones convert the electrical signal to sound, and its high impedance ensures that frequency selectivity is not reduced. The resistor \( R_1 \approx 10 \text{k} \) to 47 k provides a DC path for the proper operation of the diode. For effective operation, the antenna should be about 30 m long, about 7 m above ground and insulated from its supports.

The circuit must also have a good ground to the physical Earth using a solid copper rod driven into the ground. The circuit should be able to receive nearby AM stations, with difficulty being experienced with more distant ones.

*Ideas for Exploration:* (i) Wind the antenna into a coil of wire and see how that affects reception. (ii) Replace the ferrite rod by a 1 inch former, thereby realizing an air-cored inductor. (iii) Experiment with coils with a reduced number of turns to attempt short wave reception (1.7–30 MHz).

**1.6.14 Research Project 2**

This research project is a design based on the circuit shown in Fig. 1.72. It comprises an 8V low-voltage transformer that drives a network of capacitors and diodes. Treating terminal G as ground, as terminal A goes negative, diode \( D_1 \) turns on and charges capacitor \( C_1 \) to \( 8 \sqrt{2V} \) with the polarity shown. When terminal A goes positive, diode \( D_1 \) turns off
and diode $D_2$ turns on. The transformer voltage is then in series with the voltage across capacitor $C_1$ giving a total voltage of $\frac{16 \sqrt{2}}{}$.

Capacitor $C_2$ is charged to this voltage via diode $D_2$ giving an output voltage of $+\frac{16 \sqrt{2}}{}$ at terminal 1. Similarly on the positive half-cycle of the transformer secondary, capacitor $C_3$ charges up to $\frac{8 \sqrt{2}}{}$ via diode $D_3$ with the polarity shown. On the negative half-cycle, this voltage is in series with the transformer voltage thereby charging capacitor $C_4$ to $\frac{16 \sqrt{2}}{}$ via diode $D_4$. The result is a voltage $+\frac{16 \sqrt{2}}{}$ at terminal 2. This circuit, therefore, provides bipolar outputs $+\frac{16 \sqrt{2}}{}$, each of which is double the transformer voltage. This kind of circuit is necessary to provide power to several devices requiring bipolar supply such as operational amplifiers. The current capacity of the circuit depends on the size of the capacitors which should all be equal.
Fig. 1.72  Bipolar power supply

_Ideas for Exploration:_ (i) Try different transformer output voltages and measure the voltages at the two terminals with respect to ground; (ii) Use the circuit as a voltage quadrupler by using the voltage across terminals 1 and 2 which is approximately four times the transformer output voltage.

_Problems_

1. Briefly explain the following:

   (i) The formation of n-type and p-type material.

   (ii) Increased conductivity in n-type and p-type material.

   (iii) Why there is conduction across a forward-biased p–n junction.

   (iv) Why there is little or no conduction across a reverse-
biased p–n junction.

(v) What happens when n-type and p-type material are brought into contact.

(vi) The effect of temperature on the conductivity of intrinsic semiconductor material.

(vii) Why a conductor conducts better than a semiconductor.

(viii) Why a semiconductor conducts better than an insulator.

(ix) The cause of the barrier potential in an n–p junction.

2. Determine the dynamic resistance of a semiconductor diode for 0.5 mA current through the diode.

3. A Zener diode has $V_Z = 6.8\ V$ at 25 °C. If the diode has $T_C = 0.03\%/°C$, determine the Zener voltage at 63 °C.

4. An 10V Zener has a power rating of 400 mW. Determine the maximum reverse current $I_{Zmx}$.

5. An LED is driven by a 9V battery in series with a resistor $R_1$. Determine the value of $R_1$ if the LED is green.

6. In the circuit of problem 5, if the LED is replaced by a silicon diode, what is the value of the current for the same value of $R_1$?

7. Sketch the output waveform for each of the circuits shown in Fig. 1.73. In each case, $V_i$ is a symmetrical square wave input signal of amplitude ±10 V.

8. For the circuits in problem 7, sketch the output waveform for a sine wave input signal of amplitude ±15 V.
9. Sketch the following circuits:
   (i) Full-wave rectifier using a center-tapped transformer.
   (ii) Full-wave bridge rectifier operating into a load.
   (iii) Clipping circuit using one Zener diode.
   (iv) Clamping circuit with a peak positive output of +0.7 V.

10. Sketch the output waveform for each of the circuits shown in Fig. 1.74. In each case, the input is a symmetrical square wave input signal of amplitude ±12 V.

11. With the aid of a circuit diagram, explain the operation of a half-wave rectifier operating into a resistive load. Draw a voltage/time diagram of the output waveform. Explain the effect of a filter capacitor being placed across the load.

12. With the aid of a circuit diagram, explain the operation of a full-wave rectifier operating into a resistive load. Draw a voltage/time diagram of the output waveform. Explain the effect of a filter capacitor being placed across the load.

13. Compare the advantages and disadvantages of using a bridge rectifier with a normal transformer or two diodes and a center-tapped transformer to realize a full-wave rectifier.

14. Design a half-wave unregulated power supply delivering 15V DC at 0.5A with less than 2V peak-to-peak ripple.

15. Using a center-tapped transformer, design a full-wave unregulated power supply delivering 12V DC at 2A with less than 1V peak-to-peak ripple.

16. Re-design the circuit in problem 16 using a 15V transformer and a bridge rectifier.
   A 6V Zener diode with a minimum current requirement of 5 mA is
17. A 5V Zener diode with a minimum current requirement of 5 mA is to be used in a voltage regulator. The supply voltage is 22 V and the variable load current has a maximum value of 15 mA. Calculate the required series resistance and the minimum power rating of the Zener diode.

18. A 16V Zener diode with a minimum current requirement of 5 mA and a power rating of 800 mW is to be used in a voltage regulator. The supply voltage is 24V and the load current is variable. Calculate the required series resistance and the minimum load resistor that can be connected to the supply.

19. A 5V Zener diode has a minimum current requirement of 10 mA and is to be used in a voltage regulator. The supply voltage is 20V ± 10% and the fixed load current is 20 mA. Calculate the series resistance required, the minimum power rating of the Zener diode and the minimum instantaneous power dissipated in the Zener.

20. A 12V Zener diode has a minimum current requirement of 6 mA and is to be used in a voltage regulator. The supply voltage is 30V ± 5% and the fixed load current is 15mA. Calculate the series resistance required and the maximum instantaneous power dissipated in the Zener diode.

21. A 12V Zener diode with a minimum current requirement of 4mA and a power rating of 600 mW is to be used in a voltage regulator. The supply voltage is 20V and the load current is variable. Calculate the required series resistance and explain what occurs if the supply is short circuited.

22. A 9V Zener diode has a minimum current requirement of 3 mA and is to be used in a voltage regulator. The supply voltage is 24V ± 5% and the variable load current has a maximum value of 18mA. Calculate the series resistance required and the minimum power rating of the Zener diode.
23. A 6V Zener diode with a 1W power rating has a minimum current requirement of 5mA and is to be used in a voltage regulator. The supply voltage is 18V ± 5% and the load current is variable. Calculate the series resistance required and the maximum current that can be delivered by the supply.

24. Design a Zener regulated power supply to deliver 12V at a current of 25mA using an 18V transformer and a bridge rectifier.

25. Using the basic configuration of Fig. 1.60, design a circuit to deliver (i) 3V from a 5V DC supply and (ii) 6V from a 12V DC supply.

26. Determine how to arrange the components in the polarity indicator circuit of Fig. 1.62 if only one LED is available.

27. Using the basic Zener regulator configuration and a BZX55C2V0 2V Zener, design a circuit that supplies 1.3V from a 5V supply that can replace 1.3V mercury cells. Use an 1N4148 silicon diode to effect the voltage reduction from 2 to 1.3V.

28. The circuit shown in Fig. 1.75 is that of a mains wiring fault detector. Determine the condition of the leds (on/off) for the following fault conditions: (i) live disconnected; (ii) live and neutral interchanged; (iii) ground disconnected; (iv) live and ground interchanged; (v) neutral disconnected; and (vi) all connections good.

29. Resistor $R_1$ and LED $D_1$ in Fig. 1.76 constitute a blown fuse indicator for a power supply. Explain the operation of the arrangement and determine a suitable value for the resistor.

30. Discuss how the circuit shown in Fig. 1.77 can be used for testing fuses in an automobile without their removal and determine a suitable value of $R_1$. 
Fig. 1.73 Circuits for Question 7

Fig. 1.74 Circuits for Question 10
Fig. 1.75  Circuits for Question 28

Fig. 1.76  Circuits for Question 29
**Fig. 1.77** Circuit for Question 30

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**Bibliography**

2. Bipolar Junction Transistor

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The bipolar junction transistor or binary junction transistor (BJT) is a device that is capable of amplifying a voltage or current, something that diodes are not able to do. This amplifying characteristic makes BJT suitable for a wide range of applications. The device was invented in 1947 by Walter H. Brattain, John Bardeen, and William Shockley who were awarded the Nobel Prize in Physics in 1956 for this invention. It revolutionized the electronics industry by enabling the miniaturization of electronic circuits and increased equipment portability. This chapter discusses the characteristics of BJT and its use in elementary amplifier circuits. At the end of it, the student will be able to:

- Explain the basic operation of a BJT.
- Describe the various configurations.
- Describe the operation of a basic BJT amplifier.
- Analyze single-stage transistor amplifiers.
- Design single-stage transistor amplifiers.

2.1 Transistor Construction and Operation
The bipolar junction transistor or binary junction transistor (BJT) is basically a two-diode structure consisting of either p–n–p or n–p–n. The former is called a p-n-p transistor while the latter is called an n-p-n transistor. The n-p-n structure involving n-type, p-type, and n-type material in direct contact is shown in Fig. 2.1a, whereas the p-n-p structure consisting of p-type, n-type, and p-type material in direct contact is shown in Fig. 2.1b. In the n-p-n structure, the n-type material referred to as the emitter region of the transistor is heavily doped, while the base and collector regions are lightly doped. In normal operation as an amplifier, the emitter–base junction is forward-biased by applying a potential $V_{BE}$, and the collector–base junction is reverse-biased by applying a potential $V_{CB}$. For the n-p-n transistor, electrons ($I_E$) are injected from the emitter into the base region because of the forward bias across the base–emitter junction. Most diffuse across the base to the collector where they ($I_C$) are collected by the reverse bias potential across the collector–base junction. A few electrons ($I_B$) flow out to the base connection because of the positive potential there. This process of carriers being generated in the emitter, traversing the base, and being collected by the collector is referred to as transistor action. The p-n-p transistor behaves similarly with holes replacing electrons as the majority carriers. The symbols for n-p-n and p-n-p transistors are shown in Fig. 2.2.

![Fig. 2.1 NPN and PNP transistors. (a) NPN transistor. (b) PNP transistor](image-url)
In the arrangement in Fig. 2.3, $V_{BE}$ forward-biases the base–emitter junction as before, but instead of a voltage $V_{CB}$ directly across the collector–base junction, a voltage $V_{CE}$ is applied across the collector and emitter, thereby referring both potentials to a common reference at the emitter. $V_{CE}$ is chosen sufficiently larger than $V_{BE}$ to ensure that the collector–base junction is reverse-biased. This is called the common emitter (CE) configuration and is fundamental to transistor action. Using conventional current flow, according to Kirchhoff’s current law for current flow:

$$I_E = I_C + I_B$$  \hspace{1cm} (2.1)$$

i.e., the emitter current is the sum of the collector current and the base current. The unique property of the transistor, which makes it useful, is the fact that the collector will collect carriers with an efficiency that is almost independent of the reverse bias collector–base voltage. That means the value of the collector current $I_C$ depends almost entirely on the emitter current from which it is derived which in turn depends on the base–emitter forward bias voltage $V_{BE}$ or the base current $I_B$. This characteristic of the transistor can be used to produce amplifying action in the transistor.
Thus, the inclusion of a resistor $R$ in the collector circuit, as shown in Fig. 2.4, (where power supplies have been relabeled) will not affect the value of the collector current since the collector will still collect carriers with almost the same efficiency. Therefore, a changing base-emitter voltage corresponding to an input signal $V_i$, as shown in Fig. 2.5, will produce a changing collector current. This results in a changing voltage drop across resistor $R$ representing an output voltage signal $V_o$. For a sufficiently large resistor $R$, this output voltage $V_o$ is larger than the input signal voltage $V_i$ producing it, and hence signal amplification occurs. This important action will be discussed in detail in Sect. 2.3.1. Note that the circuit of Fig. 2.5 is not usable in this form. Certain modifications are necessary to make it functional. These will be considered in Sect. 2.3.
Another important property of the transistor is that a large collector current $I_C$ is associated with a small base current $I_B$ according to:

$$I_C = \beta I_B$$

(2.2)
where $\beta$ is the (CE) current gain, typically 100 for low-power transistors. Since most of the majority carriers from the emitter are collected by the collector, the collector current $I_C$ is very nearly equal to the emitter current $I_E$:

$$I_C = \alpha I_E$$

(2.3)

where $\alpha \leq 1$. $\alpha$ is referred to as the common base (CB) current gain. While the collector current $I_C$ comprises mainly majority carriers from the emitter, there is a small component that is made up of minority carriers. This minority carrier component is called \textit{leakage} current $I_{CO}$. Its value is quite small relative to $I_C$ and, like the reverse saturation current $I_O$ for a diode, is temperature sensitive. Its effect can be quite critical in some designs. However, in modern devices, $I_{CO}$ is often sufficiently small that it can be ignored.

2.2 Transistor Configurations

There are three transistor configurations that provide useful amplification. These are the CE, CB, and common collector (CC) configurations. These configurations using NPN transistors are shown in Fig. 2.6 with input voltage $V_i$ and output voltage $V_o$. The CE configuration shown in Fig. 2.6a is, in fact, that considered in Fig. 2.3 while discussing transistor action above. The name CE derives from the fact that the emitter terminal is common to both input and output circuits. The CB configuration shown in Fig. 2.6b is so-called because the base terminal is common to both the input and the output. It corresponds to the circuit in Fig. 2.1 used to introduce transistor operation. The CC configuration shown in Fig. 2.6c has the collector common to both the input and the output through the supply $V_{CC}$, which is a short-circuit for signals.
2.2.1 Common Emitter Configuration

Consider the CE configuration, as shown in Fig. 2.7. The input signal is applied at the base and the output signal is taken at the collector as shown. This configuration can be viewed as fundamental to transistor operation since the other two configurations can be derived from this one using negative feedback. It is the most frequently used configuration.
In the analysis and design of transistor circuits using this configuration, static characteristic curves involving current–voltage plots are available that may be used. These curves give information on the value of current flowing into or out of one terminal in response to current into the base terminal or voltage across the base–emitter terminals. Three sets of characteristics can be plotted:

(i) Input characteristics.

(ii) Mutual and transfer characteristics.

(iii) Output characteristics.
They can be experimentally determined using the circuit, as shown in Fig. 2.8. This circuit comprises a variable DC supply $V_{CC}$ that supplies the collector–emitter circuit and a variable DC supply $V_{BB}$ which supplies the base–emitter circuit. Voltmeter A measures the base–emitter voltage $V_{BE}$, whereas voltmeter B measures the collector–emitter voltage $V_{CE}$. The milliammeter measures the collector current $I_C$, whereas the microammeter measures the base current $I_B$. Each of the three sets of characteristics will now be considered.

![Circuit for the determination of transistor characteristics](image)

**Fig. 2.8** Circuit for the determination of transistor characteristics

### 2.2.1.1 Common Emitter Input Characteristic

The CE input characteristic indicates the manner in which the base current $I_B$ varies with changes in the base–emitter voltage $V_{BE}$, the collector–emitter voltage is held constant. Typical characteristics for various constant values of $V_{CE}$ are shown in Fig. 2.9. The curve has a shape that is similar to that of the diode since like the diode, little or no base current flows below approximately 0.7 V, while above 0.7 V the base current increases sharply. Note also that varying $V_{CE}$ causes only a small variation in the curves suggesting that the input characteristic is
essentially independent of the collector-emitter voltage. The AC input resistance $h_{ie}$ of the transistor for small variations in $V_{BE}$ and $I_B$ can be determined by taking the reciprocal of the slope of the curve at that point with $V_{CE}$ held constant. It is given by

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B} \bigg|_{V_{CE} \text{ constant}}$$

(2.4)

where $\Delta V_{BE}$ and $\Delta I_B$ are small changes in $V_{BE}$ and $I_B$. A parameter of less interest is the DC input resistance $h_{IE}$ given by the ratio $V_{BE}/I_B$ at a point. There may be considerable difference between $h_{ie}$ and $h_{IE}$. $V_{BE}$ and $I_B$ are related by the diode Eq. (1.1) and cannot be simultaneously controlled: one can be set, while the other assumes a value consistent with the diode equation.

Fig. 2.9 Common emitter input characteristics
2.2.1.2 Common Emitter Transfer Characteristic

The transfer characteristic shows the manner in which the collector current $I_C$ varies in response to the base current $I_B$ while keeping the collector–emitter voltage constant. A typical curve is shown in Fig. 2.10. The slope of this characteristic gives the AC gain of the transistor:

$$h_{fe} = \frac{\Delta I_C}{\Delta I_B} \bigg|_{V_{CE} \text{ constant}}$$  \hspace{1cm} (2.5)

where $\Delta I_C$ and $\Delta I_B$ are small changes in $I_C$ and $I_B$. The DC gain $\beta$ considered earlier is given by

$$\beta = h_{FE} = \frac{I_C}{I_B}$$  \hspace{1cm} (2.6)

![Common emitter transfer characteristic](image)

*Fig. 2.10* Common emitter transfer characteristic
Again, the collector–emitter voltage has little or no effect on the CE transfer characteristic; the collector current is determined by the base current (or the base–emitter voltage) and not the collector–emitter voltage. Another interesting point is that this $I_C/I_B$ characteristic is quite linear for a substantial part of the curve and therefore a (large) collector current flowing in response to a (small) base current can be quite linear. This represents (current) amplification with low distortion.

### 2.2.1.3 Common Emitter Mutual Characteristic

The mutual characteristic indicates how the collector current $I_C$ changes in response to changes in the base–emitter voltage $V_{BE}$, the collector–emitter voltage being constant. The gradient of this characteristic is the mutual conductance or transconductance $g_m$ of the transistor given by

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B} \mid_{V_{CE} \text{ constant}}$$

where $\Delta I_C$ and $\Delta V_{BE}$ are small changes in $I_C$ and $V_{BE}$. Typical characteristics for various values of $V_{CE}$ are shown in Fig. 2.11. Once again, $V_{CE}$ has relatively little effect on the curves: $I_C$ is set by $V_{BE}$ (or $I_B$) and not $V_{CE}$. This curve is similar to the input characteristic and is nonlinear. Therefore, the collector current $I_C$ flowing in response to an input signal $V_{BE}$ will experience increasing levels of distortion as the input amplitude increases. Note that $g_m$ can be written as

$$g_m = \frac{\Delta I_C}{\Delta V_{BE}} = \frac{\Delta I_C}{\Delta I_B} \times \frac{\Delta I_B}{\Delta V_{BE}} = \frac{h_{fe}}{h_{ie}}$$
This is a useful relationship that will be referred to later.

### 2.2.1.4 Common Emitter Output Characteristics

The output characteristic illustrates the manner in which collector current $I_C$ changes with collector–emitter voltage $V_{CE}$ for (a) constant values of base current and (b) constant values of base–emitter voltage. The family of curves with base current as the varying parameter is shown in Fig. 2.12. The low value of the slope of these curves is yet another indication of the limited effect of $V_{CE}$ on $I_C$. The slope at the approximately flat portion of these curves represents the output admittance $h_{oe}$ of the transistor and is given by

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}} \bigg|_{I_B \text{constant}}$$

(2.9)
where $\Delta I_C$ and $\Delta V_{CE}$ are small changes in $I_C$ and $V_{CE}$. The output impedance of the transistor in this configuration is the reciprocal of $h_{oe}$. These output characteristics can also be used to determine the (short-circuit or AC) current gain $h_{fe}$ of the transistor, since, for a given value of collector–emitter voltage $V_{CE}$, the change in collector current $\Delta I_C$ and the corresponding change in base current $\Delta I_B$ can be obtained by projection on the curves. The family of curves with base–emitter voltage as the varying parameter is shown in Fig. 2.13.

![Common emitter output characteristics for fixed values of $I_B$](image)

**Fig. 2.12** Common emitter output characteristics for fixed values of $I_B$
Output impedance as well as transconductance can be determined using these curves. The flat portion of the output curves is all asymptotic to straight lines, which intercept the collector–emitter voltage axis at approximately the same point, as shown in Fig. 2.14. The magnitude of the collector–emitter voltage where this interception occurs is called the early voltage $V_A$. 

![Figure 2.13](image-url) Common emitter output characteristics for fixed values of $V_{BE}$
**Fig. 2.14**  Early voltage $V_A$

$V_A$ is typically in the range $50 < V_A < 300$ V. It enables the output resistance of the transistor in this configuration to be determined by

$$\frac{1}{h_{oe}} = \frac{V_A + V_{CEq}}{I_{Cq}}$$

(2.10)

where $V_{CEq}$ and $I_{Cq}$ are the quiescent voltage and current, respectively (discussed in Sect. 2.3).

The basic output characteristics, shown in Fig. 2.15, illustrate three regions of transistor operation: the *active region* in which the emitter–base junction is forward-biased and the collector–base junction is reverse-biased, the *cut-off region* in which the emitter–base junction is not forward biased, and the *saturation region* in which the collector–base junction is not reverse biased. As in the silicon diode, large movements of minority carriers across the base–emitter junction will occur only if the emitter–base junction is forward-biased. If, therefore, the base–emitter voltage $V_{BE} < 0.7$ V the threshold voltage, little or no conduction takes place (only leakage current made up of minority carriers), and the transistor is said to be *cut-off*. Thus, for cut-off operation, $V_{BE} < 0.7$ V (Si), $I_B = 0$, and $I_C = I_{CEO}$. If $V_{BE} \geq 0.7$ V, majority carriers are injected from the emitter into the base region (where they become minority carriers), and their subsequent diffusion across the base into the collector depends on having an adequate reverse bias on the collector–base junction. If this junction is not reverse-biased, injection of carriers into the base will take place from the collector, and under these circumstances, the transistor is *saturated*. Thus, for saturated operation, $V_{BE} \geq 0.7$ V (Si) and the collector–base junction not reverse-biased. The terminal currents in saturation are controlled by the external collector network and not the transistor.
The boundary between saturation and the active region depends on the magnitudes of the currents involved and by Kirchhoff’s voltage law, $V_{CE} = V_{BE} + V_{CB}$. When the transistor is in conduction, $V_{BE}$ is about 0.7 V, and to maintain collector action, $V_{CB}$ must be of sufficient magnitude to collect the carriers injected into the base from the emitter. For signal level currents (units to tens of milliamps) collection requires $V_{CB} \approx 0.3$ V, so that active region operation requires $V_{CE} = 0.7 + 0.3 = 1$ V to avoid saturation, while for very small currents, $V_{CE}$ can be a few tenths of a volt. Thus, for active region operation, $I_B > 0$ or $V_{BE} \approx 0.7$ V, and $V_{CE} > V_{CESat}$. On the curves, in the cut-off region where $I_B = 0$, the small collector current $I_{CEO}$ that flows is leakage current. In the saturation
region, $V_{CE}$ is too small to maintain a reverse bias on the collector–base junction and $I_C$ flows independently of $I_B$. In the active region, the curves are almost horizontal indicating very little dependence of $I_C$ on $V_{CE}$.

### 2.2.2 Common Base Configuration

In the CB configuration, shown in Fig. 2.16, the base terminal is common to both the input and the output circuits. The input signal is applied at the emitter and the output taken at the collector as shown. In this configuration, the output current is approximately equal to the input current, i.e., $I_C \approx I_E$. In the DC mode, as we had before:

$$I_C = \alpha I_E$$  \hspace{1cm} (2.11)

![Common base amplifier](image)
Note that $\alpha \approx 1$ for practical purposes. When $I_E = 0$, collector current continues to flow, and this is the leakage current $I_{CBO}$ made up of minority carriers. It is usually quite small. In the CB configuration, an important parameter is the current gain of the transistor designated $h_{fb}$. It is defined as the ratio of a change in collector current $\Delta I_C$ to the change in emitter current $\Delta I_E$ producing it, the collector–base voltage being held constant:

$$h_{fb} = \frac{\Delta I_C}{\Delta I_E} \Big|_{V_{CB}=\text{constant}}$$  \hspace{1cm} (2.12)

The DC gain $\alpha$ considered earlier is given by

$$\alpha \equiv h_{FB} = \frac{I_C}{I_E}$$  \hspace{1cm} (2.13)

As in the case of the CE configuration, sets of characteristics can be developed in order to connect the currents and voltages into and out of the BJT in this configuration.

### 2.2.2.1 Common Base Input Characteristics

The input characteristic is shown in Fig. 2.17. It involves the input voltage $V_{EB}$ and the input current which in this case is $I_E$. As is evident, the curve is nonlinear and displays a threshold value similar to the CE input characteristics and the diode curve. This is to be expected since the emitter–base junction is a diode.
This transfer characteristic demonstrates the manner in which the collector current changes in response to the emitter current, the collector–base voltage being kept fixed. A typical curve is shown in Fig. 2.17, $V_{CB}$ having negligible effect. The gradient of this characteristic gives the current gain $h_{fb}$ of the transistor. The DC gain $\alpha$ can also be determined. In this characteristic, the collector current is determined almost completely by $I_E$ and is virtually independent of $V_{CB}$. Also, the $I_C/I_E$ characteristic is extremely linear, even more so than the corresponding $I_C/I_B$ characteristic of the CE characteristic. This improved linearity of the transfer characteristic is attributable to negative feedback, which shall be discussed in Chap. 7. $I_C/I_E \approx 1$, and
therefore, this configuration produces no current amplification. This, of course, is consistent with the fact that \( I_E = I_C + I_B \approx I_C \).

**Fig. 2.18** Common base transfer characteristic

### 2.2.2.3 Common Base Mutual Characteristic

The mutual characteristic shows the manner in which the collector current changes in response to changes in the emitter–base voltage, the collector–base voltage held constant. Typical characteristics are shown in Fig. 2.19. The curve is nonlinear as in the CE configuration though the effect of changes in \( V_{CB} \) is even less than the corresponding changes in the CE configuration. The slope is the transconductance \( g_m \) given by

\[
h_{fb} = \frac{\Delta I_C}{\Delta I_E} \bigg|_{V_{CB}=\text{constant}}
\]  

(2.14)

and the value is approximately equal to that in the CE configuration.
2.2.2.4 Common Base Output Characteristics

The output characteristic for varying $I_E$ is shown in Fig. 2.20. Note that these curves are flatter than the corresponding curves for the CE configuration. This indicates that the collector–base voltage in this configuration has an even lower effect on the collector current than the collector–emitter voltage in the CE configuration.
The output curves demonstrate the manner in which the collector current varies with collector–base voltage for constant values of (a) emitter current shown in Fig. 2.20 and (b) emitter–base voltage. The slope at a point on these curves is the output admittance $h_{ob}$ of the transistor given by

$$h_{ob} = \frac{\Delta I_C}{\Delta V_{CB}} \bigg|_{I_E=\text{constant}}$$

(2.15)

The output impedance is $1/h_{ob}$ which is higher than that in the CE configuration (consistent with flatter curves). For this configuration, the regions of operation are defined as follows:

- **Active**: $I_E > 0$, base–emitter junction forward-biased and collector–base junction reverse-biased.
• *Saturation:* $I_E > 0$, base–emitter junction forward-biased and collector–base junction forward-biased.

• *Cut-off:* $I_E = 0$, $I_C = I_{CBO}$, base–emitter junction reverse-biased and collector–base junction forward-biased.

Now

$$I_C = \alpha I_E + I_{CBO} = \alpha (I_C + I_B) + I_{CBO} \tag{2.16}$$

Rearranging, we get

$$I_C = \frac{\alpha I_B}{1 - \alpha} + \frac{I_{CBO}}{1 - \alpha} \tag{2.17}$$

In the CE configuration, when $I_B = 0$,

$$I_C \bigg|_{I_B=0} = \frac{I_{CBO}}{1 - \alpha} \tag{2.18}$$

This corresponds to the collector current for zero base current, i.e., the leakage current $I_{CEO}$. Hence,

$$I_{CEO} = \frac{I_{CBO}}{1 - \alpha} \tag{2.19}$$

This indicates that the leakage current in the CE configuration is much larger than the leakage current in the CB configuration.

### 2.2.3 Common Collector Configuration

In the CC configuration, shown in Fig. 2.21, the collector terminal is common to both the input and the output (since the voltage source powering the circuit has no internal impedance and therefore short-circuits the collector to ground). The input signal is applied at the base and the output is taken at the emitter as shown. In this configuration, the input characteristic $V_B$ vs $I_B$ depends on $R$ and, therefore, is not plotted.
2.2.3.1 Common Collector Transfer Characteristic

There are two transfer characteristics: (a) the current transfer characteristic and (b) the voltage transfer characteristic. The current transfer characteristic indicates the manner in which the emitter current changes in response to base current, the collector–emitter voltage held constant, and this is shown in Fig. 2.22. The slope of this characteristic gives the current gain \( h_{fe} \) defined as:

\[
h_{fe} = \frac{\Delta I_E}{\Delta I_B} \bigg|_{V_{ce}=\text{constant}}
\]  

(2.20)
Note that:

\[
h_{fe} = \frac{\Delta I_E}{\Delta I_B} = \frac{\Delta I_C + \Delta I_B}{\Delta I_B} = h_{fe} + 1 \tag{2.21}\]

This characteristic is reasonably linear and is independent of \( V_{CE} \).

The voltage transfer characteristic, shown in Fig. 2.23, indicates the manner in which the emitter voltage changes in response to the base voltage, the collector–emitter voltage kept constant. The slope of the characteristic gives the short-circuit voltage gain \( A_V \) defined as

\[
A_V = \frac{\Delta V_E}{\Delta V_B} \big|_{V_{CE} \text{ constant}} \tag{2.22}\]
This value is approximately one with no voltage amplification taking place. This characteristic is even more linear than the current transfer characteristic and is attributable to a negative feedback, which shall be discussed in Chap. 7. Also, the voltage characteristic like the current characteristic is virtually independent of changes in $V_{CE}$.

### 2.2.3.2 Common Collector Output Characteristics

In the CC configuration, the appropriate output signal is the voltage $V_E$. Hence, the output characteristic to be displayed is one in which the emitter voltage varies with the collector–emitter voltage. The collector–emitter voltage has essentially no effect on the emitter (output) voltage, and therefore, this family of curves is not particularly useful in practice. Note that $V_E = V_B - 0.7$. Hence $V_E \approx V_B$, that is, the output signal voltage at the emitter is approximately equal to the input signal voltage at the
base. As a result, this configuration is referred to as the emitter follower. The regions of operation are:

- **Active**: $V_{EB} \approx 0.7$ V.
- **Saturation**: $V_{EB} \geq 0.7$ V, $V_{CB}$ not reverse-biased.
- **Cut-off**: $V_{EB} < 0.7$ V, $I_E = 0$.

### 2.3 Common Emitter Amplifier

Having discussed the characteristics of the BJT in the various configurations, we now consider the application of each configuration in functioning circuits, starting with the CE configuration.

#### 2.3.1 Transistor Amplifying Action

To demonstrate the amplifying action of BJT, we use the CE configuration, as shown in Fig. 2.24. Here a sinusoidal signal is applied at the base–emitter junction of BJT, and to ensure that carriers generated in the emitter by the action of $V_i$ are collected at the collector, a voltage $V_{CC}$ is applied. Thus, as $V_i$ goes positive (for the NPN transistor), for a sufficiently large $V_i (>0.7$ V), the transistor is turned on (the base–emitter junction becomes forward biased), and electrons flow from the emitter across the base region, most being collected by the collector. A small number flow out of the base terminal. These electron flows correspond to conventional currents $I_E$, $I_C$, and $I_B$ as shown. Since a large collector current $I_C$ flows in response to a small base current $I_B$, this corresponds to the current amplification of $I_B$. Since most signals are in the form of a voltage, we are more interested in the amplification of the input voltage $V_i$ which also influences $I_C$. 
To use the output signal $I_C$ conveniently, a resistor $R_L$ is included in the collector circuit, as shown. This will not affect the action of the transistor because of the excellent charge carrier collecting ability of the collector under conditions of varying collector voltage. The presence of $R_L$ in the collector circuit means that $I_C$ produces a voltage drop $V_C = I_C R_L$ across this resistor which can be readily measured. It turns out that in bipolar junction transistors, the ratio $V_C/V_i$ can be quite large, typically of the order of a few hundred, thereby representing voltage amplification of $V_i$. This voltage amplification by the transistor is partly what has enabled it to revolutionize the electronics industry in a manner that continues today.

There are however two problems with the amplifying action just described. The first is that on the positive half-cycle of the input signal, $V_i$ must exceed 0.7 V before the transistor is turned on resulting in a flow of ($I_B$ and) collector current $I_C$. During the period before this turn on occurs, no collector current flows ($I_C = 0$), and hence there is no output voltage ($V_C = I_C R_L = 0$). This results in severe signal distortion. The second more serious problem occurs on the negative half cycle for $V_i$. 

*Fig. 2.24* Common emitter amplifier
During the part of the signal cycle, the transistor remains off and hence there is no signal transmission and therefore no amplification occurs. The result, as shown in Fig. 2.25, is that there is collector current flow for approximately only one half-cycle of the input signal. The voltage developed across the collector resistor will therefore be severely distorted.

![Waveform distortion resulting from zero biasing](image)

**Fig. 2.25** Waveform distortion resulting from zero biasing

Both problems are easily solved by turning on the transistor with suitable DC voltages and establishing a standing current $I_{Cq}$ in the device. This process is called BIASING, and the currents and voltages in the BJT are called bias or quiescent currents and voltages. This is shown in Fig. 2.26. The voltage source $V_{BB}$ is used to turn on the BJT by forward biasing the base–emitter junction. For no input signal ($V_i = 0$), this
results in DCs $I_{Cq}$ and $I_{Bq}$. When $V_i$ is applied in series with $V_{BB}$, it modulates or changes the value of the transistor base voltage such that the base–emitter voltage of the BJT is varied about its quiescent value $V_{BEq}$. This results in a corresponding variation of the collector current about its quiescent value $I_{Cq}$. $V_{BB}$ and $V_i$ must be such that the transistor never turns off at any point during the signal cycle. As can be seen in Fig. 2.27, $I_C$ is fully reproduced eliminating both the dead bands on the positive half-cycle and the nonconduction on the negative half-cycle. This results in a full voltage waveform $V_o$ at the collector of the transistor about the quiescent collector voltage $V_{Cq}$ as shown in Fig. 2.28.

![Common emitter amplifier with bias](image)

**Fig. 2.26** Common emitter amplifier with bias
Fig. 2.27 No waveform distortion with biasing
Note that the output voltage waveform is inverted relative to the input voltage waveform since, as the collector current increases say, the voltage drop across the collector resistor \( R_L \) also increases, and hence, by Kirchhoff’s voltage law, the voltage at the collector of the transistor decreases \( (V_o = V_{CC} - I_C R_L) \). This biasing scheme has the disadvantage that DC flows through the signal source which is undesirable. A second problem is that setting the bias current \( I_{Cq} \) by adjusting \( V_{BB} \) is virtually impossible because of the steep slope of the \( V_{BE} \) vs \( I_C \) curve beyond the knee in Fig. 2.9. A practical biasing scheme that overcomes these problems and the selection of \( I_{Cq} \) and \( R_L \) in order to achieve optimum performance as part of the design process is discussed next.

**Fig. 2.28** Undistorted collector voltage
2.3.2 Fixed Biasing

The basic scheme is shown in Fig. 2.29. It utilizes the fact that there is no knee on the CE transfer characteristic (2.10) and control of $I_C$ using $I_B$ is quite practical. In this approach, the bias voltage is applied to the base–emitter junction via resistor $R_B$. The effect of this is to fix $I_B$ at some value. Thus, for the base circuit, applying Kirchhoff’s voltage law:

$$V_{BB} = I_B R_B + V_{BE}$$  \hspace{1cm} (2.23)

since the transistor is on, $V_{BE} \approx 0.7$ V and therefore:

$$I_B = \frac{V_{BB} - 0.7}{R_B}$$  \hspace{1cm} (2.24)

Fig. 2.29 Common emitter amplifier with modified biasing

Hence:

$$I_C = \beta I_B = \frac{\beta}{R_B} (V_{BB} - 0.7)$$  \hspace{1cm} (2.25)

Equation (2.25) is the bias-setting equation. Knowing $\beta$ for the transistor, $R_B$ can be selected to give the desired $I_C$. 
The problem of DC bias through the signal source is addressed by the removal of the signal source from the position in which it is located in Fig. 2.26 and applying it to the input through a capacitor $C$, referred to as a coupling capacitor. This capacitor blocks the DC coming from $V_{BB}$ from flowing into the signal source. This DC could both damage the signal source and upset the bias conditions in transistor $Tr_1$. At the signal frequencies, the capacitor is assumed to be large such that its impedance is negligible and hence does not interfere with the signal flow into the transistor. We shall discuss choosing this value later.

A second important equation is that defining the output circuit including $V_{CE}$ and $I_c$ for the BJT. Applying Kirchhoff’s voltage law to the output circuit, we get:

$$V_{CC} = I_c R_L + V_{CE}$$  \hspace{1cm} (2.26)

It is called the DC load line for the circuit and represents the locus of all the possible operating $V_{CE}/I_c$ points for the device in the particular circuit under consideration. This line is plotted on the CE output characteristics, as shown in Fig. 2.30. From (2.26) when $I_c = 0$, $V_{CE} = V_{CC}$ and the transistor is cut-off. In such circumstances, there is no voltage drop across the collector resistor, and therefore the collector voltage is at $V_{CC}$, the supply voltage. When $V_{CE} = 0$, $I_c = \frac{V_{CC}}{R_L}$. This corresponds to the transistor in saturation with the maximum collector current flowing. There is usually a small voltage across the collector–emitter terminals giving the collector–emitter saturation voltage $V_{CESat} \approx 0.2 \text{ V}$. Hence, biasing sets $V_{CE}$ and $I_c$ at some operating point Q on the load line.
To amplify a sinusoidal signal $V_i$, the signal is superimposed on the DC bias conditions at the base of the transistor as shown in Fig. 2.29. For the NPN transistor, as $V_i$ goes positive corresponding to conventional current flowing into the base, the base-emitter voltage is increased, and hence the collector current $I_C$ increases. The voltage drop across $R_L$ therefore increases, and since $V_{CC}$ is fixed, $V_{CE}$ is lowered. This is manifested as a movement up the load line. As $V_i$ goes negative, the base-emitter voltage is reduced, and hence the collector current decreases with a resulting movement down the load line. When $V_{CE}$ is reduced to $V_{CESat}$ ($\approx 0.2$ V), the transistor is saturated. When $V_{CE}$ is increased such that $V_{CE} = V_{CC}$ ($I_C = 0$), the transistor is cut-off. These values of $V_{CE}$ represent the maximum and minimum voltages possible across the transistor.
In the amplification of a signal, in order for the transistor to faithfully reproduce the full waveform, $V_{CE}$ must be able to increase and decrease by approximately the same value. This is referred to as maximum symmetrical swing. Thus, since $V_{CE\text{max}} = V_{CC}$ and $V_{CE\text{min}} \approx 0 \, \text{V}$, it follows that the maximum change in $V_{CE}$ is $V_{CC}$. Therefore, for maximum symmetrical swing, we let $V_{CEq} = V_{CC}/2$, that is, set the quiescent collector voltage to be half of the supply voltage $V_{CC}$. In such a case, $I_{Cq} = I_{C\text{max}}/2$ where $I_{C\text{max}} = V_{CC}/R_L$. This will enable $V_{CE}$ to increase by $V_{CC}/2$ to $V_{CC}$ and decrease by the same amount $V_{CC}/2$ to zero. Also, instead of using two DC supplies $V_{CC}$ and $V_{BB}$, a single supply or $V_{CC}$ can be used as shown in Fig. 2.31 with $R_B$ connected to $V_{CC}$. Then in the bias-setting Eq. (2.25), $V_{BB}$ must be replaced by $V_{CC}$. Capacitor $C_2$, like $C_1$, is a coupling capacitor that couples the output signal to an external load while preventing the DC voltage at the collector of $Tr_1$ from interfering with or be interfered by that load.

![Common Emitter Amplifier Using One Power Supply](image)

**Fig. 2.31** Common emitter amplifier using one power supply

**Example 2.1** Using the circuit of Fig. 2.31, design a fixed-bias CE amplifier with a 20V supply and an NPN silicon transistor having $\beta = 100$. Design for maximum symmetrical swing.

**Solution** Choose $I_{Cq} = 1 \, \text{mA}$ for effective transistor operation. For maximum symmetrical swing, $V_{CEq} = V_{CC}/2$. Hence $V_{CEq} = 20/2 = 10 \, \text{V}$.
and $R_L = 10/1 \ mA = 10 \ k\Omega$. Since $\beta = 100$, and $I_B = I_C/\beta$, it follows that $I_{Bq} = \frac{1 \ mA}{100} = 10 \ \mu A$. Kirchhoff’s voltage law applied at the input yields $V_{CC} = I_{Bq}R_B + V_{BE}$. Therefore, $R_B = \frac{V_{CC} - V_{BE}}{I_{Bq}} = \frac{20-0.7}{10 \mu A} = 1.93 \ M\Omega$, that is, $R_B = 1.93 \ M\Omega$. The capacitors are chosen to be large say 50 \ \mu F. Hence with $R_B = 1.93 \ M\Omega$, $I_{Cq} = 1 \ mA$, $V_{CEq} = 10 \ V$ and the NPN silicon transistor is biased for maximum symmetrical swing.

A signal voltage can now be applied at the input through coupling capacitor $C_1$; the output voltage is available at the collector through coupling capacitor $C_2$. Oscilloscope traces of the input and output are shown in Fig. 2.32. The input capacitor $C_1$ presents a reactance $X_{C_1} = 1/2\pi fC_1$ to the input signal of frequency $f$. If $C_1$ is sufficiently large, then this reactance is negligible for signal frequencies and therefore is practically a short-circuit to such signals. It however blocks the flow of direct current, which would change the transistor bias current as well as possibly affect the signal source. This also applies to the output capacitor $C_2$. Methods of determining these values are discussed in Chap. 6.
The mutual characteristic shown in Fig. 2.33 illustrates the action of the transistor in the biased CE configuration. The Q point established by the bias is shown as $I_{Cq}$ and $V_{BEq}$. The input signal $V_i$ causes a variation $\Delta V_{BE}$ in $V_{BE}$ which results in a corresponding change $\Delta I_C$ in $I_C$. Thus, a change $\Delta V_{BE}$ in $V_{BE}$ produces a change $\Delta I_C$ in the collector current $I_C$ that results in a change $\Delta V_C = -\Delta I_C R_L$ in the collector (output) voltage $V_C$. The negative sign indicates that as $\Delta V_{BE}$ increases, $\Delta I_C$ increases, and hence the voltage drop across $R_L$ increases. This corresponds to a lowering of the transistor collector voltage $V_C$ by $\Delta V_C$ which is the output voltage $V_o$. It should be noted that the input signal can also be a current $I_i$ into the transistor base resulting in a change $\Delta I_B$ in $I_B$. This results in a change $\Delta I_C$ in $I_C$ and hence an output voltage $V_o = \Delta V_C$. However, most input signals are in the form of a voltage rather than a current, and hence, the focus is on input voltage signals.
2.3.3 Amplification

Now $\Delta I_C/\Delta V_{BE}$ is (approximately) the transconductance $g_m$ of the transistor, and in order to evaluate the voltage gain $\Delta I_C R_L/\Delta V_{BE}$, we need to consider the diode equation:

$$I_D = I_o \left( e^{\frac{qV_D}{mkT}} - 1 \right)$$

(2.27)

Differentiating $I_D$ with respect to $V_D$ gives:

$$\frac{dI_D}{dV_D} = I_o \left( \frac{q}{mkT} \right) e^{\frac{qV_D}{mkT}}$$

(2.28)
Noting that \( I_o \) is small, for values of \( I_D \) such that \( I_D \gg I_o \), then:

\[
\frac{dI_D}{dV_D} = \frac{q}{mkT} I_D \tag{2.29}
\]

For the transistor, \( I_D \equiv I_E \approx I_C \) and \( V_D \equiv V_{BE} \). Also, \( m \approx 1 \) and \( T = 300 \) K (room temperature) \( \frac{q}{mkT} = 40 \) \( \text{V}^{-1} \). Therefore, using (2.29), we get

\[
h_{ob} = \frac{\Delta I_C}{\Delta V_{CB}} \bigg|_{I_E=\text{constant}} \tag{2.30}
\]

Hence, \( g_m = 40 \ I_C \ A/V \) or \( g_m = 40 \ I_C \ mA/V \); where \( I_C \) is the current value in milliamperes. Note that this is approximately the same for all transistors. The voltage gain \( A_V \) of the simple CE voltage amplifier can now be found. It is given by

\[
A_V = \frac{-\Delta I_C R_L}{\Delta V_{BE}} = -40 \ I_C R_L = -g_m R_L \tag{2.31}
\]

which is approximately the same for all transistors. Again, the negative sign indicates inversion of the output voltage relative to the input signal, i.e., these two signals are 180° out of phase as shown in Fig. 2.32. The input impedance \( Z_i \) at the base of the CE amplifier is the ratio of the input voltage change \( \Delta V_{BE} \) to the corresponding input current change \( \Delta I_{BE} \) flowing into the base circuit. Thus, noting that \( I_C = \beta I_B \) and hence \( \Delta I_C = \beta \Delta I_B \):

\[
Z_i = \frac{\Delta V_{BE}}{\Delta I_B} = \frac{\Delta V_{BE}}{\Delta I_C / \beta} = \frac{\beta}{g_m} \tag{2.32}
\]

That is:

\[
(2.33)
\]
For the circuit developed in Example 2.1, determine the voltage gain and input impedance.

Solution For the circuit of Fig. 2.31, $R_L = 10 \, \text{k}\Omega$ and $I_C = 1 \, \text{mA}$. Hence using (2.31) $A_V = -40 \, I_C \, R_L = -40 \times 1 \times 10^{-3} \times 10 \times 10^3 = -400$. Using the peak values of the output and input voltages from Fig. 2.32, we find that the measured voltage gain is $-350$. Thus, the formula for gain is only an approximate one. Using $\beta = 100$, the input impedance $Z_i$ is from (2.33) given by $Z_i = \frac{100}{40 \times 1 \times 10^{-3}} = 2.5 \, \text{k}\Omega$. Thus, in the CE amplifying mode, the input impedance of the transistor is of moderate value only.

The amplified signal produced by this circuit while having reasonable fidelity for small-signal inputs does possess some level of distortion; see Fig. 2.33. It can be seen that equal changes $\pm \Delta V_{BE}$ of $V_{BE}$ do not produce equal changes $\pm \Delta I_C$ of $I_C$. The positive-going change $+\Delta V_{BE}$ in $V_{BE}$ produces a larger collector current change than the negative-going change $-\Delta V_{BE}$. This arises because of the nonlinearity of the $I_C/V_{BE}$ characteristic and results in the output voltage having a larger negative-going amplitude than the positive-going amplitude for equal amplitude bipolar inputs. This constitutes signal distortion. The effect can be reduced by (i) increasing $I_{Cq}$ such that the $Q$ point is at an increasingly linear part of the characteristic or (ii) reducing the variation of $I_C$ and thereby restricting operation to an approximately linear part of the characteristic. Operating in the latter manner is called a small-signal operation.

2.3.4 Circuit Analysis

It is sometimes necessary to analyze a given amplifier circuit to determine the voltages and currents in that circuit.

Example 2.3 Determine the collector current and voltage in the fixed-bias amplifier of Fig. 2.34, assuming transistor current gain of 100.
Solution  In analyzing this circuit, maximum symmetrical swing capability cannot be assumed. Therefore, the analysis is started by determining the base current $I_B$. Thus, applying Kirchhoff’s voltage law to the base circuit, we have $25 = I_B \times 1.5 \times 10^6 + 0.7$. This gives $I_B = 16.6 \ \mu A$. Hence the collector current is $I_C = 100 \times 16.6 \times 10^{-6} = 1.7 \ mA$. From this, $V(5 \ k) = 1.7 \ mA \times 5 \ k = 8.5 \ V$ and therefore the collector–emitter voltage $V_{CE} = 25 - V(5 \ k) = 25 - 8.5 = 16.5 \ V$.

2.4 Alternative Biasing Methods
As we have discussed, in order that a BJT is able to amplify a signal, it must be turned on so that a suitable operating point is established. The simplest method and the one already discussed is called fixed biasing (or constant current biasing). The name is derived from the fact that the base current $I_B$ is the parameter that is fixed (by fixing $R_B$ and $V_{CC}$). Since $I_C = \beta I_B$, fixing $I_B$ results in a particular value of $I_C$ being established in the transistor. There are however several problems with this technique. Firstly, it is evident that since $I_C = \beta I_B$ and $I_B$ is fixed, then $I_C$ is dependent upon the value of $\beta$. For a specific transistor such as the 2N3904, the
value of $\beta$ varies widely from one device to another. Therefore, if the transistor is changed, even though it is the same number, $\beta$ changes and hence so does $I_C$.

$\beta$ also varies from one transistor type to another. For example, the 2N3904 has $\beta$ typically at 150, while the 2N2222 has $\beta$ at about 50. $\beta$ also changes as a result of collector current changes, as shown in Fig. 2.35. Finally, $\beta$ is also temperature-dependent as can be seen in Fig. 2.35, and in response to a change of temperature may more than double its value. The effect of all $\beta$ changes is a change in collector current. This results in a movement of the Q point, which reduces the maximum symmetrical swing and in extreme circumstances may push the transistor into saturation or close to cut-off.

![Graph of current gain vs collector current](image)

**Fig. 2.35** Current gain vs collector current

**Example 2.4** Given a DC supply of 10 V, a load resistor of 1 k and a silicon NPN transistor with $\beta = 100$ at room temperature, (a) bias the transistor for maximum symmetrical swing and (b) calculate the value of $V_{CEq}$ at 50 °C if $\beta$ goes to 75.

**Solution** By Kirchhoff’s voltage law, $V_{CC} = I_C R_L + V_{CEq}$. For maximum symmetrical swing, $V_{CEq} = V_{CC}/2 = 10/2 = 5V$. Hence since $R_L = 1$ k, then
\[ I_C = \frac{(V_{CC} - V_{CEq})}{R_L} = \frac{(10 - 5)}{1 \text{k}} = 5 \text{ mA}. \] Now \( I_B = \frac{I_C}{\beta} = 5 \text{ mA}/100 = 50 \mu\text{A} \) and \( R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{10 - 0.7}{50 \mu\text{A}} = 186k\Omega \)

(a) Since \( I_B \) is fixed and \( \beta \) has changed to 75, the collector current at 50 °C can be found as follows: \( I_C = \beta I_B = 75 \times 50 \mu\text{A} = 3.75 \text{ mA} \) at 50 °C. The resulting quiescent collector voltage \( V_{CE} \) is given by

\[ V_{CEq} = V_{CC} - I_{Cq}R_L = 10 - 3.75 = 6.25 \text{V}. \]

When the BJT is biased for maximum symmetrical swing at \( V_{CEq} = 5 \text{V} \), the peak output voltage is 5Vpk or 10Vpk-pk.

(b) At 50 °C, when \( \beta \) increased, the increased collector current reduces the symmetrical swing to \( 3.75 \times 2 = 7.5 \text{V} \).

Fixed biasing is therefore not a very good biasing method as it allows wide variation in \( I_C \) which affects the circuit performance. Its main advantages, however, are its simplicity and resulting high voltage gain.

### 2.4.1 Voltage Divider Biasing

Because of the wide variations in \( \beta \), a different biasing scheme that is approximately independent of \( \beta \) is required. The voltage divider biasing method, shown in Fig. 2.36, is one such technique. It exhibits excellent Q point stability and is little affected by \( \beta \). As a result, it is one of the most commonly used in CE amplifiers. It comprises resistors \( R_1 \) and \( R_2 \) which form a voltage divider and thereby attempt to fix the base voltage rather than the base current. In addition, the resistor \( R_E \) in the emitter circuit of the transistor, working in conjunction with the fixed base voltage created by \( R_1 \) and \( R_2 \), effectively stabilizes the collector current. Thus, with a fixed base voltage, if \( I_C \) tries to increase as a result of temperature changes say, then the voltage drop across \( R_E \) would increase, thereby increasing the emitter voltage of the transistor. Since the base voltage is fixed, the base–emitter voltage of the transistor would decrease, thereby causing a decrease in the collector current close to its original value. Conversely, if \( I_C \) tries to decrease, then the voltage drop across \( R_E \) would decrease, thereby reducing the emitter voltage of the transistor. With a
fixed base voltage, it follows that the base-emitter voltage would increase, and this would result in an increase in the collector current close to its original value. Capacitor $C_3$ short-circuits resistor $R_E$ for signals, thereby nullifying the current stabilizing action of this resistor for signals. It is referred to as a bypass or decoupling capacitor.

![Voltage divider-biased common emitter amplifier](image)

*Fig. 2.36* Voltage divider-biased common emitter amplifier

Consider the circuit with the potential divider network comprising $V_{CC}$, $R_1$, and $R_2$ replaced by the Thevenin equivalent, as shown in Fig. 2.37 (with capacitors removed). Here:

\[
V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC} \quad (2.34)
\]

\[
R_B = \frac{R_1 R_2}{R_1 + R_2} \quad (2.35)
\]
Thus, for the base–emitter loop:

\[ V_{BB} = I_B R_B + V_{BE} + I_C R_E \]  \hspace{1cm} (2.36)

But \( I_B = I_C / \beta \). Therefore, (2.36) becomes:

\[ V_{BB} = \frac{I_C}{\beta} R_B + V_{BE} + I_C R_E \]  \hspace{1cm} (2.37)

which when rearranged yields:

\[ I_C = \frac{V_{BB} - V_{BE}}{R_E + R_B / \beta} \]  \hspace{1cm} (2.38)
From the numerator in Eq. (2.38), the effect on \( I_C \) of variations of \( V_{BE} \) around 0.7 V caused by temperature changes can be reduced by making
\[
V_{BB} \gg V_{BE} \tag{2.39}
\]

This ensures that \( V_{BB} - V_{BE} \approx V_{BB} \) in (2.38), i.e., that \( V_{BE} \) is small compared with \( V_{BB} \), thereby making \( I_C \) virtually immune to changes in \( V_{BE} \). From the denominator in Eq. (2.38), the effect on \( I_C \) of variations of \( \beta \) can be reduced by making
\[
R_E \gg R_B / \beta \tag{2.40}
\]

This results in \( R_E + R_B / \beta \approx R_E \) in (2.38), thereby rendering \( I_C \) independent of \( \beta \).

Now (2.39) will be satisfied if \( V_{RE} = I_C R_E \) is made very much larger than \( V_{BE} \) says \( V_{RE} \geq 5 V_{BE} = 3.5 \text{V} \) in which case \( R_E = 3.5 / I_C q \). This value of \( V_{RE} \) may be too large if for a given \( V_{CC} \), a particular peak-to-peak output swing is desired. For example, if \( V_{CC} = 10 \text{V} \), then for \( V_{RE} = 3.5 \text{V} \), the maximum peak-to-peak swing available is \( 10 - 3.5 = 6.5 \text{V} \) which is \( 3.25 \text{V} \) peak. If a higher peak output swing is required, it may be necessary to lower \( V_{RE} \). In general, therefore, a good rule of thumb is to choose \( V_{RE} \) such that:
\[
V_{RE} = V_{CC} / 10 \tag{2.41}
\]

Consider inequality (2.40), this can be rearranged to give:
\[
\frac{R_1 + R_2}{R_1 R_2} \gg \frac{1}{R_E / \beta} \tag{2.42}
\]

Multiplying both sides by the emitter voltage \( V_{RE} \) gives:
\[
\frac{V_{RE}}{R_2} \left(1 + \frac{R_2}{R_1}\right) \gg \frac{V_{RE}}{R_E / \beta} \tag{2.43}
\]

Since \( V_{RE} \) is made very much larger than \( V_{BE} \) and \( V_{Bq} = V_{BE} + V_{RE} \) it follows that:
\[
V_{Bq} \approx V_{RE} \tag{2.44}
\]
Inequality (2.43) therefore becomes:

\[
\frac{V_{Bq}}{R_2} \left(1 + \frac{R_2}{R_1}\right) \gg \frac{V_{RE}}{R_E} / \beta
\]  

(2.45)

Now \(V_{Bq}/R_2\) is the current \(I_R\) through resistor \(R_2\) of the potential divider, while \(V_{RE}/R_E\) is the collector current \(I_C\). Thus (2.45) can be written:

\[
I_R \left(1 + \frac{R_2}{R_1}\right) \gg \frac{I_C}{\beta} = I_B
\]  

(2.46)

This is satisfied if:

\[I_R \gg I_B\]  

(2.47)

Inequality (2.47) requires that the current through the potential divider is much larger than the base current of the transistor which the divider supplies. This ensures that the potential divider voltage \(V_{Bq}\) is approximately fixed. Inequality (2.47) is approximately satisfied if

\[I_R \geq 10 \cdot I_B\]  

(2.48)

Since \(\beta \approx 100\) for most (small-signal) transistors and \(I_C = \beta I_B\), then:

\[I_R \geq I_C / 10\]  

(2.49)

where \(I_R\) is the current flowing through the resistors \(R_1\) and \(R_2\) of the potential divider. Note however that \(I_R\) cannot be too large since these resistors affect the input impedance of the amplifier and may also represent a drain on the power supply. A simple design procedure for a CE amplifier can now be outlined:

1. Choose \(V_{CC}\) and \(I_{Cq} \cdot V_{CC}\) may depend on the available supply. \(I_{Cq}\) is usually in the range 0.1 mA to 10 mA depending on noise, transistor current gain, and frequency response characteristics.
2. To minimize the effects of \(V_{BE}\) changes, \(V_{RE} \geq 5V_{BE}\) which for silicon is \(V_{RE} \geq 3.5\) V. The required output voltage swing and available supply voltage may preclude the use of this design rule. In general, therefore, a good rule of thumb that is a reasonable compromise
between large voltage swing and high quiescent current stability is
\[ V_{RE} = \frac{1}{10} V_{CC} \].

3. \( R_E \geq \frac{R_B}{\beta} \), where \( R_B = \frac{R_1 R_2}{R_1 + R_2} \) in order to minimize changes in \( I_C \) due to changes in \( \beta \). This criterion can be generally realized by choosing \( I_R = \frac{1}{10} I_C \) where \( I_R \) is the current along the potential divider \( R_1, R_2 \).

4. \( V_{Bq} = V_{RE} + V_{BE} = I_R R_2 \) therefore, \( R_2 = \frac{V_{Bq}}{I_R} R_1 = \frac{(V_{CC} - V_{Bq})}{I_R} \).

5. For maximum symmetrical swing, \( V_{RL} = \frac{V_{CC} - V_{RE}}{2} \), and therefore
\[ R_L = \frac{V_{CC} - V_{RE}}{2I_{Cq}}. \] \( V_{RE} \) is held constant by the capacity \( C_3 \).

6. Select large (of order of tens of \( \mu F \)) capacitor values for good low-frequency response.

7. Calculate the resulting voltage gain using \( A_V = -g_m R_L \).

**Example 2.5**  Design a voltage divider-biased CE amplifier using an 18 V supply and an NPN silicon transistor having \( \beta = 100 \).

**Solution**  Choose \( I_{Cq} = 1 \) mA for good \( \beta \) and frequency response. Using rule-of-thumb (2.41) \( V_{RE} = 18/10 = 1.8 \) V. Use \( V_{RE} = 2 \) V. Hence, \( R_E = 2/1 \) mA = 2 k and \( R_L = \frac{18-2}{1 \text{ mA} \times 2} = 8 \) k. \( V_{Bq} = V_{RE} + V_{BE} = 2.7 \) V, and from (2.49), \( I_R = I_{Cq}/10 = 0.1 \) mA. Therefore, \( R_2 = \frac{2.7 \text{ volts}}{0.1 \text{ mA}} = 27 \) k and
\[ R_1 = \frac{18-2.7}{0.1 \text{ mA}} = 153 \) k. Choose \( C_3 = 47 \mu F \). The resulting voltage gain is
\[ A_V = -40 I_c R_L = -40 \times 1 \text{ mA} \times 8 \text{ k} = -320. \] To complete the design, large coupling capacitors, say 47 \( \mu F \), are used at the input and output. Note that the DC voltage at the emitter is kept constant by the capacitor \( C_3 \).
and hence maximum peak-to-peak symmetrical swing is reduced from $V_{CC}$ to $V_{CC} - V_{RE}$. A further point is that the resistors $R_1$ and $R_2$ are effectively in parallel with the input signal. Thus, although their values must be sufficiently low to ensure that $I_R \geq 10I_B$ for bias stability, they cannot be too low since they will load down the input signal.

Consider now the analysis of a voltage divider-biased CE amplifier circuit.

**Example 2.6** In the CE voltage, divider-biased-biased amplifier of Fig. 2.38 determines the collector current and the collector voltage.

![Fig. 2.38 Circuit for Example 2.6](image)

**Solution** In analyzing this circuit, once again maximum symmetrical swing cannot be assumed, and therefore the voltages and currents in the collector circuit are at this point unknown. The analysis must hence start at the base circuit where conditions can be determined. Specifically, making the reasonable assumption that the base current is much less than the current through the voltage divider, then
\[ V_B = \left( \frac{20}{20 \times k + 180} \right) \times 26V = 2.6V \]. This gives \( V_E = V_B - 0.7 = 1.9 \text{ V} \).

Therefore, the collector current is \( I_C = 1.9/1 \text{ k} = 1.9 \text{ mA} \) which gives \( V(6 \text{ k}) = 1.9 \text{ mA} \times 6 \text{ k} = 11.4 \text{ V} \). Hence, collector voltage \( V_C = 26 - V(6 \text{ k}) = 26 - 11.4 = 14.6 \text{ V} \). Finally, note that the collector-emitter voltage \( V_{CE} \) is given by \( V_{CE} = V_C - V_E = 14.6 - 1.9 = 12.7 \text{ V} \).

### 2.4.2 Current Feedback Biasing

Another effective biasing scheme for bias stabilization is current feedback biasing (also called collector–base feedback biasing) shown in Fig. 2.39a. This technique results in almost the same level of stability as the voltage divider biasing method but in this form has the disadvantage of a reduced gain because of the feedback resistor \( R_B \). The circuit functions as follows: if the collector current tries to increase, the increased voltage drop across \( R_L \) will result in a reduced collector voltage. This in turn reduces the base current \( I_B \) flowing through \( R_B \) into the transistor, thereby reducing \( I_C \). The converse occurs for a decrease in \( I_C \). The problem of reduced gain in this circuit can be overcome by splitting \( R_B \) and connecting a capacitor \( C_G \) to the ground, as shown in Fig. 2.39b. The effect of this capacitor is to remove the feedback action for signal frequencies while retaining it for DC. A simple design procedure is the following:

1. Choose a collector current \( I_{Cq} \). Since \( \beta \) is large, the base current is small, and hence the current through \( R_L \) is approximately equal to \( I_{Cq} \).
2. For maximum symmetrical swing, \( V_{CEq} = V_{CC}/2 \) and hence \( R_L = V_{CC}/2I_{Cq} \).
3. For \( R_B \), \( V_{RB} = V_{CEq} - V_{BE} \), and therefore \( R_B = (V_{CEq} - V_{BE})/I_B \) where \( I_B = I_{Cq}/\beta \). As in fixed biasing, \( \beta \) must be known.
Example 2.7 Using the configuration in Fig. 2.39a, design a CE amplifier utilizing current feedback biasing. Use an NPN silicon transistor having $\beta = 150$ and a 15 V supply.

Solution Choose $I_{Cq} = 1\text{mA}$. For maximum symmetrical swing, $V_{CEq} = V_{CC}/2 = 7.5\text{ V}$. Hence, $R_L = 7.5/1\text{ mA} = 7.5\text{ k}$ and $R_B = (7.5 - 0.7)/(1\text{ mA}/150) = 1.02\text{ M}\Omega$. The capacitors are chosen to be large say 50 $\mu\text{F}$. The problem of reduced gain in this circuit can be overcome by splitting $R_B$ and connecting a capacitor $C_G$ of about 50 $\mu\text{F}$ to the ground, as shown in Fig. 2.39b. The effect of this capacitor is to remove the feedback action for signal frequencies.

Analysis of the collector–base feedback-biased circuit is almost as straightforward as the other cases.

Example 2.8 Determine the collector current and voltage for the circuit shown in Fig. 2.40 assuming $\beta = 100$. 

---

**Fig. 2.39** Common emitter amplifier with collector–base feedback biasing
Solution Using Kirchhoff’s voltage law, two equations for $V_C$ can be written. They are $V_C = I_B \times 800 \, \Omega + 0.7$ and $V_C = 20 - I_C \times 2 \, \Omega = 20 - \beta \times I_B \times 2 \, \Omega$. Setting the right-hand side of these two equations equal and solving for $I_B$ yield $I_B = 19.3 \, \mu A$, and therefore, $I_C = \beta I_B = 1.9 \, mA$. From this, $V_C = 20 - I_C \times 2 \, \Omega = 20 - 1.9 \, mA \times 2 \, \Omega = 16.2 \, V$.

### 2.4.3 Biasing Using a Bipolar Supply

It is possible to bias the CE amplifier using a bipolar power supply, as shown in Fig. 2.41. Here the collector of the transistor goes to the positive supply $+V_{CC}$ through $R_L$ as before. However, the emitter is not returned to the ground but instead goes to a negative supply $-V_{CC}$ through a resistor $R_E$ which together set the collector current value. The resistor $R_B$ which supplies base current to the transistor is connected to the ground, thereby setting the base at an approximately zero potential. Capacitors $C_1$ and $C_2$ are the usual input and output coupling capacitors, while $C_3$ is the decoupling capacitor that grounds the emitter for signals.
**Example 2.9**  Design a CE amplifier using the configuration in Fig. 2.41 with a ±15 V bipolar supply and a transistor with \( \beta = 100 \).

**Solution**  Choose \( I_{Cq} = 1 \text{ mA} \) for effective transistor operation. Noting that capacitor \( C_3 \) holds the emitter at a fixed voltage close to the ground, for maximum symmetrical swing, \( V_{CEq} = V_{CC}/2 \). Hence, \( V_{CEq} = 15/2 = 7.5 \text{ V} \) and \( R_L = 7.5/1 \text{ mA} = 7.5 \text{ k} \). Since \( \beta = 100 \), and \( I_B = I_C/\beta \), it follows that

\[
I_{Bq} = \frac{1 \text{ mA}}{100} = 10 \text{ \mu A}.
\]

Resistor \( R_B \) allows this bias current to flow into the base of the transistor. Its value should be of the order of 10 k. With the transistor base at approximately zero potential, Kirchhoff’s voltage law applied to the emitter circuit yields

\[
-0.7 - (-V_{CC}) = I_{Cq}R_E.
\]

Thus, \( R_E = \frac{-0.7 + 15}{I_{Cq}} = \frac{15 - 0.7}{1 \text{ mA}} = 14.3 \text{ k} \), that is, \( R_E = 14.3 \text{ k} \). The capacitors are chosen to be large say 50 \( \mu \)F.
2.5 Common Base Amplifier

The CB amplifier is shown in Fig. 2.42. As in the case of the CE amplifier, in order for the CB circuit to operate properly, biasing is necessary to ensure that a complete signal cycle is reproduced. Therefore, a DC source $V_{BB}$ is again used to turn on the transistor so that a quiescent collector current flows in the transistor before an input signal is applied. This arrangement is shown in Fig. 2.43. The signal input $V_i$ then modulates this current so that a voltage change appears across resistor $R_L$. Similar to the CE circuit, this approach has the undesirable feature that DC flows through the signal source. As it turns out, the various biasing schemes used in the CE configuration can all be used in the CB configuration with minimal adjustments. We will first consider voltage divider biasing.
2.5.1 Voltage Divider Biasing

The voltage divider biasing technique applied to be CB configuration is shown in Fig. 2.44b. The components are the same as those used in the CE voltage divider-biased amplifier in Fig. 2.44a. Note, however, that whereas in the CE amplifier $C_3$ is grounded and the input signal applied via $C_1$ with the output at $C_2$, in the CB amplifier, $C_1$ is grounded and the input signal is applied at $C_3$. In fact, a CE voltage divider-biased amplifier may be converted to a CB voltage divider-biased amplifier by simply grounding the input capacitor $C_1$, ungrounding $C_3$, and applying the input signal via this capacitor, as shown in Fig. 2.44b.
Example 2.10  Convert the CE amplifier of Example 2.5, shown in Fig. 2.45, to a CB amplifier.

Fig. 2.44  Voltage divider-biased amplifiers. (a) Common emitter; (b) common base

Fig. 2.45  Circuit for Example 2.10
Solution  By grounding the input terminal at input capacitor $C_1$, ungrounding decoupling capacitor $C_2$ and applying the input signal at this ungrounded terminal, the CE amplifier of Fig. 2.45 has been converted to a CB amplifier in Fig. 2.46.

![Diagram](image)

*Fig. 2.46* Solution for Example 2.10

It therefore follows that the design procedure developed for the voltage divider-biased CE amplifier is directly applicable to the voltage divider-biased CB amplifier.

**Example 2.11**  Design a voltage divider-biased CB amplifier using a 20 V supply and an NPN silicon transistor having $\beta = 125$.

**Solution**  Using the circuit in Fig. 2.44b and following the procedure outlined for the CE case, choose $I_{Cq} = 1$ mA. Then, $V_{RE} = 20/10 = 2$ V. Hence, $R_E = 2/1$ mA = 2 k. For maximum symmetrical swing,
\[ V_{CEq} = V_{RL} = (20 - 2)/2 = 9\text{V}. \] Therefore, \( R_L = 9/1 \text{ mA} = 9 \text{ k}. \) Now,
\[ V_{Bq} = V_{Re} + V_{BEq} = 2.7\text{V} \text{ and } I_R = I_{Cq}/10 = 0.1 \text{ mA}. \] Hence, \( R_2 = 2.7/0.1 \text{ mA} = 27 \text{ k} \) and \( R_1 = (20 - 2.7)/0.1 \text{ mA} = 173 \text{ k}. \) Choose \( C_1, C_2, \) and \( C_3 \) large, say 100 \( \mu\text{F}. \)

The results of this circuit under test are shown in Fig. 2.47, where waveforms of the input and output voltage are shown. Before discussing the operation of the circuit, two points relating to the biasing technique must be made. Firstly, the emitter voltage, unlike the CE amplifier, is not fixed; it varies according to \( V_i \). However, this change is generally small (of the order of hundreds of mV) as compared to the changes in the collector voltage, and therefore maximum symmetrical swing calculations, which assume fixed \( V_E \), are still approximately correct. Secondly, in the CE design, in order to prevent loading down the input signal, \( R_1 \) and \( R_2 \) could not be too low. In this configuration, this restriction is removed since there is no signal input at the base of the transistor so that \( I_R \) may be made larger than \( I_C/10 \) in order to improve the bias stabilizing action of the circuit. However, note that an increased \( I_R \) represents an increased demand on the circuit power supply.
Example 2.12  Improve the bias stability in the CB amplifier in Example 2.11.

Solution  For this circuit, $V_{Bq} = V_{RE} + V_{BEq} = 2.7V$. Since there is no signal input at the transistor base, a higher current $I_R$ through $R_1$ and $R_2$ is permissible since the associated lower values of $R_1$ and $R_2$ can be accommodated. Hence choose $I_R = I_{Cq}/2 = 0.5$ mA. This value is five times higher than the value used before but is not so high as to increase the current drain on the system power supply unduly. Hence, $R_2 = 2.7/0.5$ mA $= 5.4$ k and $R_1 = (20 - 2.7)/0.5$ mA $= 34.6$ k.

Regarding the operation of the circuit, note that the capacitor $C_1$ grounds the base of the transistor for signals so that the input signal appears directly across the emitter–base junction. As $V_i$ goes positive, the emitter–base voltage of the BJT is reduced, and this results in a reduction of the transistor collector current. The voltage drop across $R_L$ is therefore reduced resulting in an increase in the collector voltage of
the BJT, i.e., $V_o$ goes positive. As $V_i$ goes negative, the emitter–base voltage of the BJT is increased, and this results in an increase in $I_C$. The voltage across $R_L$ increases, and hence, the collector voltage of the BJT goes down, i.e., $V_o$ goes negative. The overall result is that $V_i$ and $V_o$ are in phase and there is no phase inversion of the voltage as occurs in the CE amplifier.

Let us now evaluate the voltage gain $A_V$, which using Eq. (2.31), is given by.

$$A_V = \frac{V_o}{V_i} = \frac{\Delta I_C R_L}{\Delta V_{EB}} = 40 I_C R_L = g_m R_L$$  \hspace{1cm} (2.50)$$

where $g_m = 40 I_C$. Thus, the voltage gain of the CB circuit is the same as that of the CE circuit, given in Eq. (2.31) except there is no inversion. The input impedance $Z_i$ at the emitter of the CB amplifier is the ratio of the input voltage change ($\Delta V_{EB}$) to the corresponding input current change ($\Delta I_E$) flowing into the emitter. It is given by.

$$Z_i = \frac{\Delta V_{EB}}{\Delta I_E}$$  \hspace{1cm} (2.51)$$

Noting that $\Delta I_E \approx \Delta I_C$ and from Eq. (2.30):

$$Z_i = \frac{\Delta V_{EB}}{\Delta I_E} = \frac{1}{g_m} = \frac{1}{40 I_C}$$  \hspace{1cm} (2.52)$$

Thus, the input impedance of the CB circuit is a factor $\beta$ lower than that of the CE configuration given in (2.32).

**Example 2.13** For the circuit of Example 2.11, find the voltage gain and the input impedance.

**Solution**

$$A_V = 40 I_C R_L = 40 \times 1 \times 9 \text{ k} = 360 \text{ and } Z_i = \frac{1}{40 I_C} = \frac{1}{40 \times 1 \times 10^{-3}} = 25 \Omega.$$  

As is evident, the input impedance of the CB configuration is quite low.
2.5.2 Constant Current or Fixed Bias

The CB amplifier using constant current or fixed bias is shown in Fig. 2.48. This circuit is slightly different from the CE fixed-bias circuit because of the presence of $R_E$ which improves the bias stability of the CB circuit. An example illustrating the design procedure follows.

![Fixed-bias common base amplifier](image)

**Example 2.14** Design a CB amplifier using fixed bias and a silicon NPN transistor having $\beta = 100$. Use $V_{CC} = 22$ V.

**Solution** Following the procedure outlined for the CE case, choose $I_{Cq} = 1$ mA. Then, $V_{RE} = 22/10 = 2.2$ V. Use $V_{RE} = 2$ V. Therefore $R_E = 2/1$ mA = 2 k. For maximum symmetrical swing, $V_{CEq} = V_{RL} = (22 - 2)/2 = 10$ V. Therefore, $R_L = 10/1$ mA = 10 k. Now $V_{CC} = I_BR_B + V_{RE} + V_{BEq}$ giving
\[ I_C R_B / \beta = V_{CC} - V_{BEq} - V_{RE} = 22 - 0.7 - 2 = 19.3 \text{ volts}. \] Hence \( R_B = 19.3 \times 100/1 \text{ mA} = 1.93 \text{ M}. \) Choose \( C_1, C_3, \) and \( C_2 \) large, say 100 \( \mu \)F.

### 2.5.3 Biasing Using a Bipolar Supply

Once again it is possible to convert the CE amplifier using bipolar supplies, shown in Fig. 2.41, to a CB configuration by grounding the input capacitor \( C_1 \) and applying the input signal to an ungrounded capacitor \( C_3 \), as shown in Fig. 2.49. The output is taken from capacitor \( C_2 \). In this case, both base resistor \( R_B \) and capacitor \( C_1 \) can be completely removed and the transistor base terminal directly grounded.

![Common base amplifier with bipolar supply](image)

**Fig. 2.49** Common base amplifier with bipolar supply

**Example 2.15** Using the configuration, shown in Fig. 2.49, design a CB amplifier to operate from a ± 18 V supply. Determine (i) the voltage gain
and (ii) input impedance of the circuit.

**Solution**  Let the collector current be 2 mA. Since the transistor base is at ground potential, it follows that the voltage at the transistor emitter is \(-0.7 \text{ V}\). Hence \(R_E = (-0.7 - (-18))/2 \text{ mA} = 8.7k\). The voltage swing available at the collector of the transistor is approximately 18 V since the emitter voltage experiences only small variations due to the signal. Therefore, for maximum symmetrical swing, \(RL = \frac{18/2}{mA} = 4.5\ k\).

Capacitors \(C_2\) and \(C_3\) are chosen to be large for a good low-frequency response. Voltage gain is given by \(AV = +40ICR_L = 40 \times 2 \text{ mA} \times 4.5k = 360\). Input impedance is given by \(Z_i = 1/40IC = 1/40 \times 2 \text{ mA} = 12.5\ \Omega\).

### 2.6 Common Collector Amplifier

The CC amplifier is shown in Fig. 2.50. This is the third configuration in which the BJT can be used, and this too needs to be biased in order for a complete signal cycle to be reproduced. Once again, a battery \(V_{BB}\) is used to establish a quiescent collector current in the transistor before an input signal is applied. This biasing arrangement is shown in Fig. 2.51.
Fig. 2.50  Common collector amplifier
The signal input $V_i$ then causes changes in this current such that a voltage change appears across resistor $R_E$. Similar to the CE and CB circuits, this approach allows DC to flow through the signal source. Some of the biasing techniques employed in the CE and CB designs are applicable here but with some modifications.

2.6.1 Voltage Divider Biasing

Voltage divider biasing applied to the CC configuration is shown in Fig. 2.52. $R_1$ and $R_2$ fix the base voltage, and $R_E$ provides current stabilizing action (feedback). Note that there is no collector resistor; the transistor collector is connected directly to the supply. It is therefore effectively grounded for signals through the DC supply. Signal input is applied at the base and output is taken at the emitter. A simple design procedure is outlined:
1. Choose $V_{CC}$ and $I_{Cq}$. $V_{CC}$ may depend on the available supply. $I_{Cq}$ is influenced by the load that this circuit must drive and is usually in the range of 1–10 mA.

2. For maximum symmetrical swing, $V_{Eq} = V_{CC}/2$ giving $R_E = V_{CC}/2I_{Cq}$.

3. Choose $I_R = I_C/10$ in order to minimize changes in $I_C$ due to changes in $\beta$. Then, $R_2 = V_{Bq}/I_R$ and $R_1 = (V_{CC} - V_{Bq})/I_R$ where $V_{Bq} = V_{CC}/2 + V_{BE}$.

4. Choose $C_1$ and $C_2$ large.

---

**Example 2.16**  Design a CC voltage divider-biased amplifier using an 18V power supply and an NPN silicon transistor with $\beta = 100$.

**Solution**  Choose $I_{Cq} = 2$ mA and $V_{RE} = 18/2 = 9$ V. Then, $R_E = 9/2$ mA = 4.5 k. Choose $I_R = 2/10 = 0.2$ mA. Then $R_2 = (9 + 0.7)/0.2$
mA = 48.5 k and $R_1 = (18 - 9.7)/0.2 mA = 41.5 k$. Choose $C_1$ and $C_2$ large, say 100 μF.

In this circuit, $V_o$ is in phase with $V_i$. In fact, since $V_{BE}$ is approximately fixed, this results in $V_o \approx V_i$. As a result, this circuit is sometimes referred to as an emitter follower since the emitter follows the input. From circuit theory, the output impedance $Z_o$ of this circuit can be found by short-circuiting the input and applying a voltage $V$ and measuring the corresponding current $I$ at the output, as shown in Fig. 2.53.

![Circuit Diagram](image)

**Fig. 2.53** Output impedance of common collector amplifier

Hence

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}} |_{I_B \text{constant}}$$

(2.53)

Since $\Delta I_E \approx \Delta I_C$, this reduces to

(2.54)
\[
Z_o = \frac{\Delta V_{EB}}{\Delta I_C}
\]

From Eq. (2.30), \( \frac{\Delta I_C}{\Delta V_{BE}} = g_m \). Therefore:

\[
Z_o = \frac{\Delta V_{EB}}{\Delta I_C} = \frac{1}{g_m}
\]  \hspace{1cm} (2.55)

**Example 2.17** Find the output impedance of a CC amplifier in which the collector current is 1 mA.

**Solution** For \( I_C = 1 \) mA, \( Z_o = 1/40 I_C = 25 \) Ω.

Thus, the output impedance of the CC amplifier with low source impedance at the input is quite low. The input impedance is given by

\[
Z_i = \frac{V_i}{I_i}
\]

where \( I_i \) is the input current. Now ignoring for the moment, the two bias resistors \( R_1 \) and \( R_2 \):

\[
V_i = \Delta V_{BE} + I_i (1 + \beta) R_E
\]  \hspace{1cm} (2.56)

\[
Z_i = \frac{V_i}{I_i} = (1 + \beta) R_E + \frac{\Delta V_{BE}}{I_i}
\]  \hspace{1cm} (2.57)

But from (2.32), \( \Delta V_{BE}/I_B = \beta/g_m = \beta/40I_C \). Hence:

\[
Z_i = \beta/40I_C + (1 + \beta) R_E
\]  \hspace{1cm} (2.58)

This input impedance is high because the second term is quite high. The value is however reduced by resistors \( R_1 \) and \( R_2 \) which are effectively in parallel with \( Z_i \).

**Example 2.18** Determine the input impedance for the CC circuit in Example 2.16.

**Solution** For that circuit, \( Z_i = \beta/40I_C + (1 + \beta) R_E = 100/40 \times 2 \times 10^{-3} + (1 + 100) \times 4.5 \times 10^3 \). This reduces to
\[ Z_i = (1.25 + 454.5) \times 10^3 = 455.8 \text{ k} \. \text{This value is in parallel with resistors}\]
\[ R_1 = 41.5 \text{ k} \text{ and } R_2 = 48.5 \text{ k} \text{ and hence is reduced.}\]

### 2.6.2 Constant Current or Fixed Biasing

Constant current or fixed biasing applied to the CC configuration is shown in Fig. 2.54 where, as before, \( R_B \) supplies the base current. However, the presence of \( R_E \) improves the stability of the bias as it provides feedback to the emitter. A simple design procedure is the following:

1. Choose \( V_{CC} \) and \( I_{Cq} \), the latter depending on load requirements.
2. For maximum symmetrical swing, \( V_{CEq} = V_{CC}/2 \). Hence \( R_E = \frac{V_{CC}}{2I_{Cq}} \).
3. \( R_B = \frac{V_{CC} - V_{BEq}}{I_C/\beta} \) where \( V_{BEq} = \frac{1}{2}V_{CC} + 0.7 \).
4. Choose \( C_1 \) and \( C_2 \) large.
Example 2.19  Design a CC fixed-bias amplifier using a 12 V supply and a general-purpose NPN silicon transistor having $\beta = 150$.

Solution  Choose $I_{Cq} = 2$ mA. Then for maximum symmetrical swing, $V_{Eq} = 12/2 = 6$ V. Hence, $R_E = 6/2$ mA = 3 k and $R_B = 6.7/(2 \text{mA}/150) = 502.5$ k.

$Z_o = 1/g_m = 1/40I_C = 12.5$ $\Omega$. Choose $C_1$ and $C_2$ equal 47 $\mu$F. The input impedance is given by $Z_i = (1 + 150) 3 \text{ k} + \frac{150}{40 \times 2 \times 10^{-3}} = 453$ k. The actual input impedance is obtained by placing $Z_i$ in parallel with $R_B$ giving 453 k//502 k.

The CC amplifier with its high input impedance and low output impedance is excellent for serving as a buffer where a high-impedance source must drive a low-impedance load. However, when a load $R_L$ is connected, the peak-to-peak output voltage swing of the amplifier is
reduced on the negative half-cycle for an NPN (and the positive half-cycle for a PNP transistor). For the circuit shown in Fig. 2.55, on the positive half-cycle, the transistor supplies current to the load, and the peak output current is limited only by the power supply. On the negative half-cycle however, the transistor must sink and not source current and the current flowing in from $R_L$ and must be sunk by $R_E$. As this occurs, the transistor must progressively turn off since this current is now being supplied by $R_L$. Eventually, when the transistor is completely off, the maximum current flows in from $R_L$. To determine the maximum value of the peak negative swing at the output at this time, we first note that the DC voltage $V_C$ across the output coupling capacitor $C_2$ is $V_C = I_{Cq}R_E$ since no DC flows in $R_L$. Therefore, when the transistor is cut-off on the negative half-cycle, the capacitor voltage is dropped across $R_E$ and the load $R_L$, and this results in a load current $I_L$ out of the load $R_L$ and into $R_E$ of:

$$I_L = \frac{V_C}{R_E + R_L} = \frac{I_{Cq}R_E}{R_E + R_L}$$  \hspace{1cm} (2.59)
The peak negative output voltage is hence:

\[ V_o^- = I_L R_L = I_{Cq} \frac{R_E R_L}{R_E + R_L} \]  

which can be written as.

\[ V_o^- = I_{Cq} R_E \parallel R_L \]  

If we use \( V_{CEq} = V_{CC}/2 \), then:

\[ I_{Cq} = \frac{V_{CC}/2}{R_E} \]  

giving \( V_o = \frac{V_{CC}}{2} \cdot \frac{R_L}{R_E + R_L} \). In order to maximize \( V_o \), \( R_E \) should be made as small as is practicable so that \( R_L/(R_E + R_L) \rightarrow 1 \). Note, however from
(2.62), that this increases the quiescent current in the transistor. A better approach is to replace $R_E$ with a constant current source. This will be discussed in Chap. 5.

### 2.6.3 Biasing Using a Bipolar Supply

Biasing of the CC amplifier using a bipolar supply is shown in Fig. 2.56. Here the emitter is connected to the negative supply through resistor $R_E$, while the base bias is supplied via resistor $R_B$ which is connected to the ground. $C_1$ and $C_2$ are the usual input and output coupling capacitors. Note that the use of a bipolar supply in this configuration with the transistor base held at an approximately zero potential ensures that the output at the emitter is biased for maximum symmetrical swing and permits a greater output voltage swing since the emitter can approach the positive and negative supply voltages.

![Common collector amplifier with bipolar supply](image)

**Fig. 2.56** Common collector amplifier with bipolar supply

**Example 2.20** Design a CC amplifier using a bipolar supply $\pm12$ V and a general-purpose NPN silicon transistor having $\beta = 150$. 
Solution Choose $I_{eq} = 5$ mA in order to drive external loads. Then $R_E = (0.7 - (-12))/5$ mA = 2.3 k. Choose $R_B = 20$ k.

2.7 Transistor Operating Limits and Specifications

Each transistor has a region of operation in which it can function safely. This region is called the *safe operating area* (SOA) and is illustrated in the (CE) output characteristic of Fig. 2.57. The maximum collector current $I_{C_{\text{max}}}$ that a transistor can carry is set by the current-carrying capacity of the fine wire used to connect the semiconductor regions to the terminal loads. Excessive current will melt these wires resulting in an open circuit at one or more of the device terminals. It is usually referred to as continuous collector current. The maximum collector–emitter voltage $V_{CEO}$ is the maximum voltage that can be applied between the collector and emitter terminals of the transistor when the base terminal is open circuited. It is governed by the process of avalanche breakdown. In fact, beyond $V_{CEO}$ of Fig. 2.57 is a region referred to as the *breakdown region*, which represents catastrophic failure of the transistor. The vertical line on the characteristic corresponds to $V_{CE_{\text{sat}}}$ which is the minimum allowed collector–emitter voltage of BJT if it is not to enter the nonlinear *saturation region*. There is also the parameter $V_{CBO}$ which is the maximum voltage that can be applied between the collector and base terminals when the emitter is open-circuited.
The approximate horizontal line near the $V_{CE}$ axis corresponds to $I_{CEO}$, which is the leakage current. The region beneath this line is the cutoff region that must also be avoided during (linear) amplifier operation. The maximum power dissipation $P_{D\text{max}}$ in the transistor is given by

$$P_{D\text{max}} = V_{CE}I_C$$

(2.63)

This is the equation of a hyperbola that completes the boundary of the SOA. It is especially important in power transistors where considerable power is dissipated during operation. Any rise in temperature of the device results in a movement of the hyperbola toward the origin. The effect is a reduction of the SOA with a temperature increase. Appropriate strategies to mitigate these effects must be introduced in utilizing power transistors, the main strategy being the mounting of the power transistor on a heatsink. This is fully discussed in Chap. 10, which is based on power amplifiers. Finally, the
parameter \( f_T \) (sometimes referred to as the gain/bandwidth product) is the frequency at which the current gain \( h_{fe} \) of the transistor falls to unity. It gives an indication of the transistor performance at high frequencies.

2.8 Applications

In this section, several simple circuit implementations using BJTs are discussed. These are intended to enable the design of actual working circuits using BJTs.

2.8.1 Microphone Preamplifier 1

A preamplifier is an amplifier that increases the amplitude of a low-level signal such that it can drive a power amplifier. The circuit in Fig. 2.58 provides amplification for a dynamic microphone using a 9V battery. Such microphones operate on the principle of electromagnetic induction and provide a nominal output of the order of 2 mV at a low output impedance. The transistor employs collector–base feedback biasing and a collector current of 2 mA. Using the design procedure for collector–base feedback biasing, the value of \( R_L \) for maximum symmetrical swing is given by

\[
R_L = \frac{(9/2) \text{ mA}}{2 \text{ mA}} = 2.25 \text{ k}.
\]

Using a current gain of 100 for the 2N3904 transistor, the feedback resistor \( R_B \) is given by

\[
R_B = \frac{(4.5 - 0.7)}{100} \frac{\text{mA}}{100} = 190 \text{ k}.
\]

The coupling capacitors \( C_1 \) and \( C_2 \) are about 10 \( \mu \)F. The circuit provides a gain of better than 100 which when converted to decibels is 20 log 100 = 40 dB. This means the output from the amplifier is greater than 200 mV, which is sufficient to drive a power amplifier. An interesting point here is that the low output impedance of the microphone reduces the effect of the feedback via \( R_B \) on the signal and hence allows for a higher gain without the need for splitting \( R_B \) and connecting a capacitor to the ground.
Ideas for Exploration: (i) Use a loudspeaker with an impedance of 4–16 Ω to replace the dynamic microphone at the input. This device, like the dynamic microphone, operates on the principle of electromagnetic induction. While the microphone converts sound energy to an electrical signal, the loudspeaker converts an electrical signal to sound. However, its role is reversed here so that it is used as a microphone where it converts sound to an electrical signal which is connected to the input of the preamplifier. (ii) Use an electret microphone to replace the dynamic microphone. An electret or condenser microphone requires external power being fed through a resistor for its operation, as shown in Fig. 2.59. The output signal is coupled to the input of the preamplifier. Because of the voltage at the output of this microphone, a nonpolarized coupling capacitor should be used at the input of the preamplifier.
2.8.2 Microphone Preamplifier 2

Another dynamic microphone preamplifier is shown in Fig. 2.60. It comprises a CE amplifier using a small-signal transistor. Using the design technique developed in this chapter, resistors $R_1 = 73 \, k$ and $R_2 = 17 \, k$ set the base voltage of $Tr_1$ to about 1.7 V. This along with $R_3 = 1 \, k$ establishes a quiescent current of 1 mA. Biasing $Tr_1$ for maximum symmetrical swing requires that resistor $R_4 = 4 \, k$. The capacitor values are large, $C_1 = C_2 = 10 \, \mu F$, $C_3 = 100 \, \mu F$, to allow adequate low-frequency response.
Ideas for Exploration: (i) Use a loudspeaker with an impedance of 4–16 Ω to replace the dynamic microphone. (ii) Use an electret microphone to replace the dynamic microphone. Again, because of the voltage at the output of this microphone, a nonpolarized coupling capacitor should be used at the input of the preamplifier.

2.8.3 Speaker Protection Circuit
The circuit in Fig. 2.61 protects speakers at turn on from the DC that may exist at the output of a power amplifier. It consists of a small-signal NPN transistor such as the 2N3904 connected as an emitter follower. The input to the emitter follower is driven by the voltage across a capacitor $C_2$ whose potential increases at turn on because of charge current flowing in through resistor $VR_1$. The output at the emitter of the transistor drives a relay coil the contacts of which connect the speaker to the output of the amplifier. The supply voltage for the circuit is derived from the supply voltage of the amplifier. Upon turn on of the amplifier, capacitor $C_2$ charges up via potentiometer $VR_1$. Depending on
the adjusted value of $VR_1$, the time for the capacitor to charge is sufficient to allow the output of the amplifier to stabilize. Values of $C_2 = 100 \mu F$ and $VR_1 = 50 \, k\Omega$ will provide a charge time of the order of $VR_1 \times C_2 = 50 \times 10^3 \times 100 \times 10^{-6} = 5 \, s$. When the capacitor voltage attains a value of about 9 V, the relay is activated, and the contacts connect the speaker to the amplifier output. The extent of the delay can be adjusted by varying the potentiometer. Diode $D_1$ which can be an IN4001 diode protects the transistor from back voltages induced in the relay coil, while capacitor $C_1$ provides nominal filtering to the system supply voltage. A value of about 0.1 $\mu F$ is suitable.

![Speaker protection circuit](image)

*Fig. 2.61* Speaker protection circuit

**Ideas for Exploration:** (i) Redesign the system using a 2N3904 PNP small-signal transistor. This would require reversal of the polarity of the power supply. (ii) Investigate the action of the diode in protecting the transistor.

### 2.8.4 Bench Power Supply
Figure 2.62 provides a fixed output of about 9 V and a maximum current of about 250 mA. It uses a Zener diode regulator and boosts the current output with a transistor in emitter follower configuration. In order to ensure that sufficient voltage is available to deliver current to the associated Zener, a basic full-wave rectifier using a 12 V transformer, a diode bridge comprising from $D_1$ to $D_4$, and a filter capacitor $C_1 = 1000 \mu\text{F}$ provides the unregulated input. The peak voltage on the filter capacitor is $12\sqrt{2} - 0.7 = 16.3$ V. The maximum peak-to-peak ripple across the capacitor is given by

$$\Delta V = I/2fC = 100 \times 10^{-3}/2 \times 60 \times 1000 \times 10^{-6} = 0.8 \text{ V}$$

providing a minimum unregulated voltage of $15.6 - 0.8 = 14.8$ V. Using an 8.2V Zener in series with a red LED (light-emitting diode) as an on-indicator with a forward voltage of 1.8 V, the total voltage across the series arrangement is $8.2 + 1.8 = 10$ V. The voltage output at the emitter of the transistor would be 10 V less the 0.7 V of the transistor base-emitter junction giving about 9.3 V. For a Zener operating current of 10 mA, resistor $R_1$ is given by $(14.8 - 10)/10 \text{ mA} = 480 \Omega$. The 2N3055 power transistor boosts the current output capacity of the Zener diode by the factor of the current gain of the transistor which, for a 2N3055, is about 50. The maximum current available is calculated using the minimum allowable current for the Zener which is about 5 mA. Hence the available current from the Zener regulator is $10 - 5 = 5$ mA, and therefore the maximum output current is $5 \text{ mA} \times \beta = 5 \text{ mA} \times 50 = 250$ mA where $\beta = 50$ is the current gain of the transistor. The fuse provides short-circuit protection.
**Ideas for Exploration:** (i) Modify the system to produce a variable bench supply by introducing a 10-k potentiometer across the series LED-Zener arrangement and connecting the wiper of the potentiometer to the transistor base. Identify any problems with this arrangement. (ii) Use a transistor with a higher gain and explain if this provides any performance improvement. (iii) Utilize the TL431A programmable Zener introduced in Chap. 1 to design the supply instead of the Zener diode.

### 2.8.5 Electronic Fuse

This circuit adds electronic over-current protection to the bench supply just discussed. It consists of a small-signal NPN silicon transistor $T_{r2}$ with a resistor $R_2$ between the base and emitter of the transistor. The arrangement is connected to the supply, as shown in Fig. 2.63. As increased load current flows through $R_2$, the voltage drop across this resistor increases. When this value equals 0.7 V, transistor $T_{r2}$ turns on drawing current away from the base of transistor $T_{r1}$, thereby causing the supply current to remain approximately constant. Any further small increase in the load current further turns on $T_{r2}$, and this reduces the current to the Zener. The effect is that the Zener voltage falls and a constant voltage supply becomes a constant current supply. Then, $R_2 = 0.7/I_{L_{mx}}$ where $I_{L_{mx}}$ is the maximum load current.

![Electronic Fuse Circuit](image)
**Ideas for Exploration:** (i) Plot the voltage–current characteristic for the modified bench supply circuit to show the effect of the electronic fuse. (ii) Introduce a small capacitor across the output of the supply to improve filtering.

### 2.8.6 Blown Fuse Indicator

This circuit gives a visual indication when a protection fuse is blown. It is placed between the power supply and the circuit being protected and comprises a PNP transistor arranged, as shown in Fig. 2.64. During normal operation with a continuous fuse, the voltage across the base–emitter junction of the transistor is approximately zero. The transistor is therefore off and the LED does not light. If the fuse is blown because of an overcurrent, then voltage drop across the base–emitter junction causes $Tr_1$ to turn on. Current thereby flows through the LED which now turns on. When $Tr_1$ is on, the full supply voltage is dropped across the LED and resistor. Thus, for a 24 V supply and allowing an (red) LED voltage of 1.8 V and a current of 10 mA, $R_3 = (24 - 1.8)/10 \text{ mA} = 2.2 \text{ k}\Omega$. Assuming a transistor current gain of 100, the base current of $Tr_1$ is given by $10 \text{ mA}/100 = 0.1 \text{ mA}$, and this flows through $R_1$ and $R_2$. Hence, $R_1 + R_2 = (24 - 0.7)/0.1 \text{ mA} = 233 \text{ k}\Omega$. To ensure transistor saturation, use 200 k. Then noting that $R_2$ is a load on the supply, set $R_1 = R_2 = 100 \text{ k}\Omega$. 
Ideas for Exploration: (i) Introduce a green LED in series with resistor $R_2$. During normal operation, there would be sufficient current through this resistor to turn this LED on but it goes off when the fuse is blown. This would complement the action of the red LED.

2.8.7 Telephone Monitor

This circuit shown in Fig. 2.65 turns on an LED when the telephone handset is lifted indicating that the telephone is in use. The diode bridge ensures that the DC signal into the transistor from the telephone line is always of the same polarity. When the telephone is on hook, the telephone circuit is open, and 48 V available from the telephone exchange will be across tip (T) and ring (R). At this time since the emitter of the transistor is at $V_{CC}$, the resistor values $R_1$, $R_2$, and $R_3$ must be chosen such that the voltage at the base of the transistor is greater than $V_{CC} - 0.7$ V to ensure that the transistor is off. The LED would therefore not be illuminated. When the handset is lifted, the telephone circuit is closed, and as a result of line resistance, the voltage across the tip and ring will drop. With suitable values for resistors $R_1$, $R_2$, and $R_3$, the voltage at the base of the transistor will drop to a value such that the
voltage across the base–emitter junction of the transistor exceeds 0.7 V, thereby turning on the transistor and illuminating the LED. Thus, for $V_{CC} = 3 \text{ V}$, $R_1 = 470 \text{ k}$, $R_2 = 1 \text{ M}$, and $R_3 = 100 \text{ k}$, then the voltage at the base of the transistor is given by $\frac{R_3}{R_1+R_2+R_3} \times 48 = 3 \text{ V}$. At this voltage with the emitter voltage also at 3 V, it follows that the base–emitter voltage is zero and the transistor is off. When the phone is lifted off the hook, the telephone circuit is closed. Current flows such that a voltage drop occurs along the line, thereby reducing the 48 V across tip and ring. This reduces the base voltage and causes the transistor to turn on lighting the LED. Resistor $R_4$ limits the current through the LED. A value of about 100 $\Omega$ is suitable.

![Diagram of telephone monitor circuit](image)

**Fig. 2.65** Telephone monitor

*Ideas for Exploration:* (i) Introduce an LED that indicates the on-hook condition.
2.8.8 Audio Mixer

This circuit for an audio mixer in Fig. 2.66 uses a CB amplifier to enable the mixing of signals from several sources. It consists of a CB amplifier in which the transistor base is held at a fixed voltage 1.4 V using two forward-biased diodes in series instead of a voltage divider. This arrangement provides a more stable voltage at the base. Current through these diodes is supplied from a 15 V supply through a resistor $R_5 = 3.3 \, k$. Hence, the current through diodes $D_1$ and $D_2$ is $(15 - 1.4)/3.3 \, k = 4 \, mA$. Capacitor $C_5$ ensures that the transistor base is grounded for signals. Choosing a collector current of 1 mA, then $R_6 = (1.4 - 0.7)/1 \, mA = 700 \, \Omega$. For maximum symmetrical swing, the quiescent voltage across $R_4$ is made equal to the quiescent collector–emitter voltage giving $V_{CE} = V_{R_4} = (15 - 0.7)/2 = 7.2 \, V$. Hence, $R_4 = 7.2/1 \, mA = 7.2 \, k$. Input and output coupling capacitors $C_1$–$C_4$ are chosen to be large values for good low-frequency response. The input impedance at the emitter is $1/40I_C = 1/40 \times 1 \, mA = 25 \, \Omega$ which is quite low. By choosing signal input resistors $R_1$–$R_3$ to be much greater than 25 $\Omega$ say 22 $k$, very good signal mixing occurs at the transistor emitter with very low channel interaction (cross-talk).
Ideas for Exploration: (i) introduce 10 k potentiometers in each input circuit in order to adjust individual channel gain. (ii) Sacrifice maximum symmetrical swing for increased output signal amplitude by increasing the value of resistor $R_4$. (iii) Redesign the circuit using a red or green LED instead of the two signal diodes.

### 2.8.9 Power Zener Diode

The power rating of a Zener diode can be increased by coupling the Zener with a power transistor, as shown in Fig. 2.67. Resistor $R_1$ sets the current through the Zener at $0.7/R_1$. For 1 mA, we get $R_1 = 700 \, \Omega$. The effective Zener voltage $V'_Z$ across the arrangement is $V'_Z = V_Z + 0.7$, which for a 4.3 V Zener gives $V'_Z = 4.3 + 0.7 = 5 \, \text{V}$. While the current through the Zener is 1 mA, the power transistor can allow significantly higher currents, thereby increasing the power rating of the arrangement beyond the power rating of the Zener. For example, if the maximum...
transistor current is 1A, then the power rating of the arrangement becomes approximately \( P_D = 5 \text{ V} \times 1 \text{ A} = 5 \text{ W} \). Note that the base current of the power transistor flows through the Zener in addition to the 1 mA supplied to the resistor, since this latter current is set by the base-emitter voltage of the transistor.

![Power Zener diode diagram](image)

**Fig. 2.67** Power Zener diode

**Ideas for Exploration:** (i) Use this power Zener to design a high-current Zener diode regulator. (ii) Compare this regulator with that providing the bench power supply. Zener regulators are referred to as shunt regulators as the regulating device (Zener) is in parallel with the load, while the earlier regulator in the bench supply is a series regulator since the regulating element (transistor) is in series with the load. (iii) Implement this circuit using a PNP transistor.

### 2.8.10 Adjustable Zener Diode

The voltage specification of a Zener diode can be increased by coupling the Zener with a transistor, as shown in Fig. 2.68. The voltage across resistor \( R_1 \) is \( V_z + 0.7 \), and therefore the current \( I \) through resistor \( R_1 \) is
given by \(I = (V_z + 0.7)/R_1\). Assuming a high-gain transistor, the base current will be small and hence most of \(I\) flows through \(R_2\). Therefore, the effective Zener voltage \(V'_z\) across the arrangement is
\[V'_z = \left(1 + \frac{R_2}{R_1}\right)(V_z + 0.7).\]

Thus using \(R_1 = R_2 = 6.8\, k\) and a 6.8 V Zener gives \(V'_z = (1 + 1)(6.8 + 0.7) = 15\) V. The resulting current through \(R_1\) and \(R_2\) is \(I = 7.5/6.8\, k = 1.1\, mA\). The power rating of the adjusted diode will then be a function of the power rating of the associated transistor. Note that if the Zener is replaced by a short-circuit, the voltage output becomes \(V'_z = \left(1 + \frac{R_2}{R_1}\right)0.7\). This particular circuit arrangement is sometimes referred to as a \(V_{be}\) multiplier or amplified diode (see Chap. 5).

![Fig. 2.68 Adjustable Zener diode](image-url)
Ideas for Exploration: (i) Investigate the use of this adjustable Zener in the design of a variable voltage regulated supply.

2.8.11 Diode Tester
A transistor can be used in the testing of diodes, as shown in Fig. 2.69. The diode to be tested is connected to the base biasing circuit. An LED along with a current limiting resistor is connected to the collector circuit. When a good diode is connected to the test terminals with the correct polarity, conduction through the diode and $R_1$ occurs, and a fraction of the supply voltage is dropped across resistor $R_2$. This turns on $Tr_1$ and hence the LED. If the connection is reversed, the diode becomes reverse-biased, and no conduction occurs. As a result, no bias voltage is dropped across $R_2$, and therefore the transistor remains off. The LED $D_1$ does not light. An open diode will cause no conduction with both the connections and there will be no lighting of the LED. A shorted diode will cause conduction and LED lighting happens with both connections. The values of $R_1$ and $R_2$ must be chosen such that the transistor is turned on when diode conduction takes place. $R_1 = 10 \text{k}$ and $R_2 = 2.2 \text{k}$ will give a voltage at the transistor base of $2.2 \times 9/(10 + 2.2) = 1.6 \text{V}$. This value is more than sufficient to turn on the transistor and will fall as base current is drawn from the junction of the two resistors. A value for resistor $R_3$ of $1 \text{k}$ will limit the current in the transistor to less than $9 \text{V}/1 \text{k} = 9 \text{mA}$. 
Ideas for Exploration: (i) Investigate the use of the diode tester to check transistors. Noting that a transistor is made up of two back-to-back diodes, it follows that both the base–emitter and base–collector junctions of a transistor should have a low forward resistance and a high reverse resistance, while the collector–emitter terminals should have high resistance in both connections. Both NPN and PNP transistor can be tested but with appropriate polarities.

2.8.12 Dry Soil Indicator

The circuit in Fig. 2.70 functions as a dry soil detector. The two leads connected to the base and emitter terminals of the transistor are placed in the soil whose moisture level is to be monitored. If the water level is sufficient, the resistance between the two probes will be low. As a result, the voltage drop across the base–emitter junction is insufficient to turn
on the transistor, most of the supply voltage is dropped across resistor $R_1$. As the soil becomes dry, the soil resistance will increase, and hence the voltage drop across the base–emitter junction will eventually be sufficient to turn on the transistor. The LED $D_1$ in the collector circuit will therefore turn on. Some experimentation may be necessary to determine a suitable value for $R_1$. A reasonable value to start with is $R_1 = 220 \text{k}$. Since the supply voltage is only 3 V, a current limiting resistor in series with the LED may not be necessary.

![Dry soil indicator](image)

*Fig. 2.70* Dry soil indicator

*Ideas for Exploration*: (i) Try the circuit with different types of soil.

### 2.8.13 Lie Detector

A lie detector is an instrument that measures changes in body characteristics, such as skin resistance in an attempt to detect when an individual is telling a lie. It is based on the idea that skin resistance changes with emotional state, particularly as a result of perspiring. This resistance change can be easily detected and used as an indicator of lying. The lie detector circuit, shown in Fig. 2.71, utilizes a transistor $Tr_1$ with a milliammeter in the collector circuit. The probes are connected to the collector and base terminals and held firmly in both hands by the candidate under test. Under normal conditions, the body resistance will allow a level of base current to flow. This is amplified by the transistor...
giving a collector current that is measured by the milliammeter. Upon questioning, if the candidate lies, the body resistance may fall resulting in an increased base current and hence a corresponding increase in collector current. This increase is measured by the meter and may be an indication that the individual may be lying. Almost any small-signal NPN transistor such as the 2N3904 can be used. The resistor $R_1 = 1 \, k$ in series with the milliammeter limits the current to less than $9 \, mA$ in the event that the probes are short-circuited. Note however that since $R_1$ is in the collector circuit, it has very little influence on the collector current. When in use, the range of the meter should be adjusted to accommodate the resulting current.

![Diagram of Lie detector](image)

**Fig. 2.71** Lie detector

**Ideas for Exploration:** (i) Experiment with various individuals to evaluate the effectiveness of the circuit. (ii) Research other body characteristics used in lie detection including breathing rate, pulse rate, and blood pressure.

**2.8.14 Research Project 1**

This project involves the use of the transistor to improve the performance of the simple radio receiver in Fig. 1.71 of Chap. 1. The circuit is shown in Fig. 2.72. Here the output of the crystal diode $D_1$ is amplified by the single transistor amplifier stage $Tr_1$, thereby increasing the sensitivity of the receiver. The design procedure follows that given in this chapter. The output of the amplifier drives the piezoelectric
earphones. A capacitor $C_1 = 330pF$ is included to ensure the proper filtering of the signal after rectification by the diode. Resistor $R_1 = 10k$ is again required for proper circuit operation.

![Improved crystal radio circuit diagram](image)

**Fig. 2.72** Improved crystal radio

**Ideas for Exploration:** (i) Connect the transistor as shown in Fig. 2.73. Here the base–emitter junction of a germanium transistor $Tr_1$ such as the NTE101 replaces the germanium diode to produce signal demodulation. The output of the tank circuit drives the base of the transistor while the signal output at the emitter drives the piezoelectric earphone. The additional feature of this circuit compared to that of Chap. 1 is that the collector of the transistor is powered by a 9 V battery. Thus, when a radio signal from the tank circuit turns on the base–emitter junction, the signal current into the transistor base is amplified by the factor $\beta$ of the transistor. The effect is less loading of the tank circuit and hence greater frequency selectivity and increased signal output. Resistor $R_1 \approx 10k$ is again required for proper circuit operation; (ii) add a single transistor amplifier stage to the circuit of Fig. 2.73.
In this research project, the transistor is used as a high-impedance DC voltmeter (Fig. 2.74). The circuit uses a germanium instead of a silicon transistor $Tr_1$ in the CE mode and realizes a high input impedance of 200 kΩ/V by employing high-value resistors at the transistor base input. Upon application of a voltage at the input through one of these resistors, the transistor amplifies the small input base current, and the resulting larger collector current drives the microammeter $M_1$. The transistor is not biased so that the threshold voltage of the transistor has to be overcome by the input signal for circuit operation. The use of a germanium transistor ensures that this turn on voltage is low (0.3 V). The need to overcome even this low voltage does result in some nonlinearity at low input voltages. Resistors $R_1$–$R_5$ are selected such that the same value of base current flows into the transistor with application of the full voltage on each range. That value of base current would result in the full-scale deflection of the meter. Thus, on the 1 V range for $R_1 = 200$ k, ignoring the 0.3 V turn on voltage, the maximum base

\[ \text{Fig. 2.73 Modified crystal radio} \]
Current is given by $\frac{1 V}{200\ \text{k}} = 5\ \mu\text{A}$. This current is amplified by the transistor current gain of about 60, giving a collector current of 300 $\mu\text{A}$. The sensitivity of the 100 $\mu\text{A}$ meter $M_1$ is adjusted by $VR_1 = 10\ \text{k}$ to realize full-scale deflection for this current. Power supply $B_1$ provides power to the circuit, while supply $B_2$ along with $VR_2 = 100\ \text{k}$ is used to nullify transistor leakage current into the meter. The remaining resistors at the input are selected such that range-voltage/range-resistor = 5 $\mu\text{A}$. This results in $R_2 = 1\ \text{M}, R_3 = 2\ \text{M}, R_4 = 10\ \text{M}$, and $R_5 = 20\ \text{M}$.

![Fig. 2.74 High-impedance DC voltmeter](image)

*Ideas for exploration:* (i) Select $R_6$ to protect the meter from over-voltage. (ii) Determine $C_1$ to remove high-frequency noise from the input signal. (iii) Use a silicon transistor for $Tr_1$ and compare the performance of the circuit with that using a germanium transistor.

*Problems*

1. Design a fixed-bias CE amplifier with a 24 V supply and an NPN silicon transistor having $\beta = 100$. Design for maximum symmetrical swing. Determine the voltage gain and input impedance.

2. Draw the load line for the circuit of problem 1, indicating the q
point. What does the slope of the line represent?

3. Determine the collector current and voltage in the fixed-bias amplifier of Fig. 2.75, assuming transistor current gain of 100. If the transistor is replaced by one with a current gain of 75, determine the new collector current and voltage.

4. Using a DC supply of 15 V, a load resistor of 2 k, and a silicon PNP transistor with $\beta = 150$ at room temperature, (a) bias the transistor for maximum symmetrical swing using fixed bias and (b) calculate the value of $V_{CEq}$ at 50 °C if $\beta$ goes to 110.

5. In the circuit of Fig. 2.76, determine the value of $R_B$ in order to achieve a collector voltage of 10 V, assuming $\beta = 130$. Evaluate the input impedance for the circuit.

6. What are the two main sources of distortion in a CE amplifier? Discuss ways by which this distortion can be minimized.

7. Design a voltage divider-biased CE amplifier for maximum symmetrical swing using a small-signal NPN silicon transistor with a current gain of 120 and a 25 V supply. Justify all the steps in your design. Evaluate the voltage gain of your circuit.

8. In the CE voltage divider-biased-biased amplifier of Fig. 2.77 determines the collector current and the collector voltage.

9. In the CE voltage divider-biased-biased amplifier of Fig. 2.78, using a PNP transistor, determine the collector current, the collector voltage, and the emitter voltage.

10. Design a CE amplifier utilizing current feedback biasing using an NPN silicon transistor having $\beta = 200$ and a 12 V supply.

11. Determine the collector current and voltage for the collector–base feedback circuit shown in Fig. 2.79 assuming $\beta = 100$.

12. Design a CE amplifier using a ± 20 V bipolar supply and a transistor with $\beta = 150$.
Design a voltage divider-biased CB amplifier using a ± 28 V supply.
13. Design a voltage divider-biased CB amplifier using a 20 V supply and an NPN silicon transistor having $\beta = 110$. Find the voltage gain and input impedance of the circuit.

14. Explain the phase relationship between the input and output voltages in a CB amplifier.

15. Design a CB amplifier using fixed bias and a silicon NPN transistor having $\beta = 100$. Use $V_{CC} = 18$ V.

16. Design a CB amplifier using a bipolar supply $\pm20$ V. Determine the voltage gain and input impedance.

17. Design a CB amplifier for maximum symmetrical swing using a small-signal PNP silicon transistor with a current gain of 125 and a 20 V supply. Use a 3.3 V Zener to fix the base voltage. Justify all your design steps. Evaluate the input impedance and voltage gain of your circuit.

18. Design a voltage divider-biased-biased CC amplifier for maximum symmetrical swing using a small-signal PNP silicon transistor with a current gain of 110 and a 22 V supply. Justify all your design steps. Evaluate the input impedance and voltage gain of your circuit.

19. Design a voltage divider-biased-biased CC amplifier for maximum symmetrical swing using a small-signal NPN silicon transistor with a current gain of 125 and a 32 V supply. Justify all your design steps. Determine the input impedance of your circuit.

20. Design a CC fixed-bias amplifier using a 22 V supply and a general-purpose NPN silicon transistor having $\beta = 180$.

21. Evaluate the collector current and voltage in the CB amplifier of Fig. 2.80.

22. Using the configuration of bench supply, design a regulated power supply giving 5 V at 150 mA with electronic short-circuit.
23. Design a CC amplifier using a PNP silicon transistor with a ± 15 V supply.

24. Determine the collector current and voltage in the CC circuit of Fig. 2.81.

Fig. 2.75 Circuit for Question 3
Fig. 2.76  Circuit for Question 5
Fig. 2.77  Circuit for Question 8
Fig. 2.78 Circuit for Question 9
Fig. 2.79  Circuit for Question 11
Fig. 2.80  Circuit for Question 21
Fig. 2.81  Circuit for Question 24

Bibliography


3. Field-Effect Transistor

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The field-effect transistor or FET is a three-terminal semiconductor device that controls an electric current by an electric field. The FET actually predates the bipolar junction transistor (BJT) as the first patent that was granted for such a device in 1928. Its impact on industry however was felt only about a decade after the development of the transistor in 1948. The FET is a unipolar device having only one p–n junction, and it differs from the BJT in several important respects, the main one being the FET’s inherently high input impedance. There are two types of FETs: the junction gate FET (JFET) or JUGFET and the metal oxide semiconductor FET or MOSFET. The MOSFET, sometimes called the insulated gate FET or IGFET, comes in two versions: the depletion MOSFET and the enhancement MOSFET. Because of a difference in construction, the MOSFET has a higher input impedance than the JFET. The FET, like BJT, can provide amplification of a signal and operate as a switch. It is important in many applications and forms the subject of this chapter. At the end of the chapter, the student will be able to:

- Describe and explain the characteristics and operation of the JFET.
- Describe and explain the characteristics and operation of the MOSFET.
- State the various FET amplifier configurations.
3.1 Operation of JFET

The basic structure of a JFET is shown in Fig. 3.1a. The device is a three-terminal device comprising a bar of n-type silicon material forming a channel with a ring of heavily doped p-type material at the center forming a gate. The source (S) and drain (D) are located at each end of the n-type bar, and the gate (G) is connected to the p-type material. This type of JFET is referred to as an n-channel JFET. A p-channel JFET has a channel consisting of p-type material with an n-type gate, and this is shown in Fig. 3.1b. The symbols for n-channel and p-channel JFETS are shown in Fig. 3.2.
Considering the n-channel JFET, for normal operation the drain–source voltage $V_{DS}$ is positive as shown in Fig. 3.3. Majority carriers
enter the bar via the source terminal and leave the bar by way of the drain terminal. The magnitude of this drain current is inversely proportional to the resistance of the bar or wafer (which in turn depends on bar length and cross-sectional area). If, therefore, the cross-sectional area can be varied, then channel resistance and hence drain current can be influenced. From previous considerations, it is known that the region on either side of a p–n junction, known as the depletion region, is a region of high resistivity where width depends on the reverse-biased voltage applied to the junction. Through the action of this depletion layer, the reverse bias can exert control over the channel width and therefore channel current. This reverse bias is applied via the gate–source terminals. The heavy doping of the p-type region ensures that the depletion region remains within the n-channel and does not extend into the p-type region.

When the gate is connected to the source corresponding to zero gate–source voltage and the drain–source voltage $V_{DS}$ is increased...
slowly from zero, the channel behaves like a semiconductor resistor giving an approximately linear increase of current with applied voltage. The p–n junction becomes increasingly reverse-biased, causing the depletion layer to extend further into the channel. The reverse bias arises since the p-type region is at zero potential (relative to source), while the n-channel is progressively positive with increasing distance from the source to the drain. This potential gradient, which exists along the channel, produces an increased reverse bias of the p–n junction such that the width of the depletion region is increased. The region closer to the drain terminal where the potential is higher will be wider than the region closer to the source terminal where the potential is lower. The effect of this on the channel is shown in Fig. 3.4. Hence, increasing the drain–source voltage increases the depletion region and therefore increases channel resistance. The drain current is therefore reduced. Further increase in the drain–source voltage makes the depletion region extend further into the channel.
As a result of the depth of penetration of the depletion region, the width of the depletion region increases as we approach the drain, causing a constriction of the effective channel width. As the drain–source voltage $V_{DS}$ is increased, a point is reached where the drain current remains constant at a value referred to as the saturation drain current with no further increase resulting from an increasing drain–source voltage.

The channel is now said to be “pinched off,” and the FET is operating in the pinch-off or constant current region. Note that in this region, the channel is not closed off completely since this would cause the drain current $I_D$ to go to zero. The drain–source voltage at which pinch-off occurs corresponds in magnitude to what is called the pinch-off voltage $V_p$. If $V_{DS}$ is increased still further, avalanche breakdown will eventually occur as in all p–n junctions. The onset of avalanche breakdown is very rapid and may cause irreparable damage to the junction. The resulting $I_D/V_{DS}$ characteristic is shown in Fig. 3.5.

![Diagram showing the drain current vs drain–source voltage characteristic for a JFET.](image)

**Fig. 3.4** Pinch-off in n-channel JFET

**Fig. 3.5** Drain current vs drain–source voltage characteristic for JFET
The reverse bias at the gate-channel p–n junction can be increased by the application of a negative potential to the gate terminal relative to the source. Thus, instead of $V_{GS} = 0$ as before, the gate is disconnected from the source and a negative bias applied at the gate with respect to the source as shown in Fig. 3.6. This reverse bias widens the existing depletion layer and as a result decreases channel width as well as increases channel resistance, even before $V_{DS}$ is applied. Then as $V_{DS}$ is increased from zero, the decreased channel width means that pinch-off will occur at a lower value of $V_{DS}$ and a lower value of saturation drain current. Further negative increases in $V_{GS}$ result in still lower values of $V_{DS}$ at which pinch-off occurs with correspondingly lower values of saturation drain current. Eventually, at a sufficiently negative gate–source voltage $V_{GS} = -V_p$, pinch-off occurs at zero and all higher values of $V_{DS}$ such that the drain current is zero. The result is a set of characteristics $I_D$ vs $V_{DS}$ with $V_{GS}$ as a varying parameter as shown in Fig. 3.7. They are the n-channel JFET output characteristics.

Fig. 3.6 JFET with negative gate–source voltage
A p-channel junction FET operates in a similar manner except that the drain is driven by a negative potential with respect to the source and it is necessary to increase the gate–source voltage positively in order to reduce the drain current. This device is shown in Fig. 3.8 with the associated pinch-off action in Fig. 3.9 and output characteristics shown in Fig. 3.10. Both the p-channel and n-channel JFETs are operated with their gate-channel p–n junctions reverse-biased. They therefore have very high input impedances of the order of $10^9 \Omega$. 

*Fig. 3.7* n-Channel JFET $I_D$ vs $V_{DS}$ with $V_{GS}$ as a varying parameter
Fig. 3.8  p-Channel JFET in operation
Fig. 3.9 Pinch-off in p-channel JFET

Fig. 3.10 p-Channel JFET $I_D$ vs $V_{DS}$ with $V_{GS}$ as a varying parameter
3.2 JFET Characteristics

JFET output characteristics consist of three distinct regions for any particular value of $V_{GS}$ (Fig. 3.5):

- An approximately linear or Ohmic region.
- An approximately pinch-off or saturation region.
- An avalanche or breakdown region.

The Ohmic region where $V_{DS} < V_P$ is one in which the JFET operates as a voltage-controlled resistor since varying $V_{GS}$ changes the channel resistivity. The pinch-off or saturation region is the region where the drain current is almost completely controlled by the gate–source voltage and is virtually independent of the drain–source voltage. It is in this region that amplifying action is possible. The device is never operated in the breakdown region as catastrophic failure results. These characteristics can be obtained using the circuit shown in Fig. 3.12.

Using power supply $P_1$ and the voltmeter between the gate and source, $V_{GS}$ is set at a specific negative voltage. Using power supply $P_2$ and the voltmeter between the drain and the source, $V_{DS}$ is varied. As $V_{DS}$ is varied, the corresponding value of drain current $I_D$ is recorded using the milliammeter in the drain circuit for various values of $V_{DS}$. This is repeated for various fixed values of $V_{GS}$. The result is a set of drain characteristics for the device.

As indicated earlier, the saturation drain current is the drain current that flows when the JFET is operated in the constant current region beyond pinch-off. The equation that defines the behavior of the JFET is Shockley's equation which is given by

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$  \hspace{1cm} (3.1)

where $I_{DSS}$ is the saturation drain current which flows when the gate–source voltage is zero and $V_P$ is the pinch-off voltage. This equation defines the relationship between the drain current of the JFET and the gate–source voltage. In typical, drain characteristics for the JFET are shown in Fig. 3.11, each curve has a region of small values of $V_{DS}$ in
which \( I_D \) is proportional to \( V_{DS} \). In this region, the device can be operated as a voltage-dependent resistance, i.e. as a resistance whose value \( V_{DS}/I_D \) depends on the value of \( V_{GS} \). Here, the gate–source voltage on the FET determines the channel resistance according to

\[
r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2}
\]  

(3.2)

where \( r_o \) is the channel resistance \( r_d \) with \( V_{GS} = 0 \) V.

**Fig. 3.11** JFET output characteristics

The mutual or transfer characteristic of a JFET is a graph of drain current against gate–source voltage for constant values of drain–source voltage above pinch-off obtained using the circuit of Fig. 3.12. Using power supply \( P_2 \) and the voltmeter between the drain and source, \( V_{DS} \) is set at a specific positive voltage. Using power supply \( P_1 \) and the voltmeter between the gate and the source, \( V_{GS} \) is varied. As \( V_{GS} \) is varied, the corresponding value of drain current \( I_D \) is recorded using the milliammeter in the drain circuit for various values of \( V_{GS} \). This is
repeated for various fixed values of $V_{DS}$. The result is the mutual characteristic for the device.

\[ \text{Fig. 3.12 Circuit for the determination of the characteristics of the n-channel JFET} \]

This curve shows the effect of gate–source voltage directly on saturation drain current and indicates that JFET is a voltage-controlled device. Mutual characteristics for n-channel and p-channel JFETs are shown in Figs. 3.13 and 3.14, respectively. From these curves, it can be seen that for $|V_{DS}| > |V_p|$ where $I_D$ assumes its saturation value, as $V_{GS}$ is changed from zero, the saturation drain current decreases from $I_{DSS}$. At some value $V_{GS} = V_p$, the drain current goes to zero, and this voltage is referred to as the pinch-off voltage for FET. It is negative for n-channel JFETs and positive for p-channel JFETs. Therefore, the pinch-off voltage $V_p$ is defined as that value of p–n junction reverse bias which removes all the free charges from the channel; it is the reverse bias that will cause the depletion regions to pinch off. Now, $V_{DS}$ is set at a value above pinch-off and $V_{GS}$ and the corresponding value of drain current are recorded. There is very little variation in the curve for different values of $V_{DS}$ above pinch-off. On examination of the saturation drain characteristic in Fig. 3.11, it can be seen that as the gate reverse bias is increased, pinch-off occurs at lower values of drain voltage, and at pinch-off, $V_p$ can be approximated by the relation $|V_p| = |V_{DSp}| + |V_{GS}|$ where $V_{DSp}$ is the
drain–source voltage at the point of pinch-off. The values of transconductance and the drain–source resistance can be obtained from the drain characteristics, while the transconductance conductance can be determined from the mutual characteristic.

Fig. 3.13 n-Channel JFET mutual characteristic
3.3 JFET Parameters

The important parameters of a JFET are its mutual conductance $g_m$, its input resistance $R_i$, and its drain–source resistance $r_{DS}$. The mutual conductance or transconductance is defined as the ratio of a change in the drain current $\Delta I_D$ to the change in the gate–source voltage $\Delta V_{GS}$ producing it, with the drain–source voltage $V_{DS}$ held constant, i.e.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} , V_{DS} \text{ constant}$$  \hspace{1cm} (3.3)

As in the BJT, the FET transconductance directly determines the gain of the FET when the device is connected as an amplifier. Typically, $g_m$ has a value in the range 1–10 mA/V and is generally much smaller than that for BJT. Its value can be found graphically using the slope of the mutual characteristic at particular operating conditions or analytically using Shockley’s equation (3.4). Thus, from Shockley’s equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$ \hspace{1cm} (3.4)

Differentiating $I_D$ with respect to $V_{GS}$ gives

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{-2I_{DSS}}{V_P} \left(1 - \frac{V_{GS}}{V_P}\right)$$ \hspace{1cm} (3.5)

Using (3.4), this can be written as

$$g_m = \frac{-2I_{DSS}}{V_P} \sqrt{\frac{I_D}{I_{DSS}}}$$ \hspace{1cm} (3.6)

For $V_{GS} = 0$, (3.5) reduces to

$$g_m = \frac{-2I_{DSS}}{V_P}$$ \hspace{1cm} (3.7)
The input impedance $R_i$ of a JFET is the high value presented by the reverse-biased gate-channel p–n junction. Typically, JFET input impedance is greater than $10^8 \, \text{M}\Omega$. Finally, the drain–source resistance $r_{DS}$ is the ratio of a change in the drain–source voltage $\Delta V_{DS}$ to the corresponding change in drain current $\Delta I_D$, with the gate–source voltage $V_{GS}$ held constant, i.e.

$$r_{DS} = \frac{\Delta V_{DS}}{\Delta I_D}, \quad V_{GS} \text{ constant}$$  \hspace{1cm} (3.8)

$r_{DS}$ may be in the range $40k\Omega\text{−}1M\Omega$ and can be found from the inverse of the slope of the drain characteristic.

**Example 3.1** A JFET has a signal voltage of 1.5 Vpk value applied to its gate relative to its source. The drain current varies by ±2 mA about its quiescent value. Calculate $g_m$.

**Solution** Using (3.3),

$$g_m = \frac{2 \times 10^{-3}}{1.5} = 1.33 \, \text{mA/V}.$$

**Example 3.2** An n-channel JFET has $I_{DSS} = 10 \, \text{mA}$ and $V_P = -8 \, \text{V}$. For a drain current of 5 mA, determine $g_m$.

**Solution** Using (3.6),

$$g_m = \frac{-2 \times 10^{-8}}{-8} \sqrt{\frac{5}{10}} = 1.77 \, \text{mA/V}.$$

### 3.4 Using the JFET as an Amplifier

Like the BJT, the JFET can be operated in three configurations, the common source, common gate, and common drain configurations, as shown in Fig. 3.15.
3.4.1 Common Source Configuration

This configuration is shown in Fig. 3.15a. It is the most frequently used amplifying configuration among FETs and is fundamental to the FET amplifying action. The input signal is applied at the gate terminal of the FET relative to the grounded source. The effect of this is to vary the drain current, which is similar to the collector current in the BJT that must be initially nonzero. This is achieved by biasing which will be considered shortly. In order to convert the varying drain current $I_D$ into a varying voltage, a resistor $R_L$ is included in the drain circuit. This means that a change $\Delta I_D$ in $I_D$ produces a drain voltage change $\Delta V_D = -\Delta I_D R_L$ in the drain circuit which can be easily monitored. The negative sign indicates that as $I_D$ increases, the drain voltage $V_D$ decreases since the voltage across $R_L$ increases with the increase in drain current. The result is that a signal input $V_i = \Delta V_{GS}$ results in a signal output $V_o = \Delta V_{DS} = -\Delta I_D R_L$ and a full signal cycle can be reproduced. Now, $\Delta I_D/\Delta V_{GS}$ is the transconductance $g_m$ of the JFET. Hence, the voltage gain $A_V = V_o/V_i$ for the JFET is given by

$$A_V = \frac{V_o}{V_i} = -\frac{\Delta I_D \cdot R_L}{\Delta V_{GS}} = -g_m R_L$$

(3.9)
Example 3.3  If a JFET having $g_m = 2.5 \text{ mA/V}$ is used in a common source amplifier, determine the voltage gain if $R_L = 10k$.

Solution

$$A_v = -g_m R_L = -2.5 \text{ mA} \times 10 \text{ k} = -25$$

It is instructive to note that the transconductance for a JFET is given by

$$g_m = \frac{-2I_{DSS}}{V_P} \sqrt{\frac{I_D}{I_{DSS}}}$$

while that for BJT is given by

$$g_m = -40I_C$$

3.4.1.1 Fixed-Bias Configuration

Like the BJT, the FET needs to be operated with quiescent current so that changing the input voltage ($V_{GS}$) results in a changing drain current such that a full signal cycle can be reproduced. A fixed-bias arrangement for the common source JFET analogous to that for the common emitter BJT is shown in Fig. 3.16(a). The potential $V_{GG}$ establishes the reverse bias $V_{GS}$ on the gate–source junction, while resistor $R_G$ connects the gate to ground without short-circuiting $V_i$. This resistor does not inhibit the action of $V_{GG}$ because of the high gate impedance of the JFET. Resistor $R_L$ converts drain current changes into drain voltage changes. In order to determine the quiescent current, $I_{Dq}$ use is made of Shockley’s equation

$$I_D = I_{DSS}(1 - \frac{V_{GS}}{V_P})^2.$$  

Thus, knowing $V_P$ and $I_{DSS}$ for the JFET, $V_{GS}$ is substituted and $I_D$ calculated or vice versa.
Example 3.4  
Bias the n-channel JFET for a drain current of 5 mA using fixed-bias. For the JFET, $I_{DSS} = 10$ mA and $V_P = -8$ V. Use $V_{DD} = 12$ V and choose $R_L$ for maximum symmetrical swing.

Solution  
Using $I_{DSS} = 10$ mA, $V_P = -8$ V, and $I_D = 5$ mA in Shockley’s equation gives

$$V_{GS} = \left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) V_P = \left(1 - \sqrt{\frac{5 \, \text{mA}}{10 \, \text{mA}}}\right)(-8) = (1 - 0.707)(-8) = -2.34 \, \text{V}.$$ 

Hence, $V_{GG} = -2.34$ V. For maximum symmetrical swing with $V_{DD} = 12$ V, $R_L = \frac{12/2}{5 \, \text{mA}} = 1.2 \, \text{k}$. The input impedance of a JFET is greater than $10^8 \, \Omega$, and therefore $R_G$ is chosen to be $1 \, \text{M} \Omega$ to ensure that there is no voltage drop across this resistor arising from small currents into the gate. The solution is shown in Fig. 3.16(b). Input and output coupling capacitors must be used because of the voltages present on the gate and drain. Using (3.5), $g_m$ is given by
Hence, the voltage gain \( A_V \) is given by 
\[
A_v = -g_m R_L = -1.72 \times 1.2 \text{ k} = -2.
\]
This of course is quite low as compared with the BJT and results from the comparatively low value of FET transconductance.

3.4.1.2 Self-Bias
One disadvantage of the fixed-bias method is the need for two voltage supplies. The voltage source \( V_{GG} \) can be eliminated by the inclusion of \( R_S \) in the source circuit of the JFET as shown in Fig. 3.17.
This method of biasing is referred to as self-bias and operates in the following manner: Since the gate is connected to ground through $R_G$, the positive voltage developed across $R_S$ as $I_D$ flows results in the gate (0 V) being at a lower potential than the source (+$I_D R_S$) as in the fixed-bias configuration. $V_{GS}$ is effectively replaced by $V_{GS} = -I_D R_S$. In order to determine the value of $R_S$ to produce a desired $I_D$, Shockley’s equation is again used. Thus, from (3.4),

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 = I_{DSS} \left( 1 + \frac{I_D R_S}{V_P} \right)^2$$  \hspace{1cm} (3.12)

Re-arranging, this yields

$$R_S = \left( \frac{\sqrt{I_D}}{I_{DSS}} - 1 \right) \frac{V_P}{I_D}$$  \hspace{1cm} (3.13)

**Example 3.5** Using the JFET of Example 3.4, find $R_S$ to replace $V_{GG}$.

**Solution** From (3.13),

$$R_S = \left( \sqrt{\frac{5 \text{ mA}}{10 \text{ mA}}} - 1 \right) \frac{-8 \text{ mV}}{5 \text{ mA}} = \frac{0.2929 \times \frac{-8 \text{ mV}}{5 \times 10^{-3}}}{5 \text{ mA}} = 469 \ \Omega.$$  

With the presence of $R_S$, a bypass capacitor $C_3$ is now necessary across $R_S$ in order to ground the FET source for signals and therefore not reduce the voltage gain. Coupling capacitors $C_1$ and $C_2$ are also required for DC blocking. In the presence of $R_S$, the load resistor $R_L$ has to be recalculated for maximum symmetrical swing. This is done by subtracting the source voltage of 2.34 V preserved by the capacitor from the full voltage swing 12 V before computing $R_L = (12 - 2.34)/2/5\text{mA} = 966\Omega$.

**Example 3.6** Using Shockley’s equation $I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$ and a 20 V supply, design a common source amplifier using an n-channel JFET having a pinch-off voltage of −3 V and $I_{DSS} = 8 \text{ mA}$. Use self-bias and a
2 mA quiescent current. Show that \( g_m = -2 \frac{\sqrt{I_D I_{DSS}}}{V_P} \) and use this to calculate the voltage gain of your circuit.

**Solution**  Using \( I_{DSS} = 8 \text{ mA}, V_P = -3 \text{ V}, \text{ and } I_D = 2 \text{ mA} \) in Shockley's equation gives

\[
V_{GS} = \left( 1 - \sqrt{\frac{I_D}{I_{DSS}}} \right) V_P = \left( 1 - \sqrt{\frac{2 \text{ mA}}{8 \text{ mA}}} \right) (-3) = (1 - 0.5) (-3) = -1.5 \text{ V}.
\]

Hence, \( I_D R_S = 1.5 \text{ V} \) giving \( R_S = 1.5 \text{ V}/2 \text{ mA} = 750 \Omega \). For maximum symmetrical swing with \( V_{DD} = 20 \text{ V}, R_L = \frac{(20-1.5)/2}{2 \text{ mA}} = 4.6 \text{ k} \). The input impedance of the JFET is greater than \( 10^8 \Omega \), and therefore \( R_G \) is chosen to be 1 M\( \Omega \). The solution is shown in Fig. 3.18. Input and output coupling capacitors must be used because of the voltages present on the gate and drain. From (3.8), \( g_m \) is given by

\[
g_m = -2 \frac{I_{DSS}}{V_P} \sqrt{\frac{I_D}{I_{DSS}}} = -2 \frac{\sqrt{2 \text{ mA} \times 8 \text{ mA}}}{-3} = -2 \times \frac{4 \text{ mA}}{-3} = 2.67 \text{ mA/V}.
\]
Hence, the voltage gain $A_V$ is given by $A_V = -g_m R_L = - 2.67 \times 4.6 \text{ k} = -12.3$.

### 3.4.1.3 Voltage Divider Biasing

A third FET biasing scheme is the voltage divider bias as shown in Fig. 3.19. Since there is no gate current,

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD} \quad (3.14)$$

and

$$\text{(3.15)}$$
In order to determine the value of $R_S$ to produce a desired $I_D$ using Shockley’s equation, it is easy to show that

$$R_S = \left( \frac{I_D}{I_{DSS}} + \frac{V_G}{V_P} - 1 \right) \frac{V_P}{I_D}$$  \hspace{1cm} (3.16)$$

This scheme, for the same $R_S$, permits higher values of $I_D$. Conversely, for a given value of $I_D$, this scheme permits higher values of $R_S$, which improves quiescent current stability.
Example 3.7 Using an n-channel JFET having $I_{DSS} = 8$ mA and $V_P = -4$ V, bias the device using voltage divider biasing for a drain current of 1.2 mA. Design for a maximum symmetrical swing with $V_{DD} = 12$ V.

Solution Using $V_G = V_{DD}/10 = 1.2$ V say, for $I_{DSS} = 8$ mA, $V_P = -4$ V, and $I_D = 1.2$ mA, Shockley’s equation gives

$$R_S = \left( \sqrt{\frac{1.2}{8} + \frac{1.2}{4} - 1} \right) \frac{4}{1.2} = 3.04 \text{ k}$$

Hence, for maximum symmetrical swing

$$R_L = \frac{(V_{DD} - 3.65)/2}{1.2} = \frac{(12 - 3.65)/2}{1.2} = 3.48 \text{ k}.$$  

Since $V_G = 1.2$ V, then for $R_2 = 200 \text{ k}, R_1 = 10.8 \times 200 \text{ k}/1.2 = 1.8 \text{ M}.$

3.4.1.4 Biasing Using Bipolar Supply

The self-biased system of Fig. 3.17 can be improved by returning $R_S$ to a negative supply voltage as shown in Fig. 3.20. This results in a larger value for $R_S$ and hence greater bias stability as small changes in drain current result in larger corrective changes in gate–source voltage.
Example 3.8  For the fixed-bias common source amplifier in Example 3.6, re-design the system to use a bipolar supply of ±20 V and return $R_S$ to the negative supply voltage instead of ground.

Solution  The modified system is shown in Fig. 3.20. Since $R_S$ is being connected to −20 V instead of ground, its value has to be re-calculated. From the design in Example 3.6 where $R_S$ was connected to ground, for $I_D = 2$ mA, $V_{GS} = -1.5$ V, and hence $R_S$ was calculated from $I_D R_S = 1.5$. Now for $R_S$ connected to −20 V, the full voltage drop across $R_S$ is $1.5 - (-20) = 21.5$, and therefore $R_S$ is calculated from $I_D R_S = 21.5$. This
gives $R_s = 21.5/2 \text{ mA} = 10.8 \text{ k}$. All other component values remain the same.

### 3.4.2 Common Drain Configuration

This FET configuration is shown in Fig. 3.15(b) and is also referred to as a source follower configuration. It is analogous to the common collector or emitter follower configuration in the BJT. Here, the input signal is at the gate and the output signal is at the source. The drain is grounded through the supply. In this configuration, the FET retains its high input impedance but now has reduced output impedance and near unity voltage gain. Figure 3.21 shows the configuration biased for signal amplification. Biasing is based on a voltage divider arrangement which sets FET source voltage at half of the supply voltage for maximum symmetrical swing.

![JFET common drain amplifier](image)

*Fig. 3.21* JFET common drain amplifier
This gives $R_S = \frac{V_{DD}/2}{I_D}$. The gate–source voltage is determined for the desired drain current using Shockley’s equation as before, and the gate voltage set by the voltage divider is then given by $V_G = \frac{V_{DD}}{2} + V_{GS}$.

Coupling capacitors $C_1$ and $C_2$ take the signal into and out of the circuit.

**Example 3.9** Design a source follower circuit using a JFET with $I_{DSS} = 8$ mA, $V_P = -4$ V, and a 12 V supply.

**Solution** Since $V_{DD} = 12$ V, then the quiescent source voltage is 6 V. Hence, if we choose $I_D = 2$ mA, then $R_S = 6$ V/2 mA = 3 k. For $I_D = 2$ mA, $V_{GS} = \left(1 - \sqrt{\frac{2 \text{ mA}}{8 \text{ mA}}}\right)(-4 \text{ V}) = -2 \text{ V}$. Hence, $V_G = 6 - 2 = 4$ V. From this, it follows that $R_1 = 2$ M and $R_2 = 1$ M will produce this gate voltage.

**3.4.2.1 Biasing Using Bipolar Supply**

The common drain amplifier of Fig. 3.21 using voltage divider biasing can be improved by returning $R_S$ to a negative supply voltage $-V_{DD}$ as shown in Fig. 3.22. This results in a larger value for $R_S$ and hence greater bias stability as well as a larger output voltage swing since the available peak-to-peak voltage swing increases from $V_{DD}$ to $2V_{DD}$.
Example 3.10  For the common drain amplifier in Example 3.9, re-design the system to use a bipolar supply of ±12 V and return \( R_S \) to the negative supply voltage instead of ground.

Solution  The modified system is shown in Fig. 3.22. Since \( R_S \) is being connected to −12 V instead of ground, its value has to be re-calculated. From the design in Example 3.9 where \( R_S \) was connected to ground, for maximum symmetrical swing, the source voltage was set at half the supply voltage giving \( R_S = 6 \, V / I_D \). Now for \( R_S \) connected to −12 V, for maximum symmetrical swing, the source voltage is set at 0 V giving a voltage drop across \( R_S \) of 0 − (−12) = 12 V. Therefore, \( R_S \) is calculated from \( R_S = 12 / 2 \, mA = 6 \, k \). All other component values remain the same.

3.4.3 Common Gate Configuration
The last configuration of the FET is the common gate configuration shown in Fig. 3.15(c). Here, the input signal is applied to the source and the output signal taken from the drain of the FET. The gate is grounded and hence common to both input and output. This configuration is analogous to the common base BJT amplifier and is frequently used in high-frequency amplifiers and where low input impedance is required. A practical implementation of this configuration in an amplifier circuit is shown in Fig. 3.23. The design of this circuit follows the same procedure as the common source circuit discussed in Sect. 3.4.1. In the self-bias case, the resistor $R_G$ is now not necessary, and the gate can be connected directly to ground. In the voltage divider bias, the gate is grounded using a capacitor. In both cases, the signal is injected at the source using a capacitor, and the output signal is available at the drain. Hence, a common source amplifier can be converted to a common gate amplifier by grounding the input coupling capacitor and lifting the grounded end of the bypass capacitor and there applying the input signal.
Example 3.11  Show how a common source amplifier can be converted to a common gate amplifier.

Solution   The common source amplifier of Example 3.6 is shown again in Fig. 3.24(a). Its conversion to a common gate amplifier can be effected by lifting the bypass capacitor $C_3$ from ground and applying the input signal through it to the source and grounding the capacitor going to the gate. The resulting circuit is shown in Fig. 3.24(b). The gate resistor and input capacitor are no longer needed and can be replaced by a short circuit.
Biasing Using Bipolar Supply

Example 3.12  For the common gate amplifier in Example 3.11, re-design the system to use a bipolar supply of ±20 V and return \( R_S \) to the negative supply voltage instead of ground.

Solution  The modified system is shown in Fig. 3.25. Since \( R_S \) is being connected to −20 V instead of ground, its value has to be re-calculated. Thus, from the design in Example 3.11 where \( R_S \) was connected to ground, for \( I_D = 2 \) mA, \( V_{GS} = -1.5 \) V, and hence \( R_S \) was calculated from \( I_D R_S = 1.5 \). Now with \( R_S \) connected to −20 V, the full voltage drop across \( R_S \) is \( 1.5 - (-20) = 21.5 \), and therefore \( R_S \) is calculated from \( I_D R_S = 21.5 \). This gives \( R_S = 21.5/2 \) mA = 10.8 k. All other component values remain the same. As is evident, this procedure is exactly that for the bipolar biasing of a self-biased common source amplifier.
In addition to the JFET, there is the MOSFET which is of two types – depletion and enhancement – and both of these are available in n-channel and p-channel types. This device achieves extremely high input impedance because of an insulating layer of silicon dioxide between the gate and the conduction channel instead of the reverse bias method of the JFET.

3.5.1 Depletion-Type MOSFET
In the depletion-type MOSFET shown in Fig. 3.26, a channel is diffused between source and drain, with the same type of impurity as used for the source and drain. Thus, the n-channel type consists of a lightly
doped p-type substrate into which two highly doped n regions along with relatively lightly doped n-channel are diffused. A thin silicon dioxide (SiO$_2$) layer is also placed over the surface and aluminum contacts introduced for gate, source, and drain terminals. In order to ensure that the p–n junction formed between the channel and substrate is reverse-biased, the substrate is held at a negative potential relative to the channel. This is accomplished either by connecting the substrate to the source internally as occurs in most devices or by way of an external connection. The effect is that as the drain–source voltage $V_{DS}$ is increased from zero, an increase in a voltage drop along the channel results with a consequent flow in drain current through the channel. Since the p-type substrate is connected to the source, the voltage drop along the channel results in a reverse bias between the n-type channel and the p-type substrate. This creates a depletion region in the n-type channel that extends into the channel to a depth that depends on the magnitude of $V_{DS}$. Since the voltage drop along then channel is greater at the drain as compared with the source, the width of penetration of the depletion layer is greater near the drain than near the source. With the gate–source voltage held at zero, as the drain–source voltage $V_{DS}$ is increased, the voltage drop along the channel causes the depletion layer to extend further into that part of the channel region nearest to the drain than across the part nearest the source to an extent that depends on the magnitude of the drain–source voltage as shown in Fig. 3.27(a). This penetration determines the resistance of the channel to current flow.
Fig. 3.26  n-Channel depletion MOSFET structure
The overall effect is that an increase of drain–source voltage initially causes an increase of drain current. Further increase results in an increase in the width of the depletion region, and this leads to saturation of the drain current as the width of the depletion region extends almost completely across the drain. Such a condition is referred to as pinch-off and prevents further increase of the drain current with increase of the drain–source voltage. The resulting drain current versus drain–source voltage is shown in Fig. 3.28.

If the gate–source voltage is made negative relative to the source as shown in Fig. 3.27(b), electrons are repelled out of the channel into the n$^+$ region. This reduces the number of free electrons which are available for conduction in the channel region and so the channel resistance is increased. As a result, pinch-off occurs at a lower drain–source voltage and saturation current.

If the gate–source voltage is changed from zero and made positive, electrons will be attracted into the channel from the heavily doped n$^+$ regions. The number of conduction electrons is increased and so the channel resistance is reduced. This will cause a greater drain current to flow for a given drain–source voltage and means that a larger value of drain–source voltage is required to cause pinch-off. Therefore, the overall effect of the gate–source voltage increase is an increase in pinch-off voltage and saturation current. This mode is referred to as the
enhancement mode. Thus, the gate–source voltage controls the saturation drain current of the MOSFET. Moreover, because of the silicon dioxide layer, an n-channel depletion MOSFET operates in both an enhancement and a depletion mode, and it is possible to change the polarity of the gate–source voltage. The transfer and output characteristics are shown in Figs. 3.29 and 3.30, respectively, and are similar to those of JFET except that JFET has only the depletion mode. Shockley’s equation given by

\[ I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 \]

also defines the behavior of the depletion MOSFET.

\[ Fig. 3.29 \text{ n-Channel mutual characteristics} \]
The p-channel depletion MOSFET is shown in Fig. 3.31. It operates in a manner similar to the n-channel depletion MOSFET except that all polarities are reversed. The associated drain characteristics are shown in Fig. 3.32 with reversed voltage polarities. The mutual characteristic is shown in Fig. 3.33, and here too the polarity change in the gate–source voltage can be seen. As previously observed, the JFET is also a depletion mode or normally on device. It cannot be used in the enhancement mode because this would involve forward biasing the gate–source junction. This could result in excessive gate-current flow and would lower the input impedance or even damage the device.
Fig. 3.31 p-Channel depletion MOSFET structure
Fig. 3.32  Drain characteristics of p-channel depletion MOSFET
Fig. 3.33  p-Channel mutual characteristics

Symbols for the depletion MOSFET are shown in Fig. 3.34.

Fig. 3.34 Symbols for the depletion MOSFET (a) n-channel and (b) p-channel
3.5.2 Enhancement-Type MOSFET
The n-channel enhancement-type MOSFET is shown in Fig. 3.35. It consists of a lightly doped p-type substrate into which two highly doped n$^+$ regions are diffused. A thin layer of insulating silicon dioxide (SiO$_2$) is grown over the surface and aluminum contacts made as shown in the diagram. Like the enhancement-type MOSFET, the substrate and source are connected together in order to ensure that the channel substrate junction is reverse-biased. Unlike the depletion-type MOSFET, no channel exists between the two highly doped drain and source regions. Because of this, if no potential is applied between gate and source, there is essentially no conduction through the channel with the application of a drain–source voltage. In fact for $V_{GS} \leq 0$, the channel current is of the order of a few nano-amperes (since the channel consists of two back-to-back diodes). With a positive voltage applied between gate and source as shown in Fig. 3.36, a virtual channel is created between the drain and the source. The positive voltage attracts negative carriers into the p-type substrate from the n-type regions, and this results in significantly increased conductivity between drain and source.
The minimum positive gate–source voltage that is necessary for the creation of the virtual channel so that conduction is possible is called the threshold voltage. Its value at which the drain current \( I_D \) reaches some defined value, say 10 \( \mu \)A, is often quoted and is typically about 2 V. Thus, the positive voltage enhances the drain current, and such a device is called an enhancement-type MOSFET. As \( V_{GS} \) is made positive, the drain current \( I_D \) increases slowly then rapidly.

An increase in the gate–source voltage above the threshold value will attract more electrons into the channel region. Once the virtual channel has been formed, the drain current which flows is influenced by the magnitude of both the gate–source and drain–source voltages. For a given \( V_{GS} > V_T \) as \( V_{DS} \) is increased, the width of the depletion region increases until pinch-off occurs, thereby causing saturation of the drain current as occurred in the depletion MOSFET. As \( V_{GS} \) is increased above \( V_T \), channel conductivity increases, and therefore, pinch-off occurs at the
higher values of $V_{DS}$ and $I_D$ as shown in Fig. 3.37. Thus, the drain current of the enhancement-type MOSFET can be controlled by the gate–source voltage.

![Graph showing drain characteristics of n-channel enhancement MOSFET](image)

**Fig. 3.37** Drain characteristics of n-channel enhancement MOSFET

The enhancement-type MOSFET has a mutual characteristic Fig. 3.38 that is very different from the JFET and the depletion-type MOSFET. The main difference arises because of the need for the gate–source voltage to exceed a threshold value in order that channel conduction occurs. The defining equation is different from the Shockley and is given by

$$I_D = k(V_{GS} - V_T)^2$$  \hspace{1cm} (3.17)

where $k$ is a constant. It is found using

$$k = \frac{I_D(\text{on})}{(V_{GS(\text{on})} - V_T)^2}$$  \hspace{1cm} (3.18)

where $I_D(\text{on})$ and $V_{GS(\text{on})}$ are particular drain current and associated gate–source voltage values for the device. Specification sheets usually
provide \( V_T \), \( V_{GS(on)} \), and \( I_{D(on)} \). Having found \( k \), Eq. (3.17) can be used to find \( V_{GS} \) for a given \( I_D \).

The p-channel enhancement-type MOSFET operates in a similar manner except that the polarities are reversed. The corresponding drain and mutual characteristics are shown in Figs. 3.39 and 3.40. It is important to note that the enhancement-type MOSFET has no conducting channel and one has to be created by enhancement process. Therefore, like JFET, the gate–source voltage can only be of one polarity. Also, the existence of a turn-on threshold gate–source voltage in the enhancement-type MOSFET is similar to the existence of a turn-on threshold base-emitter voltage in BJT. Symbols for the enhancement-type MOSFET are shown in Fig. 3.41.
**Fig. 3.39** Drain characteristics of p-channel enhancement MOSFET

**Fig. 3.40** Mutual characteristic of p-channel enhancement MOSFET


### 3.5.3 MOSFET Parameters

The MOSFET has a set of parameters similar to the JFET. Specifically, these are its transconductance $g_m$ which is typically in the range $1$–$10$ mA/V, its input resistance $R_i$ which is usually higher than about $10^{10}$ Ω, and its drain–source resistance $r_{DS}$ which is of the order $5$–$50$ kΩ. The flat nature of the output characteristics is an indication of the independence of $I_D$ of $V_{DS}$ for a given $V_{GS}$. In practice, however, increasing $V_{DS}$ after pinch-off has occurred causes the channel pinch-off point to migrate away from the drain toward the source. This causes an effective channel length reduction, a phenomenon referred to as channel length modulation. The overall effect is to cause an increase in drain current with further increase in drain–source voltage in the saturation region. This manifests itself as output characteristics that have a slightly positive slope instead of being flat. As occurred with the BJT, these curves when extrapolated intercept the $V_{DS}$ axis at a common point $V_{DS} = -V_A$. The curves enable the determination of the drain output resistance.

### 3.6 MOSFET Amplifiers

The MOSFET can also be used in three configurations of MOSFET amplifiers. These are discussed in this section with several examples given of practical applications.
3.6.1 Depletion-Type MOSFET Common Source Amplifier

The depletion-type MOSFET which also obeys Shockley’s equation can be biased in a similar manner to JFET. This is shown in Fig. 3.42 where self-bias is used.

![Depletion MOSFET common source amplifier using self-bias](image)

**Fig. 3.42** Depletion MOSFET common source amplifier using self-bias

**Example 3.13** Using self-bias, design a biasing network for a common source n-channel depletion-type MOSFET having $I_{DSS} = 8$ mA and $V_P = -8$ V.

**Solution** The circuit is shown in Fig. 3.42. Choosing a quiescent drain current of 2 mA, Shockley’s equation gives

$$V_{GS} = \left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) V_P = \left(1 - \sqrt{\frac{2}{8\ mA}}\right)(-8 \ V) = -4 \ V.$$
Hence, $R_S = 4 V/2 \text{mA} = 2 \text{k}$. We determine $R_D$ in order to achieve maximum symmetrical swing. Therefore, $R_D = (V_{DD} - I_D R_S)/2I_D$. This yields $R_D = (20 - 4)/2 \times 2 \text{mA} = 4 \text{k}$. Finally, resistor $R_G$ can be set at 1 M because of the high input impedance of the device.

A depletion-type common source amplifier using voltage divider bias is shown in Fig. 3.43. The design approach is similar to that used in the JFET amplifier in Fig. 3.17. In Fig. 3.43 since there is no gate current,

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD} \tag{3.19}$$

and

$$V_{GS} = V_G - I_D R_S \tag{3.20}$$

![MOSFET voltage divider bias](image)
The value of $R_S$ required to produce a desired $I_D$ is determined by using Shockley’s equation. This gives

$$R_S = \left( \sqrt{\frac{I_D}{I_{DSS}}} + \frac{V_G}{V_P} - 1 \right) \frac{V_P}{I_D}$$  \hspace{1cm} (3.21)$$

This scheme, for the same $R_S$, permits higher values of $I_D$ than is possible with self-bias. Conversely, for a given value of $I_D$, this scheme permits higher values of $R_S$, which generally improves quiescent current stability.

**Example 3.14** Using an n-channel depletion MOSFET having $I_{DSS} = 6$ mA and $V_P = -3$ V and the circuit shown in Fig. 3.43, bias the device using voltage divider biasing for a drain current of 5 mA. Design for a maximum symmetrical swing with $V_{DD} = 18$ V.

**Solution** Using $V_G = V_{DD}/10 = 1.8$ V, for $I_{DSS} = 6$ mA, $V_P = -3$ V, and $I_D = 5$ mA, Shockley’s equation gives $R_S = \left( \sqrt{\frac{1.8}{6}} + \frac{1.8}{-3} - 1 \right) = 631 \Omega$.

Note, $I_D R_S = 5 \times 0.631 = 3.2$ V. Hence, for maximum symmetrical swing $R_L = \frac{(V_{DD} - 3.2)/2}{5} = 1.48$ k. Since $V_G = 1.8$ V, then for $R_2 = 200$ k and $R_1 = 18 \times 200 \text{ k}/1.8 - 200$ k = 1.8 M.

### 3.6.2 Depletion-Type MOSFET Common Drain Amplifier

This MOSFET configuration is shown in Fig. 3.44. It is similar to the common drain or source follower configuration using JFET in Fig. 3.21. As in the JFET common drain configuration, the MOSFET retains its high input impedance but now has reduced output impedance and approximately unity voltage gain. Figure 3.44 shows the configuration biased for signal processing. Biasing employs a voltage divider network which sets the MOSFET source voltage at half of the supply voltage for maximum symmetrical swing. This gives $R_S = \frac{V_{DD}/2}{I_D}$. The gate–source voltage is again determined for the desired drain current using
Shockley’s equation, and the gate voltage set by the voltage divider is then given by \( V_G = \frac{V_{dd}}{2} + V_{GS} \). Capacitors \( C_1 \) and \( C_2 \) are the input and output coupling capacitors.

**Fig. 3.44** MOSFET common drain amplifier

**Example 3.15** Using the circuit shown in Fig. 3.44, design a common drain amplifier using an n-channel depletion MOSFET having \( I_{DSS} = 7 \, \text{mA} \) and \( V_P = -5 \, \text{V} \). Design for maximum symmetrical swing with \( V_{DD} = 20 \, \text{V} \).

**Solution** Since \( V_{DD} = 20 \, \text{V} \), then the quiescent source voltage must be 10 V for maximum symmetrical swing. Hence, if we choose \( I_D = 4 \, \text{mA} \), then \( R_S = 10 \, \text{V}/4 \, \text{mA} = 2.5 \, \text{k} \). For \( I_D = 4 \, \text{mA} \),

\[
V_{GS} = \left(1 - \sqrt{\frac{4 \, \text{mA}}{8 \, \text{mA}}}\right)(-4 \, \text{V}) = -1.2 \, \text{V}
\]

Hence, \( V_G = 10 - 1.2 = 8.8 \, \text{V} \).

Resistors \( R_1 = 880 \, \text{k} \) and \( R_2 = 1.12 \, \text{M} \) will produce this gate voltage.
3.6.3 Depletion-Type MOSFET Common Gate Amplifier
The third configuration in which the MOSFET can be used is the common gate configuration, which is shown in Fig. 3.45. This configuration is similar to the common gate JFET amplifier of Fig. 3.23.

Fig. 3.45 MOSFET common gate amplifier

The design of this circuit follows the same procedure as the common source circuits discussed earlier. In the self-bias case, the resistor $R_G$ is no longer necessary, and the gate can be connected directly to ground as shown in Fig. 3.45. In the voltage divider bias, the gate is grounded using the input capacitor. In both cases, the signal is injected at the source using a capacitor, and the output signal is taken at the drain. Hence, the common source amplifier can be converted to a common gate amplifier by grounding the input coupling capacitor and lifting the grounded end of the bypass capacitor and there applying the input signal.
Example 3.16  Design a common gate amplifier using an n-channel depletion MOSFET with \( I_{DSS} = 2 \, \text{mA} \) and \( V_P = -3 \, \text{V} \). Design for maximum symmetrical swing using a 24 V supply.

Solution  The circuit is shown in Fig. 3.45. Choosing a quiescent drain current of 1 mA, Shockley’s equation gives

\[
V_{GS} = \left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) V_P = \left(1 - \sqrt{\frac{1}{2}} \right) (-3 \, \text{V}) = -0.88 \, \text{V}.
\]

Hence, \( R_S = 0.88 \, \text{V}/1 \, \text{mA} = 880 \, \Omega \). We determine \( R_D \) in order to achieve maximum symmetrical swing.

Therefore, \( R_D = (V_{DD} - I_D R_S)/I_D \). This yields

\[
R_D = (24 - 0.88)/1 \times 2 \, \text{mA} = 11.6 \, \text{k}.
\]

Note that no gate resistor \( R_G \) is needed as the gate can be directly connected to ground.

### 3.6.4 Enhancement-Type MOSFET Common Source Amplifier

As indicated earlier, the equation defining the characteristics of the enhancement-type MOSFET is different from the depletion-type device. Recall that the drain current is zero for zero gate–source voltage since there is initially no conducting channel. The gate–source voltage \( V_{GS} \) must exceed a threshold voltage \( V_T \) for channel conduction to occur. Then, the drain current is given by

\[
I_D = k(V_{GS} - V_T)^2
\]  \( (3.22) \)

The specification sheet for the device typically provides the threshold voltage \( V_T \) along with a drain current value and the corresponding gate–source voltage. The constant \( k \) can be found using these values after which the equation can be used to determine gate–source voltage for achieving a particular value of drain current. One method of biasing the enhancement-type MOSFET is feedback biasing as shown in Fig. 3.46. Here since there is no gate current, there is no voltage drop across \( R_G \) and therefore \( V_{GS} = V_{DS} \).
Example 3.17  Using the circuit shown in Fig. 3.46, design a feedback biasing network for an enhancement-type MOSFET having $V_T = 3$ V, $I_{Don} = 6$ mA, and $V_{GSon} = 8$ V. Use $V_{DD} = 15$ V.

Solution  The circuit is shown in Fig. 3.46. Using the data provided, $k$ is given by $k = 6$ mA/(8 V – 3 V)$^2 = 0.24$ mA/V$^2$. For a quiescent drain current of 3 mA, $V_{GS} = V_T + \frac{I_D}{k} = 3 + \sqrt{\frac{3 \text{ mA}}{0.24 \text{ mA/V}^2}} = 6.54$ V. Hence, $V_{GS} = V_{DS} = 6.54$ V, and therefore $R_D = (V_{DD} - V_{DS})/I_D = (15 - 6.54)/3 \text{ mA} = 2.8$ k. Note that $V_{RD} = 15 - 6.54 = 8.46$ V while $V_{DS} = 6.54$ V. This is not biased for maximum symmetrical swing, though it will deliver a reasonable output.
The extremely high input impedance of the FET means that $R_G$ can be a high-value resistor, say 10 M.

The bias arrangement in Fig. 3.47 is a modified version of that in Fig. 3.46. The two resistors $R_{G1}$ and $R_{G2}$ result in a lower voltage at the gate of the FET as compared with the drain and hence allow maximum symmetrical swing design.

**Fig. 3.47** Modified enhancement-type MOSFET bias

**Example 3.18** Using the configuration in Fig. 3.47, design a modified feedback biasing network for an enhancement-type MOSFET having $V_T = 3$ V, $I_{Don} = 6$ mA, and $V_{GSon} = 8$ V. Use $V_{DD} = 20$ V.
Solution  The circuit is shown in Fig. 3.47. Using the data provided, \( k \) is given by \( k = 6 \text{ mA}/(8 \text{ V} - 3 \text{ V})^2 = 0.24 \text{ mA}/V^2 \). For a quiescent drain current of 3 mA, 
\[
V_{GS} = V_T + \sqrt{\frac{3 \text{ mA}}{0.24 \text{ mA}/V^2}} = 6.54 \text{ V}.
\]
For maximum symmetrical swing, \( V_D = V_{DD}/2 = 20/2 = 10 \text{ V} \) and therefore 
\[
R_D = V_D/I_D = 10/3 \text{ mA} = 3.3 \text{ k}.
\]
Since the drain is at 10 V and the gate is at 6.54 V, the resistors \( R_{G1} \) and \( R_{G2} \) can now be calculated. The extremely high input impedance of the FET means that no current flows into the gate. Therefore, 
\[
6.54/R_{G2} = 10/(R_{G1} + R_{G2})
\]
which for \( R_{G2} = 10 \text{ M} \) gives \( R_{G1} = 5.3 \text{ M} \).

Another popular biasing method for the enhancement MOSFET is voltage divider biasing shown in Fig. 3.48. As in the case of BJT, the resistor \( R_S \) provides improved stability of the quiescent drain current.
Example 3.19 Using the configuration in Fig. 3.48, design a voltage divider-biased common source amplifier using an enhancement-type MOSFET having $V_T = 2 \text{ V}$, $k = 0.05 \text{ mA/V}^2$ and use $V_{DD} = 15 \text{ V}$.

Solution The circuit is shown in Fig. 3.48. For a quiescent drain current of 10 mA,

$$V_{GS} = V_T + \sqrt{\frac{0.1}{0.05}} = 2.45 \text{ V}.$$ 

Using the rule-of-thumb $V_S = V_{DD}/10$ to allow large output voltage swing,

$V_S = 15/10 = 1.5 \text{ V}$. Then, $R_S = 1.5/10 \text{ mA} = 150 \Omega$. For maximum symmetrical swing, $V_{RD} = (V_{DD} - V_S)/2 = (15 - 1.5)/2 = 6.75 \text{ V}$ and
therefore \( R_D = \frac{6.75}{I_D} = \frac{6.75}{10} \text{ mA} = 675 \Omega \). The resistors \( R_{G1} \) and \( R_{G2} \) can now be calculated. \( V_G = V_{GS} + V_S = 2.45 + 1.5 = 3.95 \) V. The extremely high input impedance of FET means that no current flows into the gate. Therefore, \( \frac{3.95}{R_{G2}} = \frac{15}{(R_{G1} + R_{G2})} \) which for \( R_{G2} = 1 \) M gives \( R_{G1} = 2.8 \) M.

### 3.6.5 Enhancement-Type MOSFET Common Drain Amplifier

The configuration shown in Fig. 3.49 is the common drain amplifier using the enhancement-type MOSFET. It is similar to that for the other FET types. Here it is biased using voltage divider biasing. The standard approach of setting the source voltage to half the supply voltage in order to make possible maximum symmetrical swing can be employed. Another approach is to set the gate to half of the supply voltage by selecting \( R_{G1} = R_{G2} \) then using Eq. (3.20) to determine the value of \( R_S \) to give the desired value of drain current.
Example 3.20 Using the configuration in Fig. 3.49, design a voltage divider-biased common drain amplifier using an enhancement-type MOSFET having $V_T = 2 \, \text{V}$, $k = 0.25 \, \text{mA/V}^2$, and use $V_{DD} = 20 \, \text{V}$.

Solution The circuit is shown in Fig. 3.49. Setting $R_{G1} = R_{G2} = 1 \, \text{M}$ this gives $V_G = 10 \, \text{V}$. For a quiescent drain current of 2 mA,

$$V_{GS} = V_T + \sqrt{\frac{I_D}{k}} = 2 + \sqrt{\frac{2 \, \text{mA}}{0.25 \, \text{mA/V}^2}} = 4.8 \, \text{V}.$$ 

Hence,

$$V_S = V_G - V_{GS} = 10 - 4.8 = 5.2 \, \text{V}$$ 

and therefore $R_S = 5.2/2 \, \text{mA} = 2.6 \, \text{k}$.

3.6.6 Enhancement-Type MOSFET Common Gate Amplifier

The common gate configuration shown in Fig. 3.50 can be derived from the voltage divider-biased common source in Fig. 3.48. Once again by
grounding the input capacitor $C_1$, ungrounding the bypass capacitor $C_S$, and injecting the input signal through this latter capacitor, the circuit now functions as a common gate amplifier. The signal output is taken at the drain.

**Fig. 3.50** Common gate amplifier

**Example 3.21** Using the configuration in Fig. 3.50, design a voltage divider-biased common gate amplifier using an enhancement-type MOSFET having $V_T = 2 \text{ V}$, $k = 0.05 \text{ mA/V}^2$, and use $V_{DD} = 15 \text{ V}$ as used in the voltage divider-biased common source amplifier in Example 3.19.

**Solution** The design procedure used in Example 3.19 for the voltage divider-biased common source amplifier is employed to produce the design shown in Fig. 3.48. However, now capacitor $C_1$ is grounded and
the input signal applied at capacitor $C_S$ which is ungrounded. The resulting circuit is shown in Fig. 3.51.

![Circuit Diagram]

**Fig. 3.51** Solution for Example 3.21

### 3.7 Applications

In this section, we discuss several circuits in which field-effect transistors are applied. Before doing so, we summarize and compare the characteristics of BJT, JFET, and MOSFET in Table 3.1. These varying characteristics enable these devices to be used in a wide range of applications, some of which are below.

**Table 3.1** Comparison of characteristics

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>BJT</th>
<th>JFET</th>
<th>MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control type</td>
<td>Current (and voltage) controlled</td>
<td>Voltage controlled</td>
<td>Voltage controlled</td>
</tr>
<tr>
<td>Characteristic</td>
<td>BJT</td>
<td>JFET</td>
<td>MOSFET</td>
</tr>
<tr>
<td>-----------------------</td>
<td>------------------------------</td>
<td>-----------------------------------------</td>
<td>-----------------------------</td>
</tr>
<tr>
<td>Controlling terminal</td>
<td>Base</td>
<td>Gate</td>
<td>Gate</td>
</tr>
<tr>
<td>Current flow</td>
<td>Bipolar (majority and minority carriers)</td>
<td>Unipolar (majority carriers)</td>
<td>Unipolar (majority carriers)</td>
</tr>
<tr>
<td>Junction</td>
<td>One forward- and one reverse-biased junctions</td>
<td>One reverse-biased junction</td>
<td>One reverse-biased junction</td>
</tr>
<tr>
<td>Input resistance</td>
<td>Moderate</td>
<td>High</td>
<td>Very high</td>
</tr>
<tr>
<td>Gain</td>
<td>High</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Noise</td>
<td>Moderate (low at low currents)</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Mutual characteristic</td>
<td>Nonlinear</td>
<td>Nonlinear</td>
<td>Nonlinear</td>
</tr>
</tbody>
</table>

3.7.1 Headphone Amplifier

The circuit shown in Fig. 3.52 is a common source amplifier using a JFET that provides an amplified signal to a pair of high-impedance headphones such as the widely available piezoelectric earphones. It uses the design principles outlined in Sect. 3.4.1 and incorporates a volume control potentiometer in the drain circuit instead of a fixed resistor. Capacitor $C_2$ ensures that none of the DC interferes with the headset. As a rule of thumb, the coupling capacitors are chosen such that their reactance value is equal to the impedance of the load at the lowest desired frequency of operation.
**Ideas for Exploration:** Explain why the headphone volume goes down as the wiper of the potentiometer moves toward the positive supply voltage.

### 3.7.2 JFET Preamplifier

The circuit shown in Fig. 3.53 is another common source amplifier that amplifies the signal from a crystal microphone or other signal source. The design principles outlined in Sect. 3.4.1 again apply. The output is used to drive a power amplifier.
**Fig. 3.53** Preamplifier circuit

*Ideas for Exploration:* Re-design the circuit using a p-channel JFET such as the 2N5460.

(i) Simulate the circuit in Multisim and determine the gain.

### 3.7.3 Crystal Microphone Lead Extender

Piezoelectric or crystal microphones have a high output impedance of about 1 M. As a result, they cannot be used with long leads into the amplifier. The circuit shown in Fig. 3.54 has a low output impedance and allows the crystal microphone to be used with long leads. It comprises a common drain or source follower amplifier using a 2N4393 JFET with $I_{DSS} = 10$ mA and $V_T = -2$ V. In order to make it portable, a 9V
battery is used to provide power. Choosing a drain current of 2 mA, Shockley’s equation gives

\[ V_{GS} = \left(1 - \sqrt{\frac{2}{10}}\right) \cdot (-2) = -1.1 \text{ V}. \]

Then

\[ R_2 = 1.1V/2 \text{ mA} = 550 \Omega. \] Let \( R_1 = 2.2 \text{ M} \) giving the circuit a high input impedance. The low output impedance of JFET requires that a large electrolytic capacitor \( C_1 = 100 \mu\text{F} \) value be employed at the output. Resistor \( R_3 = 10 \text{ k} \) connects the negative plate of the capacitor to ground, thereby ensuring that it is properly polarized.

1

*Ideas for Exploration:* (i) Modify the circuit by using a bipolar supply of \( \pm 9 \text{ V} \). Such voltages can be supplied by two 9 V batteries for portable use. In this design, \( R_S \) connects the source terminal of JFET to the negative supply and not ground as before. For \( I_D = 2 \text{ mA} \), the required gate–source voltage is \( V_{GS} = -1.1 \text{ V} \). Since the gate is at zero potential and must be 1.1 V lower than the source, it follows that the source is at 1.1 V. Hence, the voltage drop across \( R_S \) is 1.1 V – \((-9 \text{ V})\) = 10.1 V. The value of \( R_S \) is therefore given by

\[ R_S = 10.1 \text{ V}/2 \text{ mA} = 5 \text{ k}. \] The increased supply voltage provides increased symmetrical swing. (ii) Test both circuits using several meters of shielded cable feeding into a power amplifier.
3.7.4 JFET DC Voltmeter

The circuit shown in Fig. 3.55 employs a JFET in a DC voltmeter application that is able to measure voltages from 0 to 100 V with an input impedance of 1 MΩ on all of five ranges. It comprises a JFET in the source follower mode driving a microammeter in a Wheatstone bridge arrangement. Resistors $R_8$ and $R_9$ and potentiometer $VR_2$ form a potential divider across the supply such that a zero-reference voltage at point A means that point B is at −4 V and point C is at +8 V. Selecting a drain current of 1 mA, Shockley’s equation for the 2N3819 JFET gives $V_{GS} = −2.8$ V. Hence, with the gate connected to the reference voltage point A through the resistors $R_1$ to $R_6$, the voltage drop across $R_7$ is $2.8 − (−4) = 6.8$ V which gives $R_7 = 6.8/1$ mA = 6.8 kΩ. Thus, $Tr_1$, $R_7$ along with $R_8$, $VR_2$ and $R_9$ form a Wheatstone bridge network and $VR_2$ is adjusted such that for zero signal into the JFET, the bridge is balanced and no current flows through the meter. A positive voltage signal at the input is delivered at the source of the JFET, and this causes the bridge to go out of balance such that current proportional to the input signal flows in the meter. Using $R_9 = 1.5$ kΩ, then the current through the $R_8$, $VR_2$, $R_9$ chain is $4/1.5$ kΩ = 2.67 mA. For a 2 kΩ potentiometer for $VR_2$, then the series arrangement of $R_8$ and $VR_2$ has a voltage drop given by $2.67$ mA × $(R_8 + 2$ kΩ) = 8 V giving $R_8 = 1$ kΩ. This allows a voltage drop across $VR_2$ of 5.3 V which enables balancing of the bridge since the source voltage is 2.8 V. $VR_1$ is chosen to be a 2.5 kΩ potentiometer that enables calibration of the meter. The potential divider network $R_1$-$R_5$ provides ranges of 1 V, 5 V, 10 V, 50 V, and 100 V. These values are $R_1 = 10$ kΩ, $R_2 = 10$ kΩ, $R_3 = 80$ kΩ which is made up with standard resistor values 68 kΩ + 12 kΩ, $R_4 = 100$ kΩ and $R_5 = 800$ kΩ which is made up with standard resistor values 680 kΩ + 120 kΩ. Therefore, when on the 5 V range, 5 V at the input would result in 1 V at the junction of $R_3$ and $R_2$. Similarly, when on the 50 V range, 50 V at the input would result in 1 V at the junction of $R_2$ and $R_1$. Thus, with no signal applied, $VR_2$ is adjusted for zero current through the meter. With the meter switched to the 1 V range, 1 V DC is applied
and $VR_1$ adjusted for full-scale deflection. In order to avoid excessive drift, this circuit will benefit from the use of a Zener-regulated power supply. Resistor $R_6 = 1 \, \text{M}$ protects the JFET from over-voltage at the input.

![JFET DC voltmeter circuit diagram](image)

**Fig. 3.55** JFET DC voltmeter

**Ideas for Exploration:** (i) Expand the voltage ranges of the voltmeter from 5 to 7 to cover the range 1 V to 1000 V, using the attenuator network shown in Fig. 3.56.
3.7.5 JFET AC Voltmeter

The circuit of an AC voltmeter using a JFET is shown in Fig. 3.56. The circuit utilizes a 2N4868 JFET in the common source configuration such that voltage signals at the gate are amplified and delivered at the drain. The pinch-off voltage for this FET is $V_P = -2\ V$ with $I_{DSS} = 2\ mA$. Hence, for a drain current of 0.4 mA, Shockley’s equation gives...
Thus, $R_{10} = 1.1/0.4 = 2.75 \, k$. In order to allow sufficient voltage swing at the output, resistor $R_9$ is set at $10 \, k$. The voltage drop across this resistor is therefore $4 \, V$, and with $1.1 \, V$ across $R_{10}$ that leaves about $4 \, V$ across the transistor drain–source junction. The output of the drain drives diodes $D_1$ and $D_2$ through coupling capacitor $C_2 = 1 \, \mu F$. On the positive half-cycle at the output, diode $D_2$ turns off, while diode $D_1$ turns on. Current through $R_9$ flows through diode $D_1$. On the negative half-cycle, diode $D_1$ turns off and diode $D_2$ turns on. The current then flows through the $100 \, \mu A$ meter-potentiometer-$D_2$ connection into the drain of the FET. $VR_1 = 20 \, k$ is used to calibrate the meter. Resistors $R_1$–$R_7$ form an input attenuator which reduces the voltage to be measured before it is applied to the gate of the JFET. This divider network provides seven ranges of $1$, $5$, $10$, $50$, $100$, $500$, and $1000 \, V$ so that the JFET gate voltage is $1 \, V$ when the maximum voltage on any range is applied at the measurement input. For this, $R_7 = 800 \, k$, $R_6 = 100 \, k$, $R_5 = 80 \, k$, $R_4 = 10 \, k$, $R_3 = 8 \, k$, $R_2 = 1 \, k$, $R_1 = 1 \, k$. Therefore, on the $5 \, V$ range, $5 \, V$ at the input would result in $1 \, V$ at the junction of $R_3$ and $R_2$. Similarly, on the $100 \, V$ range, $100 \, V$ at the input would result in $1 \, V$ at the junction of $R_2$ and $R_1$. The input attenuator presents an input impedance of $1 \, M$ on all ranges. Resistor $R_8 = 1 \, M$ protects the JFET from over-voltage at the input. Coupling capacitor $C_1 = 1 \, \mu F$ prevents DC from entering the system. Coupling capacitor $C_2 = 10 \, \mu F$ and bypass capacitor $C_3 = 100 \, \mu F$.

*Ideas for Exploration:* (i) Test the frequency response of the system by applying a fixed input voltage, varying the frequency from about $20 \, Hz$ to about $100 \, kHz$ and noting the response on the meter.

### 3.7.6 MOSFET Amplifier

This amplifier circuit shown in Fig. 3.57 employs an enhancement MOSFET in a simple configuration that is quite versatile. The potentiometer $VR_1$ is adjusted in order to overcome the threshold voltage and turn on the device. Its value is not critical and can be between $10$ and $100 \, k$. Resistor $R_1$ ensures that the input impedance to
the amplifier is sufficiently high. Its value can be quite high, say 100 k to 1 M since a very tiny current flows through into the gate of MOSFET because of its inherently high input resistance. Through this adjustment, the drain voltage is set at half the supply voltage for maximum symmetrical swing. If $R_2$ is sufficiently low, the circuit can be used to drive a speaker for audio output. In that case the quiescent current will be high, and therefore a heatsink will be required to keep MOSFET cool. For example, using a 9 V power supply and $R_2 = 50 \, \Omega$, adjustment of $VR_1$ for maximum symmetrical swing gives a drain voltage of $9/2 = 4.5$ V. Hence, the quiescent current through MOSFET is $4.5/50 = 90$ mA. In practice, $V_{DD}$ can be in the range of about 9 V to 24 V. Because of the high input resistance of MOSFET, capacitor $C_1$ can be a relatively low value of 1 $\mu$F. Since capacitor $C_2$ couples the output signal to a possibly low-impedance load such as headphones or a speaker, its value must be higher. $C_2 = 220$ $\mu$F has a reactance at 1 kHz of $10^6/2\pi \times 100 \times 220 = 7 \, \Omega$ which is comparable to an 8-Ω speaker load. A higher value capacitor will improve the low-frequency response of the circuit. Capacitor $C_3$ provides power supply filtering if necessary. The IRF510 MOSFET used in the circuit has a maximum drain–source voltage rating of 100 V and can handle drain currents of up to 5.6 A. It can dissipate 125 W of power. The threshold turn-on voltage is typically 3 V. As the quiescent current is increased, the increased power dissipation in the MOSFET may necessitate a heatsink (see Chap. 9). Finally, since the MOSFET can sink large current values on the negative half-cycle of the output signal while on the positive half-cycle output current must be sourced through resistor $R_2$, the output voltage will experience some asymmetry with the negative half-cycle being greater in amplitude than the positive half-cycle. This asymmetry will increase as the load resistor value decreases. A circuit example is shown in Fig. 3.58.
Fig. 3.57 MOSFET amplifier
Fig. 3.58 MOSFET amplifier with component values

Ideas for Exploration (i) Replace $R_2$ with an 8-Ω speaker and operate the circuit. Note that the current will always be flowing through the coil of the speaker. Investigate the issues associated with this, particularly speaker size.

3.7.7 DC Motor Speed Controller

This simple project is a DC motor speed controller based on an enhancement MOSFET such as the STP55NF06 in the source follower configuration (Fig. 3.59). The potentiometer $VR_1 = 100$ kΩ connected across the power supply applies a variable positive gate–source voltage that turns on MOSFET. The motor is connected between the source of MOSFET and ground, while the drain is connected to the 9 V supply. Thus, as the voltage on the wiper of the potentiometer is increased, the gate voltage is increased until the threshold voltage of MOSFET is exceeded and the device turns on. This voltage is transferred to the low-voltage DC motor $M$ which then operates. The speed of the motor increases as the voltage is increased. The value of the potentiometer is not critical, and the high input impedance of the FET allows the use of a high-value potentiometer such as 100 kΩ or higher.

Fig. 3.59 DC motor speed controller
Ideas for Exploration: (i) Replace the motor by a 9V lamp to realize one form of a lamp dimmer. (ii) Remove the motor and use the system as a variable bench supply by taking the voltage output from the source of MOSFET. How does the threshold voltage of MOSFET affect the operation of the circuit?

3.7.8 Light Dimmer

This is another simple circuit using the IRF540N enhancement MOSFET with a minimum threshold voltage of 2 V but now in the common drain mode (Fig. 3.60). A potentiometer $VR_1$ in series with a fixed resistor $R_1$ is connected across the power supply. The wiper of the potentiometer applies a variable positive gate–source voltage that turns on the MOSFET. The lamp is connected between the drain of the MOSFET and the 12 V supply. Thus, as the voltage on the wiper of the potentiometer is increased, the gate–source voltage is increased until the threshold voltage of the MOSFET is exceeded and the device turns on lighting the lamp. The brightness of the lamp is controlled by the amount of current flowing through the MOSFET which increases as the voltage is increased. The value of the potentiometer is not critical, and the high input impedance of the MOSFET allows the use of a high-value potentiometer such as 100 k or higher. If $VR_1 = 500$ k, then for $R_1 = 47$ k, the minimum voltage on the gate will be 1 V which is just below the threshold voltage for the MOSFET.
Idea for Exploration: (i) Replace the lamp by a 12-V DC motor and experiment with the resulting motor speed controller.

3.7.9 Adjustable Timer

The circuit in Fig. 3.61 is an adjustable timer. It uses the IRF510N enhancement MOSFET in the common drain configuration. When the switch is depressed, capacitor $C_1$ charges up to the supply voltage and turns on the MOSFET, thereby lighting the LED. Resistor $R_2 = 1 \, k$ limits the LED current to about 10 mA. When the switch is released, the capacitor $C_1$ discharges through $R_1$. When the capacitor voltage falls below the threshold voltage of the MOSFET, it turns off and also turns off the LED. For $C_1 = 500 \, \mu F$ and $R_1 = 10 \, k$, the discharge time is about 10s.
**Fig. 3.81** Adjustable timer

*Ideas for Exploration*: (i) Derive the equation \[ t = R_1C_1 \ln \left( \frac{V_f}{V_T} \right) \] for the discharge time of the capacitor through the resistor, given the initial voltage \( V_I \) and the threshold voltage of MOSFET \( V_T \). (ii) Vary the resistor and capacitor values to achieve different delay times. (iii) Experiment with different loads between the supply and the drain of MOSFET.

**3.7.10 Research Project 1**

This project involves the design of a circuit for checking inductance values. It uses the principle of series resonance which occurs in a series connection of an inductor and a capacitor when, at a particular
frequency, the magnitude of the reactance of the capacitor is equal to the magnitude of the reactance of the capacitor. In such a case, the voltages across these two components cancel and the circuit impedance is at a minimum. Current flow through the circuit is therefore at a maximum. The circuit in Fig. 3.62 operates on this basis. The JFET is connected in the source follower mode with a signal of variable frequency applied at the input. The output drives a capacitor $C_3 = 0.01 \mu F$ and the inductor $L$ to be tested with a microammeter inserted to measure current. In operation, a sinusoidal signal from an oscillator is passed into the system. Potentiometer $VR_1$ enables the adjustment of the amplitude of the signal. The frequency of the signal is adjusted over a wide range, and at the resonant frequency of the LC circuit, the current in the microammeter will increase sharply. The signal frequency and amplitude are adjusted until the maximum current increase occurs corresponding to almost full-scale deflection on the meter. At resonance, $2\pi fL = 1/2\pi fC$ giving $L = 10^9/395f^2$ in Henrys where $f$ is the frequency reading on the signal oscillator.

**Fig. 3.62** Inductance tester

**Ideas for Exploration:** (i) Test the system with some known inductances. (ii) Does the use of JFET confer any particular advantage to the circuit?

**3.7.11 Research Project 2**
This second research project investigates the internal structure of the MOSFET and in particular identifies and utilizes the internal capacitance between the gate and the source. The data sheet of the IRF1405 provides information on the gate–source capacitance for this device. The project involves using this device in a touch-sensitive switch that exploits this junction capacitance as shown in Fig. 3.63. It employs the IRF1405 enhancement MOSFET in the common source configuration. The relay is a 12 V device whose contacts connect a lamp or other appliance to the mains supply. Diode $D_1$ protects the MOSFET from back emf from the relay coil. When the contacts A are bridged by touch, charge is transferred from the supply to the internal gate–source capacitance of the MOSFET, thereby turning on the device. When the contacts B are touched, the capacitor is discharged and the MOSFET turns off. This system can be used in a variety of applications.

![Touch-sensitive switch](image)

*Fig. 3.63* Touch-sensitive switch

**Ideas for Exploration:** (i) Investigate the internal structure of the enhancement MOSFET and the junction capacitances that are used in the switching. (ii) Try using the system to switch on other devices such as a motor or radio.

### 3.7.12 Research Project 3
This research project uses the JFET to design a radio frequency signal booster as shown in Fig. 3.64 (a). This simple circuit uses an MPF102 or other suitable JFET in the common source mode. Resistor $R_1 = 1 \, M$ ensures that the gate is grounded for JFET biasing. $C_1 = C_2 = 1000 \, pF$ are coupling capacitors which can be small since the circuit is operating at high frequencies (540 kHz to 1600 kHz).

![Diagram](image)

**Fig. 3.64** Radio frequency signal booster (a) driving crystal radio (b)

The inductor $L_1 = 500 \, \mu H$ at 1MHz say has a reactance $X_L = 2\pi f L = 3.1k$. Therefore with $g_m \approx 5 \, mA/V$ for the MPF102, the circuit gain for signals at 1 MHz is $g_m X_L = 5 \, mA \times 3.1k = 15.5$. Capacitor $C_3 = 0.1 \, \mu F$ provides decoupling of the power supply to ensure reduced noise. The antenna to this circuit can now be a portable telescopic type or short piece of wire. The output of this RF signal booster goes to the tank circuit of the crystal radio of Fig. 1.71 in Chap. 1 as shown in Fig. 3.64 (b) and replaces the long-wire antenna of that system.

**Ideas for Exploration:** (i) Use the RF signal booster to replace the long-wire antenna in the crystal radio with single-transistor amplifier in Fig. 2.72 in Chap. 2. This would represent an enhanced crystal radio with RF signal booster and single-stage audio amplifier. Check if reception is improved; (ii) Use the RF signal booster to replace the long-wire antenna in the modified crystal radio in Fig. 2.73 in Chap. 2 and check if reception is improved.
Problems

1. Briefly explain the following:
   (a) The high input impedance of JFET.
   (b) The high input impedance of MOSFET.
   (c) The main difference between enhancement and depletion mode MOSFETS.
   (d) Pinch-off in JFET.
   (e) The difference between n-channel and p-channel JFETS.
   (f) The main similarity between BJT and an enhancement-type MOSFET.
   (g) The main similarity between JFET and a depletion-type MOSFET.

2. A JFET has a signal voltage of 0.75 Vpk value applied to its gate relative to its source. The drain current varies by ±1.5 mA about its quiescent value. Calculate $g_m$.

3. An n-channel JFET has $I_{DSS} = 6$ mA and $V_P = -5$ V. For a drain current of 4 mA, determine $g_m$ using Shockley’s equation. If this JFET is used in a common source amplifier with its source grounded for signals and drain resistance $R_L = 10$ k, determine the voltage gain from gate to drain.

4. Using fixed-bias, bias a n-channel JFET for a drain current of 3 mA using a device having $I_{DSS} = 7$ mA and $V_P = -4$ V. Use $V_{DD} = 14$ V and choose $R_L$ for maximum symmetrical swing.

5. Bias a p-channel JFET for a drain current of 2 mA using fixed-bias. For FET, $I_{DSS} = 12$ mA and $V_P = +5$ V. Use $V_{DD} = -18$ V and select $R_L$ for maximum symmetrical swing.
6. Using FET of problem 4 above, find $R_S$ to replace the fixed-bias voltage source $V_{GG}$.

7. Using Shockley’s equation $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$ and a 26 V supply, design a common source amplifier based on self-bias, using an n-channel JFET having a pinch-off voltage of −2.5 V and $I_{DSS} = 5$ mA. Use a 3 mA quiescent current. Use $g_m = -2 \sqrt{I_{DSS}}/V_P$ to calculate the voltage gain of your circuit.

8. Using an n-channel JFET having $I_{DSS} = 3$ mA and $V_P = -5.5$ V, bias the device using voltage divider biasing for a drain current of 2.5 mA. Design for a maximum symmetrical swing with $V_{DD} = 18$ V.

9. State the advantages and disadvantages of self-bias as compared with voltage divider bias in JFETs.

10. For the self-biased common source amplifier in problem 7, redesign the system to use a bipolar supply of ±15 V, returning $R_S$ to the negative supply voltage.

11. Using Shockley’s equation $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$ and a 27 V supply, design a common source amplifier using an p-channel JFET having a pinch-off voltage of +4 V and $I_{DSS} = 6$ mA. Use a 1 mA quiescent current and fixed-bias. Noting $g_m = -2 \sqrt{I_{DSS}}/V_P$, determine the voltage gain of your circuit.

12. Using Shockley’s equation $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$ and an 18 V supply, design a common source amplifier using an n-channel JFET having a pinch-off voltage of −3 V and $I_{DSS} = 4$ mA. Use voltage
divider bias and a 2 mA quiescent current. Explain the functions of the input gate resistor and the source resistor.

13. Using Shockley’s equation and a 24 V supply, design a common source amplifier using an n-channel depletion MOSFET having a pinch-off voltage of −4 V and \( I_{DSS} = 5 \) mA. Use a 5 mA quiescent current and self-bias. Calculate the voltage gain of your circuit using \( g_m = -2 \frac{\sqrt{I_p} \sqrt{I_{DSS}}}{V_P} \).

14. For the fixed-bias common source amplifier in problem 13, re-design the system to use a bipolar supply of ±22 V and return \( R_S \) to the negative supply voltage instead of ground.

15. Determine the drain current in the circuit shown in Fig. 3.65 if the quiescent gate–source voltage for JFET is −2.8 V.

16. Design a common drain amplifier using an n-channel JFET having \( I_{DSS} = 4.1 \) mA and \( V_P = -5.3 \) V and voltage divider biasing. Design for a maximum symmetrical swing with \( V_{DD} = 27 \) V.

17. Design a source follower circuit using a p-channel JFET with \( I_{DSS} = 8 \) mA, \( V_P = +2.3 \) V and a −12 V supply.

18. For the common drain amplifier in problem 16, re-design the system to use a bipolar supply of ±18 V and return \( R_S \) to the negative supply voltage instead of ground.

19. Design a common gate amplifier using an n-channel JFET having \( I_{DSS} = 3.2 \) mA and \( V_P = -1.9 \) V. Design for a maximum symmetrical swing with \( V_{DD} = 18 \) V.

20. Using self-bias, design a biasing network for a common source n-channel depletion-type MOSFET having \( I_{DSS} = 2.9 \) mA and \( V_P = -4.7 \) V. Design for maximum symmetrical swing.
21. Using an n-channel depletion MOSFET having $I_{DSS} = 3.7 \text{ mA}$ and $V_p = -3.9 \text{ V}$, bias the device for common source operation using voltage divider biasing and a drain current of 3 mA. Design for a maximum symmetrical swing with $V_{DD} = 16 \text{ V}$.

22. Repeat the design in problem 21 using a p-channel depletion MOSFET having $I_{DSS} = 4.1 \text{ mA}$ and $V_p = +4.7 \text{ V}$.

23. Design a common drain amplifier using an n-channel depletion MOSFET having $I_{DSS} = 5.9 \text{ mA}$ and $V_p = -6.1 \text{ V}$. Design for maximum symmetrical swing with $V_{DD} = 32 \text{ V}$.

24. Design a common gate amplifier using an n-channel depletion MOSFET with $I_{DSS} = 1.3 \text{ mA}$ and $V_p = -2.9 \text{ V}$. Design for maximum symmetrical swing using a 14 V supply.

25. Using the circuit shown in Fig. 3.66, design a feedback biasing network for an enhancement-type MOSFET having $V_T = 2.7 \text{ V}$, $I_{Don} = 5 \text{ mA}$, and $V_{GSon} = 7 \text{ V}$. Use $V_{DD} = 15 \text{ V}$.

26. Design a feedback biasing network for a common source enhancement-type p-channel MOSFET having $V_{GST} = 2.5 \text{ V}$, $I_{Don} = 4 \text{ mA}$, and $V_{GSon} = 7 \text{ V}$. Use $V_{DD} = 25 \text{ V}$.

27. Using the configuration in Fig. 3.67, design a modified feedback biasing network for a common source enhancement-type MOSFET having $V_T = 3.3 \text{ V}$, $I_{Don} = 6.4 \text{ mA}$, and $V_{GSon} = 5.3 \text{ V}$. The supply voltage is $V_{DD} = 12 \text{ V}$.

28. Using the configuration in Fig. 3.68, design a voltage divider-biased common source amplifier using an enhancement-type MOSFET having $V_T = 2.4 \text{ V}$ and $k = 0.07 \text{ mA/V}^2$, and use $V_{DD} = 22 \text{ V}$.

29. Using the configuration in Fig. 3.49, design a voltage divider-biased common drain amplifier using an enhancement-type n-channel MOSFET having $V_T = 2.4 \text{ V}$ and $k = 0.29 \text{ mA/V}^2$, and use $V_{DD} = 25 \text{ V}$. 
30. Using the configuration in Fig. 3.50, design a voltage divider-biased common gate amplifier using an enhancement-type MOSFET having $V_T = 2.1$ V and $k = 0.05$ mA/V$^2$, and use $V_{DD} = 30$ V.

Fig. 3.65 Circuit for Question 15
Fig. 3.66 Circuit of Question 25
Fig. 3.67  Circuit for Question 27
**Fig. 3.68** Circuit for Question 28

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**Bibliography**


In Chaps. 2 and 3, the bipolar junction transistor (BJT) and the field-effect transistor (FET) were introduced, and their operation was discussed. The need for biasing was established, and various biasing schemes were presented. Also, the operation of the BJT and FET as amplifiers each in three configurations was discussed. While the utilized methods gave reasonably good answers, more precise design requires the use of BJT and FET models or equivalent circuits. The models we adopt are the hybrid parameter or $h$-parameter model and the $y$-parameter model. These transistor parameters can, in general, be obtained from manufacturer’s data sheets. At the end of the chapter the student will be able to:

- Explain $h$- and $y$- parameters
- Use $h$- and $y$- parameters in the analysis of transistor circuits.

### 4.1 $h$-Parameters and the BJT

Small-signal amplifiers are amplifiers that are assumed to operate over the linear range of the active device (BJT or FET) by using only small-
signal voltages and currents. Therefore, the AC operation may be deduced by representing the transistor by an equivalent circuit consisting of linear signal generators and circuit elements. In deducing this equivalent circuit, the transistor is regarded as an active two-port network, as shown in Fig. 4.1, i.e., it has two input terminals and two output terminals. The BJT is considered first.

Fig. 4.1 Transistor as an active two-port network

There are four external variables: the input voltage and current $V_i$ and $I_i$ and output voltage and current $V_o$ and $I_o$. Since operation takes place over the linear range of transistor characteristics (small-signal operation), $V_i$, $I_i$, $V_o$ and $I_o$ can be related to each other by constant parameters. Thus, $V_i$ and $I_o$ can be related to $V_o$ and $I_i$, respectively, by four constants, called hybrid or $h$-parameters giving

\begin{align}
V_i &= h_i I_i + h_r V_o \\
I_o &= h_f I_i + h_o V_o
\end{align}

which can be represented as shown in Fig. 4.2. (Note that there are other ways of relating the four variables; see Sect. 4.5.)

Fig. 4.2 Transistor $h$-parameter equivalent circuit
Under small-signal conditions:

\[
\begin{align*}
  h_i &= \frac{V_i}{I_i} \bigg|_{V_o=0} \quad \text{input impedance with short-circuited output} \\
  h_f &= \frac{I_o}{I_i} \bigg|_{V_o=0} \quad \text{forward current gain with short-circuited output} \\
  h_r &= \frac{V_o}{V_i} \bigg|_{I_i=0} \quad \text{voltage feedback ratio with open-circuited input} \\
  h_o &= \frac{I_o}{V_o} \bigg|_{I_i=0} \quad \text{output admittance with open-circuited input}
\end{align*}
\]

(4.3) (4.4) (4.5) (4.6)

The values of these parameters depend on the transistor configuration. In order to distinguish among the three configurations, i.e., common emitter (CE), common base (CB), and common collector (CC), a second subscript is added to each \( h \)-parameter. Thus, for the CE configuration, \( h_i \) becomes \( h_{ie} \); for the CB, it is \( h_{ib} \); for the CC, it is \( h_{ic} \); and so on for the other parameters.

Now, for the CE configuration, \( h_{ie} \) is the ratio of a small change in input voltage (\( \Delta V_i \)) to the resulting small change in input current (\( \Delta I_i \)), which for this configuration is the input impedance. Hence, from (2.33) in Chap. 2,

\[
h_{ie} = \frac{h_{fe}}{40I_C}.
\]

(4.7)

Here, \( h_{fe} \) is the ratio of the change in output current to the change in input current producing it, and hence,

\[
h_{fe} = \beta.
\]

(4.8)

The actual value of \( h_{fe} \) is a function of the transistor collector current \( I_C \), temperature, and signal frequency. Figure 4.3 shows a typical
plot of $h_{fe}$ against collector current $I_C(mA)$.

![Graph of $h_{fe}$ against $I_C$](image)

**Fig. 4.3** Transistor current gain against collector current

It can be seen that $h_{fe}$ initially increases with collector current but reaches a maximum at around 40–50 mA. Manufacturers generally state the maximum value of $h_{fe}$ and the associated collector current at which it attains this value. A plot of current gain against temperature is shown in Fig. 4.4, where $h_{fe}$ increases with temperature by as much as twice its value over a temperature change from 20 to 80 °C. Finally, the current gain $h_{fe}$ of a transistor varies with signal frequency, its value falling off at higher frequencies. This is illustrated in Fig. 4.5. $f_\beta$ is the frequency at which the current gain falls by 3 dB of its low-frequency value and is referred to as the cut-off frequency of the transistor. The frequency at which the current gain falls to unity is called the transition frequency $f_t$. 
We are now ready to use the $h$-parameter CE amplifier analysis equivalent circuit to analyze an amplifier circuit. Specifically, we wish to study the CE amplifier configuration. Now, the $h$-parameter model is valid only for linear systems, and since the transistor characteristics are nonlinear, the signals must be restricted to small voltage and current.

4.2 Analysis of a Common Emitter Amplifier Using $h$-Parameters

We are now ready to use the $h$-parameter CE amplifier analysis equivalent circuit to analyze an amplifier circuit. Specifically, we wish to study the CE amplifier configuration. Now, the $h$-parameter model is valid only for linear systems, and since the transistor characteristics are nonlinear, the signals must be restricted to small voltage and current.
variations about the Q point such that the transistor operates approximately linearly. In such circumstances, the $h$-parameters can be used to analyze transistor networks for the small time-varying components of signals and not the DC component.

Consider the basic CE circuit shown in Fig. 4.6(a), in which the biasing components have been omitted for simplicity. In an AC equivalent circuit, the battery is a short circuit to AC. Thus, replacing the transistor by the $h$-parameter equivalent circuit yields Fig. 4.6(a), which becomes Fig. 4.6(b) after rearranging. This is called the AC equivalent circuit for the CE amplifier. Since $h_{re} \approx 0$ and assuming $1/h_{oe} \gg R_L$, then this circuit can be reduced to that shown in Fig. 4.7.

![Common Emitter Amplifier and its Equivalent Circuit](image)

**Fig. 4.6** (a) Common emitter amplifier and (b) its equivalent circuit

![Modified Equivalent Circuit](image)

**Fig. 4.7** Modified equivalent circuit

All of the linear circuit laws including those of Ohm, Thevenin, Norton, Kirchhoff, and the Superposition theorem can now be applied
since the nonlinear transistor has been linearized about the operating point. We can now derive an expression for the voltage gain $A_v$ of the amplifier, where $A_v = V_o / V_i$.

From Fig. 4.7, noting that $I_i = I_b$, where $I_b$ is the signal current flowing into the base of the transistor, and $I_o = I_c$, where $I_c$ is the signal current flowing into the collector,

$$V_o = -I_o R_L = -h_f I_b R_L \tag{4.9}$$

$$V_i = h_i I_b \tag{4.10}$$

Therefore, the voltage gain $A_v = V_o / V_i$ is given by

$$A_v = \frac{V_o}{V_i} = \frac{-h_f R_L}{h_i} \tag{4.11}$$

The negative sign is indicative of an inversion between the output voltage and the input voltage. Similarly, the current gain $A_i = I_o / I_i$ is given by

$$A_i = \frac{I_o}{I_i} = \frac{h_f I_b}{I_b} = h_f. \tag{4.12}$$

The input impedance $Z_i$ can be obtained from (4.10). $Z_i$ is the ratio of the applied input voltage $V_i$ to the input current $I_b$, i.e.,

$$Z_i = \frac{V_i}{I_b} = h_{ie} \tag{4.13}$$

In order to determine the output impedance $Z_o$, we first find the Thevenin equivalent of the amplifier output. Then, $Z_o = V_{os} / I_{sc}$, where $V_{oc}$ is the open-circuit voltage and $I_{sc}$ is the short-circuit current. The open-circuit output voltage is [from (4.9)]

$$V_{oc} = -h_f I_b R_L. \tag{4.14}$$

The short-circuit output current is obtained by short-circuiting the output, i.e., resistor $R_L$ giving

$$V_{os} = -h_f I_b R_L \tag{4.15}$$
\[ I_{sc} = -h_{fe}I_b. \]

Therefore, the output impedance is given by

\[ Z_o = \frac{V_{oc}}{I_{sc}} = \frac{-h_{fe}I_bR_L}{-h_{fe}I_b} = R_L. \] (4.16)

If the parameter \(1/h_{oe}\) is included, then it will appear in parallel with \(R_L\), and the open-circuit output voltage \(V_{oc}\) becomes

\[ V_{oc} = -h_{fe}I_bR_L/\frac{1}{h_{oe}}. \] The output impedance then becomes

\[ Z_o = R_L/\frac{1}{h_{oe}}. \] (4.17)

Consider now the practical CE amplifier circuit with fixed bias and coupling capacitors shown in Fig. 4.8(a). We assume that the capacitors are sufficiently large so that they are short circuits to AC for the frequencies involved. Noting again that the DC supply is a short circuit to AC, the \(h\)-parameter equivalent circuit is shown in Fig. 4.8(b). The resistor \(R_B\) connected to the transistor base is grounded through the DC supply. The expressions for the voltage gain and the output impedance are unaffected, but since \(R_B\) appears in parallel with \(h_{ie}\), the input impedance is reduced. Hence,

\[ Z_i = h_{ie} || R_B. \] (4.18)

![Fig. 4.8](image-url) (a) Fixed-bias common emitter amplifier with (b) equivalent circuit
The current gain $I_o/I_i$ is slightly reduced since some of the input signal current flow into $R_B$. However, since $R_B \gg h_{ie}$, this reduction is very small.

**Example 4.1** For the CE amplifier shown in Fig. 4.9, draw the equivalent circuit using $h$-parameters. Then, for a collector current of 1 mA, determine the voltage gain and input impedance.

![Common emitter amplifier](image)

**Fig. 4.9** Common emitter amplifier

**Solution** The equivalent circuit is shown in Fig. 4.10. For this circuit, $h_{ie} = \frac{h_{fe}}{40I_C} = \frac{100}{40 \times 1 \text{ mA}} = 2.5 \text{ k}$. Hence, from (4.18), the input impedance is given by $Z_i = 2.5 \text{ k} \parallel 1.93 \text{ M} \approx 2.5 \text{ k}$. From (4.11), the voltage gain is given by $A_V = \frac{-100 \times 10 \text{ k}}{2.5 \text{ k}} = -400$. 
Fig. 4.10 Equivalent circuit of common emitter amplifier

Example 4.2 The circuit of Example 4.1 is used to drive a 20-k load, as shown in Fig. 4.11. Draw the equivalent circuit using $h$-parameters and determine the voltage gain and input impedance.

Solution The only change in the equivalent circuit is the inclusion of the 20k load resistor in parallel with the 10k collector resistor, as
shown in Fig. 4.12. Thus, the input impedance remains the same, but the voltage gain is reduced to \[ A_V = \frac{-100 \times 10 \text{ k} / 20 \text{ k}}{2.5 \text{ k}} = -267. \]

**Fig. 4.12** Equivalent circuit of common emitter amplifier driving a load

For the CE amplifier with voltage-divider bias shown in Fig. 4.13, we approach the drawing of the AC equivalent as before.

**Fig. 4.13** Voltage divider-biased common emitter amplifier
We short-circuit all capacitors and the DC supply. The resulting AC equivalent circuit is shown in Fig. 4.14. Bias resistors $R_1$ and $R_2$ appear in parallel with $h_{ie}$ with no other changes. Hence, the voltage gain remains the same as in the fixed bias case, but the input impedance becomes $Z_i = R_1 \parallel R_2 \parallel h_{ie}$. The current gain changes since some of the signal current is lost in the bias resistors $R_1$ and $R_2$. The fraction that flows into the base $I_b/I_i$ is using the current divider theorem given by

$$\frac{I_b}{I_i} = \frac{R_1 \parallel R_2}{h_{ie} + R_1 \parallel R_2}.$$  \hspace{1cm} (4.19)

Fig. 4.14 Equivalent circuit of voltage divider-biased common emitter amplifier

Hence,

$$A_i = \frac{I_o}{I_i} = \frac{I_o}{I_b} \times \frac{I_b}{I_i} = h_{fe} \times \frac{R_1 \parallel R_2}{h_{ie} + R_1 \parallel R_2}.$$  \hspace{1cm} (4.20)

Thus, the current gain suffers attenuation when bias components are introduced. For the voltage-divider-biased CE circuit involving a source resistor $R_S$ connected in series with the input, as shown in Fig. 4.15, the equivalent circuit is shown in Fig. 4.16. $R_S$ in conjunction with the resistors $R_1, R_2$, and $h_{ie}$ forms a potential divider and, hence, introduces voltage signal attenuation. The voltage gain $A_V$ is given by

$$A_V = \frac{V_o}{V_i} = \frac{V_o}{V_b} \times \frac{V_b}{V_i}.$$  \hspace{1cm} (4.21)
where $V_b$ is the signal voltage at the base of the transistor. Now, from (4.11), we have

$$\frac{V_o}{V_b} = \frac{-h_{fe}R_L}{h_{ie}}$$  \hspace{1cm} (4.22)

and

$$\frac{V_b}{V_i} = \frac{Z'_{i}}{R_s + Z'_{i}}$$  \hspace{1cm} (4.23)

where

\begin{figure}
\centering
\includegraphics[width=\textwidth]{fig415}
\caption{Common emitter amplifier with input resistor}
\end{figure}
Fig. 4.16 Equivalent circuit of common emitter amplifier with input resistor

\[
Z'_i = \frac{R_1}{R_2}/h_{ie}.
\]  

(4.24)

Hence,

\[
A_V = \frac{-Z'_i}{R_S + Z'_i} \cdot \frac{h_{fe}R_L}{h_{ie}}.
\]  

(4.25)

The input impedance \(Z_i\) would now be \(Z_i = R_S + Z'_i\).

**Example 4.3**  For the circuit shown in Fig. 4.17, draw the \(h\)-parameter equivalent circuit and determine voltage gain, current gain, input impedance, and output impedance.
**Solution**  The equivalent circuit is shown in Fig. 4.18. The collector current is easily shown to be 1 mA, and hence,

\[ h_{ie} = \frac{h_{fe}}{40 I_C} = \frac{100}{40 \times 1 \text{ mA}} = 2.5 \text{ k}\. \] Hence the voltage gain is given by

\[ A_V = \frac{-100 \times 9}{2.5 \text{ k}} = -360. \] Using (4.20), current gain

\[ A_i = h_{fe} \times \frac{R_1 || R_2}{h_{ie} + R_1 || R_2} = 100 \times \frac{27 \text{ k}/173 \text{ k}/2.5 \text{ k} + 27 \text{ k}/173 \text{ k}} = 90. \] From (4.24), the input impedance is given by

\[ Z_i = \frac{R_1 || R_2}{h_{ie}} = 27 \text{ k}/173 \text{ k}/2.5 \text{ k} = 2.3 \text{ k}. \] The output impedance is simply the 9k load resistor.
If a 15k external load resistor is added to the circuit of Fig. 4.17, then the equivalent circuit in Fig. 4.18 is modified by the inclusion of a 15k load resistor in parallel with the 9k collector resistor. The voltage gain becomes $A_V = \frac{-100 \times 9\ \text{k}}{2.5\ \text{k}} = -225$. The current gain defined by the ratio of the current into the 15 k resistor to the input current is given by

$$A_i = h_{fe} \times \frac{R_1 || R_2}{h_{ie} + R_1 || R_2} \times \frac{9\ \text{k}}{9\ \text{k} + 15\ \text{k}} = 90 \times 0.375 = 33.8.$$ 

The input impedance remains the same.

### 4.2.1 Common Emitter Amplifier with Partial Decoupling

The next amplifier to be discussed is the CE amplifier shown in Fig. 4.19, in which the emitter resistor is only partially bypassed. The equivalent circuit is shown in Fig. 4.20. Note that while $R_E$ is short-circuited by the capacitor $C_3$, $R_e$ is not and, therefore, appears in the equivalent circuit. Note that both $I_b$ and $h_{fe}I_b$ flow into $R_e$. Hence, at the input, we have

$$V_i = I_b h_{ie} + (I_b + h_{fe}I_b) R_e = I_b \left( h_{ie} + \left(1 + h_{fe}\right) R_e \right). \quad (4.26)$$
Fig. 4.19 Common emitter amplifier with partially decoupled emitter resistor
At the output, we have

\[ V_o = -h_{fe} I_b R_L. \] (4.27)

Hence, the voltage gain of the circuit is given by

\[ A_V = \frac{V_o}{V_i} = \frac{-h_{fe} R_L}{h_{ie} + (1 + h_{fe}) R_e}. \] (4.28)

Since \( h_{fe} \) is large, \( 1 + h_{fe} \approx h_{fe} \). Therefore, dividing through by \( h_{fe} \), we get

\[ A_V = \frac{-R_L}{R_e + r_e}, \text{ where } r_e = h_{ie}/h_{fe}. \] (4.29)

If \( R_e \) is large, then \( R_e \gg r_e \), and (4.29) reduces to

\[ A_V \approx \frac{-R_L}{R_e}. \] (4.30)

The output impedance is the ratio of the open-circuit output voltage to the short-circuit output current, i.e.,

\[ Z_o \equiv \frac{1}{A_V}. \] (4.31)
The circuit input impedance is found by first finding the ratio \( V_i/I_b \) which is from (4.26)

\[
Z_o = \frac{-h_{fe}I_b R_L}{-h_{fe}I_b} = R_L.
\]

From Fig. 4.20, this impedance is clearly in parallel with \( R_1 \) and \( R_2 \) and hence

\[
Z' = \frac{V_i}{I_b} = h_{ie} + \left(1 + h_{fe}\right) R_e.
\] (4.32)

Comparing this circuit with the CE amplifier with completely bypassed emitter resistor, first, the voltage gain magnitude goes from \( h_{ie} \), i.e., the presence of \( R_e \) significantly reduces the voltage gain. Second, the input impedance changes from \( h_{ie} \) to \( h_{ie} + (1 + h_{fe}) R_e \) (ignoring the effect of \( R_1 \) and \( R_2 \)), i.e., \( R_e \) causes a significant increase in the input impedance, looking into the transistor base. In practice, however, \( R_1 \) and \( R_2 \) limit the input impedance increase.

**Example 4.4** In the circuit of Fig. 4.17, consider the case where the emitter resistor is split such that only 1.6 \( \Omega \) is bypassed. Determine the voltage gain and input impedance.

**Solution** Using the circuit values of Fig. 4.17 and the nomenclature of Fig. 4.19, \( R_e = 400 \) and \( R_E = 1.6 \) k. Then, from (4.29), the voltage gain is given by \( A_V = \frac{-9}{0.4 + 0.025} = -21 \). This is significantly reduced from the original value of \( A_V = \frac{-9}{0.025} = -360 \) as a result of the presence of the unbypassed 400\( \Omega \) resistor. This resistor also affects the input resistance, which becomes

\[
Z_i = 27 \text{k}{//}173 \text{k}{|}(2.5 \text{k} + (1 + 100)0.4 \text{k}) = 27 \text{k}{//}173 \text{k}{//}42.9 \text{k} = 11 \text{k}.
\]
The reduction of gain resulting from the inclusion of $R_e$ in the emitter circuit of a CE amplifier allows the design of such amplifiers for both maximum symmetrical swing and a specific (reduced) gain.

**Example 4.5** Using the partially bypassed configuration in Fig. 4.19, design a CE amplifier having a gain of 50, using a 2N3904 npn transistor and a 24V power supply. Determine the input impedance.

**Solution** Choosing a quiescent current of 1 mA, the design procedure for maximum symmetrical swing in a voltage-divider CE amplifier in Chap. 2 yields $R_E = 2.4 \, k$, $R_L = 10.8 \, k$, $R_1 = 209 \, k$ and $R_2 = 31 \, k$. Using (4.29) for the voltage gain of the partially bypassed configuration and noting that $r_e = 1/40I_C = 25 \, \Omega$, $50 = \frac{-10800}{R_e + 25}$ giving $R_e = 191 \, \Omega$. Thus, the emitter resistor $R_E = 2.4 \, k$ must be split into $R_E = 2.2 \, k$ and $R_e = 191 \, \Omega$. The input impedance is given by

$$Z_i = 31 \, k \parallel 209 \, k \parallel (2.5 \, k + (1 + 100)0.191 \, k) = 31 \, k \parallel 209 \, k \parallel 21.8 \, k = 12.1 \, k.$$  

**4.2.1.1 Bootstrapping**

In order to reduce the effect of $R_1$ and $R_2$ and thereby realize higher input impedance, bootstrapping can be employed in the partially bypassed circuit of Fig. 4.19. The technique involves (i) the introduction of resistor $R_B$ between the transistor base and the junction of $R_1$ and $R_2$ and (ii) the introduction of a capacitor $C_B$ between the transistor emitter and the junction of $R_1$, $R_2$ and $R_B$, as shown in Fig. 4.21. As usual, all capacitors are assumed to be large enough to be short circuit to AC. Using the simplified model of the BJT, the equivalent circuit representing the bootstrapped circuit is shown in Fig. 4.22. Let $R'_e = R_1 \parallel R_2 \parallel R_e$. From Kirchhoff’s voltage law (KVL), we have

$$I_b h_{ie} = I_x R_B$$  \hspace{1cm} (4.34)

giving $R'_e$.
Fig. 4.21  Bootstrapping in a common emitter amplifier
Using KVL at the input of the circuit, we have

\[ V_i = I_b h_{ie} + I_b \left( 1 + h_{fe} + \frac{h_{ie}}{R_B} \right) R'_e. \]  \hspace{1cm} (4.36)

Hence, the input impedance to the circuit is given by

\[ Z_i = \frac{V_i}{I_b + I_x} = \frac{V_i}{I_b \left( 1 + h_{ie}/R_B \right)} = \frac{h_{ie} + \left( 1 + h_{fe} + \frac{h_{ie}}{R_B} \right)}{1 + \frac{h_{ie}}{R_B}}. \]  \hspace{1cm} (4.37)

If \( R_B \gg h_{ie} \), then (4.37) reduces to

\[ Z_i = h_{ie} + \left( 1 + h_{fe} \right) R'_e. \]  \hspace{1cm} (4.38)

Thus, the original circuit input impedance
\[ Z_i = R_1 \| R_2 \left( h_{ie} + (1 + h_{fe}) R_e \right) \] becomes
\[ Z_i = h_{ie} + (1 + h_{fe}) \left( R_1 \| R_2 \| R_e \right), \] and
the effect of $R_1$ and $R_2$ is reduced. Note, however, that bias stability is also reduced since the effective source resistance of the voltage divider bias changes from $R_1 \parallel R_2$ to $R_1 \parallel R_2 + R_B$. Because of this, the DC voltage across $R_B$ should be small compared with the DC voltage across $R_E + R_e$.

The voltage gain of the circuit can also be determined. From Fig. 4.22, the output voltage is given by

$$V_o = -h_{fe}I_bR_L.$$  \hfill (4.39)

Hence, using (4.36) for $V_i$, the voltage gain $A_V$ is given by

$$A_V = \frac{V_o}{V_i} = -\frac{h_{fe}R_L}{h_{ie} + (1 + h_{fe} + h_{ie}/R_B)R'_e}. \hfill (4.40)$$

This reduces to

$$A_V = -\frac{h_{fe}R_L}{h_{ie} + (1 + h_{fe})R'_e}, \quad R_B \gg h_{ie}. \hfill (4.41)$$

Thus, the gain of the original circuit is virtually unchanged. If a resistor $R'_L$ is connected to $C_2$ and grounded, this represents a load on the CE amplifier. This resistor appears in parallel with $R_L$ in the equivalent circuit. Hence, $R_L \rightarrow R_L \parallel R'_L$. The effect of this is to reduce the voltage gain $A_V$. Thus, loading the CE amplifier reduces the voltage gain.

**Example 4.6** Improve the input impedance of the partially bypassed configuration in Example 4.5 using bootstrapping.

**Solution** Bootstrapping requires the introduction of resistor $R_B$ into the circuit. In order to maintain quiescent current stability, the voltage across $R_B$ must be significantly less than the voltage at the emitter which is 2.4 V. Using $V_{RB} = 0.24$ V, then with a base current of $1 \text{ mA}/h_{fe} = 0.01 \text{ mA}$, the value of $R_B$ is $R_B = 0.24 \text{ V}/0.01 \text{ mA} = 24 \text{ k}$.

Hence, the new input impedance is given by $Z_i = 2.5 \text{ k} + (1 + 100)$
\(31 \, k\parallel 209 \, k\parallel 0.19 \, k\) = 21.5 \, k, which is significantly larger than the original value.

4.2.1.2 Alternative Amplifier Configuration

The amplifier discussed in Fig. 4.19, in which the emitter resistor is only partially bypassed, had a lower but less variable gain. We now consider an alternative version shown in Fig. 4.23, in which the emitter resistor \(R_E\) is bypassed by a resistor \(R_e\) in series with capacitor \(C_3\). The form of equivalent circuit is shown in Fig. 4.20. Note that \(R_E\) is not short-circuited by the capacitor \(C_3\), which is in series with resistor \(R_e\). Therefore, in the equivalent circuit, \(R_E\) and \(R_e\) appear in parallel, and \(C_3\) is a short circuit for signals. Hence, the equivalent circuit is shown in Fig. 4.24, and the expressions for voltage gain and input impedance are the same for both circuits with \(R_e \rightarrow R_E\parallel R_e\), which reduces to \(R_e\) for \(R_E \gg R_e\).
Fig. 4.23  Alternative common emitter amplifier
4.2.2 Common Emitter Amplifier with Collector–Base Feedback Bias

The $h$-parameter equivalent circuit will be used to analyze the CE amplifier with collector–base feedback biasing. The configuration is shown in Fig. 4.25, and the equivalent circuit is shown in Fig. 4.26. Here, the resistor $R_F$ connects the collector to the base. From Fig. 4.26, the input and output voltages are given by

$$V_i = I_b h_{ie}$$

(4.42)
Fig. 4.25  Common emitter amplifier with collector–base feedback bias

Fig. 4.26  Equivalent circuit of amplifier with collector–base feedback bias

\[ V_o = \left( -h_{fe} I_b - I_F \right) R_L \]  \hspace{1cm} (4.43)

where

\[ I_F = \frac{V_o - V_i}{R_F}. \]  \hspace{1cm} (4.44)

Substituting (4.44) into (4.43), we get
\[ V_o = I_b \frac{R_L R_F}{R_L + R_F} \left( h_{ie} - h_{fe} R_F \right) = I_b R_L // R_F \left( \frac{h_{ie} - h_{fe} R_F}{R_F} \right). \]  \hfill (4.45)

Hence, the voltage gain is given by

\[ A_V = \frac{V_o}{V_i} = \frac{R_L // R_F \left( \frac{h_{ie} - h_{fe} R_F}{R_F} \right) / R_F}{h_{ie}} = R_L // R_F \left( 1 - \frac{h_{fe} R_F}{h_{ie}} \right) / R_F. \]  \hfill (4.46)

Since \( h_{fe} R_F / h_{ie} \gg 1 \), \( (4.46) \) reduces to

\[ A_V = -h_{fe} R_L / h_{ie}. \]  \hfill (4.47)

Note that if \( R_F \to \infty \) (i.e., removed from the circuit), then \( (4.47) \) reduces to

\[ A_V = -h_{fe} R_L / h_{ie} \]  \hfill (4.48)

which is the standard equation for the voltage gain of the fixed or voltage-divider-biased CE amplifier. The input impedance to this circuit can be found from \( Z_i = V_i / I_i \), where \( I_i \) is the total current flowing into the input of the circuit. Noting that \( I_i = I_b - I_F \), the input admittance \( Y_i = 1/Z_i \) is given by

\[ Y_i = \frac{I_i}{V_i} = \frac{I_b - I_F}{V_i} = \frac{I_b}{V_i} + \frac{-I_F}{V_i} = Y_b + Y_F \]  \hfill (4.49)

where \( Y_b = I_b / V_i \) and \( Y_F = -I_F / V_i \) are the input admittances making up \( Y_i \). From \( (4.42) \), \( Y_b = I_b / V_i = 1/h_{ie} \). From \( (4.44) \),

\[ I_F = (V_o - V_i) / R_F = (A_V - 1) V_i / R_F. \]  \hfill (4.50)

Hence,

\[ Y_F = -I_F / V_i = (1 - A_V) / R_F. \]  \hfill (4.51)

Therefore,

\[ Y_i = \frac{I_i}{V_i} = Y_b + Y_F = \frac{1}{h_{ie}} + \frac{1 - A_V}{R_F}. \]  \hfill (4.52)
This corresponds to two impedances in parallel given by

\[ Z_i = 1/Y_i = h_{ie}/R_F/(1 - A_V). \]

(4.53)

**Example 4.7**  The CE amplifier in Fig. 4.27 is biased for maximum symmetrical swing. Determine the voltage gain and the input impedance for the circuit.

![Circuit for Example 4.7](image)

**Solution**  Since the circuit is biased for maximum symmetrical swing, it follows that the collector voltage is half the supply voltage, i.e., 10 V. Hence, the transistor collector current is \(10/3.3 \text{ k} = 3 \text{ mA}\). The transistor base current is \((10 - 0.7)/470 \text{ k} = 0.02 \text{ mA}\). Hence, the current gain of the transistor is \(h_{fe} = 3 \text{ mA}/0.02 \text{ mA} = 150\). Therefore, \(h_{ie}\) for the transistor is \(h_{ie} = h_{fe}/40I_c = 150/40 \times 3 \text{ mA} = 1.25 \text{ k}\). From the expression \((4.48)\), the voltage gain for the circuit of Fig. 4.27 is given
by \( A_V = -h_{fe}R_L/h_{ie} = -150 \times 3.3/1.25 = -396 \). Using (4.43), the input impedance \( Z_i = 1.25k/\left(470k/1+396\right) = 0.6k \).

Thus, the input impedance of the CE amplifier with collector–base feedback bias is reduced from \( h_{ie} \) to \( h_{ie}R_F/\left(1 - A_V\right) \), where the feedback network causes the reduction. This effect can be virtually eliminated by splitting \( R_F \) into two resistors and connecting the junction to ground with a capacitor, as shown in Fig. 4.28. With this arrangement, the changed input impedance becomes \( h_{ie}R_{F_1} \), which is approximately \( h_{ie} \) since \( R_{F_1} \gg h_{ie} \).

\[ \text{Fig. 4.28} \quad \text{Common emitter amplifier with modified collector–base feedback bias} \]

The gain of the CE amplifier with collector–base feedback biasing can be stabilized by the inclusion of an emitter resistor, as shown in Fig. 4.29. The equivalent circuit is shown in Fig. 4.30. Here, the resistor \( R_E \) is introduced in the emitter circuit. From Fig. 4.30, the input and output voltages are given by

\[ V_i = I_b\left[h_{ie} + \left(1 + h_{fe}\right)R_E\right] \quad (4.54) \]
\[ V_o = \left( -h_{fe}I_b - I_F \right) R_L \]  \hspace{1cm} (4.55)

where

\[ I_F = \frac{(V_o - V_i)}{R_F}. \]  \hspace{1cm} (4.56)

**Fig. 4.29** Collector–base feedback bias amplifier with an emitter resistor
Substituting (4.56) and (4.54) into (4.55), we get

\[
V_o = -h_{fe}I_bR_L - \frac{R_L}{R_F}(V_o - V_i) = I_b\frac{R_LR_F}{R_L + R_F}\left(-h_{fe} + \frac{h_{ie} + (1 + h_{fe})R_E}{R_F}\right).
\] (4.57)

Hence, the voltage gain is given by

\[
A_V = \frac{V_o}{V_i} = \frac{R_L/R_F\left(-h_{fe} + \frac{h_{ie} + (1 + h_{fe})R_E}{R_F}\right)}{h_{ie} + (1 + h_{fe})R_E}.
\] (4.58)

For \(R_F \gg R_E, h_{ie}, R_L\), (4.58) reduces to

\[
A_V = \frac{V_o}{V_i} = \frac{-h_{fe}R_L}{h_{ie} + (1 + h_{fe})R_E} = \frac{-R_L}{R_E + r_e} \approx \frac{-R_L}{R_E}, R_E \gg r_e.
\] (4.59)

Determination of the input impedance follows the steps of the circuit without \(R_E\) with the input admittance given by

\[
Y_i = \frac{I_i}{V_i} = \frac{I_b - I_F}{V_i} = \frac{I_b}{V_i} + \frac{-I_F}{V_i} = Y_b + Y_F.
\] (4.60)

From (4.42),

\[
\] (4.61)
From (4.44),

\[
I_F = \frac{(V_o - V_i)}{R_F} = (A_V - 1) \frac{V_i}{R_F}
\]

where \(A_V = -\frac{R_L}{(R_E + r_e)}\).

Hence,

\[
Y_F = -\frac{I_F}{V_i} = \frac{(1 - A_V)}{R_F}.
\]

Therefore,

\[
Y_i = \frac{I_i}{V_i} = Y_b + Y_F = \frac{1}{h_{ie} + \left(1 + h_{fe}\right)R_E} + \frac{1 - A_V}{R_F}.
\]

This corresponds to two impedances in parallel given by

\[
Z_i = \frac{1}{Y_i} = \frac{1}{h_{ie} + \left(1 + h_{fe}\right)R_E} \| \frac{1}{R_F/(1 - A_V)}.
\]

If the \(R_F\)-splitting arrangement used above is employed here, then \(Z_i\) becomes \(Z_i = \frac{1}{Y_i} = \frac{1}{h_{ie} + \left(1 + h_{fe}\right)R_E} \| \frac{R_E}{R_F/(1 - A_V)}\), which is higher.

Example 4.8 Using a supply voltage of 24 V, design a collector–base feedback-biased CE circuit with fixed gain of 10 using an emitter resistor as in Fig. 4.29 and a transistor with \(h_{fe} = 125\).

Solution Let \(I_{cq} = 2 \text{ mA}\). For maximum symmetrical swing \(V_{RL} \approx V_{CE} = a\). Further, for a gain of 10, \(R_L = 10R_E\), and therefore, the quiescent voltage across \(R_E\) is \(V_{RE} = a/10\). It follows that

\[24 = a + a + a/10\], which yields \(a = 11.4\) V. Hence, \(R_L = 11.4/2 \text{ mA} = 5.7\) kΩ and \(R_E = 1.14/2 \text{ mA} = 570\) Ω. The collector voltage \(V_C\) of the transistor is

\[V_C = V_{CE} + V_{RE} = 11.4 + 1.14 = 12.54\] V, the base voltage

\[V_B = 1.14 + 0.7 = 1.84\] V, and the base current is

\[I_{Bq} = I_{cq}/h_{fe} = 2 \text{ mA}/125 = 0.016\] mA.
Therefore, \( R_F = \frac{(V_C - V_B)}{I_{Bq}} = \frac{(12.54 - 1.84)}{0.016 \text{ mA}} = 669 \text{ k} \Omega \).

### 4.3 Analysis of the Common Collector Amplifier Using \( h \)-Parameters

In this section, we will utilize the CE \( h \)-parameter CC amplifier analysis BJT equivalent circuit to analyze the CC amplifier. Consider the basic CC circuit shown in Fig. 4.31(a), in which bias components have been excluded. The equivalent circuit using CE \( h \)-parameters is shown in Fig. 4.31(b). Using previous approximations, since \( h_{re} \approx 0 \), \( h_{re} V_{ce} \) can be neglected, and if \( 1/h_{oe} \gg R_E \), it can also be neglected. Using KVL, we obtain

\[
V_i = I_b (h_{ie}) + (1 + h_{fe}) i_b R_E
\]  

\[
V_o = (1 + h_{fe}) I_b R_E.
\]

![Common Collector Amplifier and Equivalent Circuit](image)

**Fig. 4.31** (a) Common collector amplifier circuit and (b) equivalent circuit

Hence, the voltage gain \( A_V \) from base to emitter is given by

\[
(4.68)
\]
\[ A_V = \frac{V_o}{V_i} = \frac{(1 + h_{fe}) I_b R_E}{((1 + h_{fe}) R_E + h_{ie}) I_b} = \frac{R_E}{R_E + r_e}. \]

From (4.68), it follows that \( A_V < 1 \). Since \( r_e \ll R_E \) in most instances, \( A_V \approx 1 \) for the CC amplifier. Note that output and input voltages are in phase. To calculate the input impedance, we need to find the ratio \( V_i/I_b \).

From (4.66), we have

\[ Z_i = \frac{V_i}{I_b} = h_{ie} + (1 + h_{fe}) R_E. \]  \hspace{1cm} (4.69)

Thus, the input impedance is quite large since \( h_{fe} \gg 1 \). For voltage divider biasing, two bias resistors \( R_1 \) and \( R_2 \) would now appear in parallel with \( Z_i \) such that the reduced input impedance is given by

\[ Z_i = \frac{1}{1/R_1 + 1/R_2} (h_{ie} + (1 + h_{fe}) R_E). \]  \hspace{1cm} (4.70)

In order to calculate the output impedance, we short-circuit the input voltage source and apply a voltage \( V \) at the output and find the corresponding current \( I \) flowing into the emitter (ignoring \( R_E \)), as shown in Fig. 4.32. Here, \( R_S \) is the source resistance.

\[ \text{Fig. 4.32} \text{ Determining output impedance of a common collector amplifier} \]

Then,
\[ V = I_b (h_{ie} + R_S) \]  \hspace{1cm} (4.71)

\[ I = I_b \left( 1 + h_{fe} \right). \]  \hspace{1cm} (4.72)

Hence,

\[ Z_o = \frac{V}{I} = \frac{R_S + h_{ie}}{1 + h_{fe}} = \frac{R_S}{h_{fe}} + r_e. \]  \hspace{1cm} (4.73)

Since this is in parallel with \( R_E \), then \( Z_o = R_E || Z_o \). Usually, \( Z_o \ll R_E \) giving \( Z_o = \frac{R_S}{h_{fe}} + r_e \). The output impedance of the CC amplifier is quite low.

**Example 4.9**  For the amplifier circuit shown in Fig. 4.33, determine the voltage gain, input impedance and output impedance.
Solution  Using (4.68), the voltage gain is given by

\[ A_v = \frac{R_E}{R_E + r_e} = \frac{10 \text{ k}}{10 \text{ k} + 0.25 \text{ k}} \approx 1. \]

The input impedance is given by

\[ Z_i = 93\text{ k}/(2.5 \text{ k} + (1 + 100)10 \text{ k}) = 47.4 \text{ k}, \]  
where \( h_{ie} = 2.5 \text{ k}. \) The output impedance is \( Z_o = r_e = 25 \Omega. \)

The high input impedance and low output impedance of the CC amplifier makes it ideal for coupling the output of the CE amplifier to a load as shown in Fig. 4.34. The high input impedance prevents the loading of the collector of the CE amplifier, which would lower the voltage gain, while the low output impedance means that most of the output voltage is dropped across the external load. A further advantage of this two-transistor arrangement is that the CC amplifier can be directly coupled to the collector of the CE amplifier, thereby eliminating the need for a coupling capacitor between these stages. The
voltage gain from the input of the first transistor to the output of the second remains approximately the same. This arrangement will be explored in Chap. 5.

![Two-stage amplifier using the common collector amplifier](image)

**Fig. 4.34** Two-stage amplifier using the common collector amplifier

### 4.3.1 Bootstrapping

It was seen in (4.70) that the input impedance of the CC amplifier is reduced by the voltage-divider biasing resistors. The bootstrapping technique used in the partially bypassed CE amplifier to overcome this problem can also be used in the CC amplifier, as shown in Fig. 4.35. The analysis is essentially the same with the emitter resistor $R_E$ in the CC amplifier replacing the un-bypassed emitter resistor $R_e$. 
Example 4.10  Improve the input impedance of the CC amplifier in Example 4.9 using bootstrapping.

Solution  Bootstrapping requires the introduction of resistor $R_B$ into the circuit. In order to maintain quiescent current stability, the voltage across $R_B$ must be significantly less than the voltage at the emitter which is 2.4 V. Using $V_{RB} = 0.24$ V, then with a base current of $1 \text{ mA}/h_{fe} = 0.01 \text{ mA}$, the value of $R_B$ is

$$R_B = 0.24 \text{ V}/0.01 \text{ mA} = 24 \text{ k} \gg h_{ie} = 2.5 \text{ k}.$$  

Hence, the new input impedance is given by $Z_i = 2.5 \text{ k} + (1 + 100)(93 \text{ k}||107 \text{ k}||10 \text{ k}) = 844 \text{ k}$, which is significantly larger than the original value of 47 k.
4.4 Analysis of the CB Amplifier Using $h$-Parameters

Here, we analyze the third configuration, namely, the CB amplifier, using CE $h$-parameters. A biased CB amplifier is shown in Fig. 4.36. Assuming $h_{re} V_{ce} \approx 0$ and $1/h_{oe}$ is large, the equivalent circuit reduces to that shown in Fig. 4.37. The input voltage $V_i$ is given by

$$V_i = -I_b h_{ie}$$  \hfill (4.74)

while

$$V_o = -h_{fe} I_b R_L.$$  \hfill (4.75)

Fig. 4.36  Common base amplifier
Hence, the voltage gain is given by

\[
A_v = \frac{V_o}{V_i} = \frac{-I_b h_{fe} R_L}{-I_b h_{ie}} = \frac{h_{fe} R_L}{h_{ie}} = \frac{R_L}{r_e}. \tag{4.76}
\]

Note that the voltage gain for the CB amplifier has the same magnitude as that for the CE amplifier, but unlike the CE amplifier, the output and input voltages are in phase. In the CE amplifier, the output voltage is 180° out of phase with the input voltage (represented by a negative sign), while in the CB amplifier the output voltage is in phase with the input voltage.

To calculate the input impedance, \(Z_i\), we evaluate the input current \(I_i\) flowing into the emitter of the BJT:

\[
I_i = -I_b \left(1 + h_{fe}\right) \tag{4.77}
\]

\[
V_i = -I_b h_{ie}. \tag{4.78}
\]

Hence,

\[
Z_i = \frac{V_i}{I_i} = \frac{h_{ie}}{1 + h_{fe}} = r_e. \tag{4.79}
\]

Hence, the input impedance of the CB amplifier is quite low and is comparable in value to the output impedance of the CC amplifier. This value is lowered even further by \(R_E\) which is effectively in parallel with
\[ Z_i, \text{i.e., } Z_i = r_e \parallel R_E \text{. By short-circuiting the input and applying a voltage at the output, the output impedance } Z_o \text{ is easily shown to be } Z_o = R_L. \]

We wish to determine the output impedance \( Z_o \) of a CB amplifier looking in at the transistor collector (and ignoring the collector resistor \( R_L \)), with an input signal that is associated with a high source impedance, i.e., a current source input signal as shown in Fig. 4.38. The equivalent circuit is shown in Fig. 4.39 with \( R_E \gg h_{ie} \). With an open-circuited input, a voltage \( V \) is applied at the collector and the resulting current \( I \) determined. Then,

\[ I = h_{fe} I_b + I_x = -I_b \tag{4.80} \]

which yields

\[ I_x = -\left(1 + h_{fe}\right) I_b \tag{4.81} \]

\[ V = I_x \left(1/h_{oe}\right) - I_b h_{ie} = -\left(1 + h_{fe}\right) I_b \left(1/h_{oe}\right) - I_b h_{ie}. \tag{4.82} \]
Fig. 4.38 Current-driven common base amplifier

Fig. 4.39 Determination of the output impedance of a common base amplifier

Hence,

\[
Z_o = \frac{V}{I} = \frac{-I_b \left[ (1 + h_{fe}) \left( \frac{1}{h_{oe}} \right) + h_{ie} \right]}{-I_b} = \left(1 + h_{fe}\right) \left( \frac{1}{h_{oe}} \right) + h_{ie}. \quad (4.83)
\]
Hence, the output impedance of a current-driven CB amplifier is extremely high.

**Example 4.11** For the CB amplifier shown in Fig. 4.40, determine the voltage gain, input impedance and output impedance.

![Common base amplifier for Example 4.11](image)

**Solution** The voltage gain is $A_v = \frac{9 \text{k}}{0.25} = 360$, while the input impedance is given by $Z_i = r_e || R_E$. This yields $Z_i = 0.025 \text{k} || 2 \text{k} \approx 25$. The output impedance $Z_o = 9 \text{k}$.
4.5 $y$-Parameters and the FET

As in the case of the BJT, small-signal operation of the FET assumes device operation over the linear range. Hence, the AC operation may be realized by representing the FET by an equivalent circuit comprising linear signal generators and other linear circuit elements. The FET is regarded as an active two-port network with the input and output currents and voltages related by constant parameters, as shown in Fig. 4.41. If the voltages are represented as the independent variables and the currents the dependent variables, then the constants are referred to as $y$-parameters with

$$I_o = y_f V_i + y_o V_o$$  \hspace{1cm} (4.84)

$$I_i = y_i V_i + y_r V_o.$$  \hspace{1cm} (4.85)

![Fig. 4.41 Linear circuit representation of FET](image)

We use these parameters to derive the equivalent circuit for the FET shown in Fig. 4.42. From Chap. 3, the output and input currents were given by

$$I_o = g_m V_i + \frac{1}{r_d} V_o$$  \hspace{1cm} (4.86)

$$I_i = \frac{1}{r_i} V_i \approx 0.$$  \hspace{1cm} (4.87)

where $g_m$ is the transconductance of the FET, $r_d$ is the output resistance and $r_i$ is the input resistance. Comparing (4.84) and (4.85) with (4.86) and (4.87) gives $y_f = g_m, y_o = 1/r_d, y_i = 1/r_i$ and $y_r = 0$. The BJT $h$-
parameter equivalent circuit can also be represented using $y$-parameters. Thus, using $h_{re} \approx 0$, from Sect. 4.1, we have

$$I_o = \frac{h_f}{h_i} V_i + h_o V_o$$  \hspace{1cm} (4.88)

$$I_i = \frac{1}{h_i} V_i$$  \hspace{1cm} (4.89)

and the BJT $y$-parameters can be determined by comparing (4.88) and (4.89) with the defining eqs. (4.86) and (4.87). Here, $y_f \equiv \frac{h_f}{h_i}$, and this is the trans-conductance $g_m$ of the BJT. This result was stated in Chap. 4. $y_o \equiv h_o$ is the output admittance and $y_i = 1/h_i$ is the input admittance. The resulting equivalent circuit is shown in Fig. 4.43.

![Equivalent circuit representation of FET](image)

*Fig. 4.42* Equivalent circuit representation of FET
4.6 Analysis of the Common-Source JFET Amplifier

The basic common-source amplifier with a fixed bias is shown in Fig. 4.44(a). The corresponding $y$-parameter model is shown in Fig. 4.44(b).

The analysis of this circuit is quite straightforward. The output voltage is given by
\[ V_o = -g_m V_{GS} R_L / r_d \approx -g_m V_{GS} R_L, R_L \ll r_d. \]  

(4.90)

Hence, the voltage gain \( A_V \) is given by

\[ A_V = \frac{V_o}{V_i} = -\frac{g_m V_{GS} R_L}{V_{GS}} = -g_m R_L. \]  

(4.91)

The transconductance \( g_m \) is usually small, and hence, the voltage gain of a common-source FET is usually lower than the voltage gain of a CE BJT. Note that the input impedance is \( R_G \) since the internal input impedance of the FET is of the order of \( 10^{10} \Omega \), which is normally much greater than \( R_G \). \( r_d \) corresponds to the output impedance seen at the drain of the FET and is of the order of 100 k\( \Omega \). It can be found using the channel resistance equation \( r_d = \frac{r_o}{(1-V_{GS}/V_P)^2} \) from Chap. 3.

If part of the resistor \( R_S \) of the FET is un-bypassed or if capacitor \( C_3 \) is removed, then the equivalent circuit becomes that shown in Fig. 4.45. If we assume \( r_d \gg R_L \), then

\[ V_o = -g_m V_{GS} R_L \]  

(4.92)

\[ V_i = V_{GS} + g_m V_{GS} R_S. \]  

(4.93)
Fig. 4.45  Equivalent circuit of common-source amplifier with un-bypassed source resistor

Hence,

\[
\frac{V_o}{V_i} = -\frac{g_m V_{GS} R_L}{(1 + g_m R_S) V_{GS}} = -\frac{g_m R_L}{1 + g_m R_S}.
\]  

(4.94)

Thus, as in the BJT, inclusion of an un-bypassed source resistor \( R_S \) reduces the voltage gain of the common-source FET amplifier.

Example 4.12  For the circuit shown in Fig. 4.44 with \( R_L = 966 \, \Omega \), \( R_S = 468 \, \Omega \), \( R_G = 1 \, \text{M}\Omega \) and \( g_m = 5 \, \text{mA/V} \), find the voltage gain and the input impedance.

Solution  Using (4.91), the voltage gain is given by

\[ A_V = -g_m R_L = 5 \times 0.966 = -4.83. \]

The input impedance is set by resistor \( R_G = 1 \, \text{M}\Omega \).

Example 4.13  If the bypass capacitor in Example 4.12 is removed, determine the changed value of the voltage gain.

Solution  Using (4.94), the changed voltage gain is given by

\[ A_V = -\frac{g_m R_L}{1 + g_m R_S} = -\frac{5 \times 0.966}{1 + 5 \times 0.468} = -1.45. \]

4.7 Analysis of the Common-Drain JFET Amplifier

The basic circuit of a common-drain or source follower JFET amplifier is shown in Fig. 4.46. The equivalent circuit is shown in Fig. 4.47. The output voltage is given by

\[ V_{RL} \approx V_{CE} = a \]  

(4.95)
and the input voltage $V_i$ is given by

$$V_i = V_{GS} + V_o = V_{GS} + g_m V_{GS} R_S.$$  \hspace{1cm} (4.96)

Hence, the voltage gain $A_V$ becomes

$$A_V = \frac{V_o}{V_i} = \frac{g_m V_{GS} R_S}{V_{GS}}.$$  \hspace{1cm} (4.97)
If \( g_m R_S \gg 1 \), then \( A_V \approx 1 \). That is, the gain of the common-drain amplifier is approximately unity, which means that the source follows the gate.

In order to evaluate the output impedance \( Z_o \) looking in at the source, we find the ratio of the open-circuit output voltage and short-circuit current, i.e., \( Z_o = V_{oc}/I_{sc} \). The open-circuit voltage is given by

\[
V_{oc} = A_V V_i
\]

and the short-circuit current is given by

\[
I_{sc} = g_m V_{GS} = g_m V_i
\]

since, when the output is short-circuited, \( V_{GS} = V_i \). Hence,

\[
Z_o = \frac{V_{os}}{I_{sc}} = \frac{g_m R_S}{1 + g_m R_S} \frac{V_i}{g_m V_i} = \frac{R_S}{1 + g_m R_S}.
\]  

(4.100)

Note that the output impedance of the JFET is independent of any source resistance and dependent only on the transconductance and the value of \( R_S \). Note also that the input impedance of this circuit is very high because of the inherently high input impedance at the gate of the FET. The source follower is, therefore, analogous to the emitter follower. It possesses very high input impedance, approximately unity gain and relatively low output impedance.

**Example 4.14**  For the circuit of Fig. 4.46, \( R_1 = 2 \, \text{M} \Omega, R_2 = 1 \, \text{M} \Omega, R_S = 3 \, \text{k} \Omega \) and \( g_m = 5 \, \text{mA/V}, \) find the voltage gain, input impedance and output impedance.

**Solution**  Using (4.97), the voltage gain is given by

\[
A_V = \frac{g_m R_S}{1 + g_m R_S} = \frac{5 \times 3}{1 + 5 \times 3} = 0.94.
\]

The input impedance is
$R_1//R_2 = 1//2 \, \text{M} \Omega = 667 \, \text{k}$. From (4.100), the output impedance is given by

$$Z_o = \frac{R_S}{1+g_mR_S} = R_S//1/g_m = 3 \, \text{k}//1/5 \, \text{k} = 188 \, \Omega.$$ 

### 4.8 Analysis of the Common-Gate JFET Amplifier

The common-gate amplifier configuration and its equivalent circuit are shown in Fig. 4.48. The input signal is at the source, and the output signal is taken from the drain with the gate grounded. This circuit is generally used in high-frequency applications. It is analogous to the CB BJT amplifier. For this circuit, the output and input voltages are given by

$$V_o = -g_m V_{GS} R_L$$

(4.101)

$$V_i = -V_{GS}.$$  

(4.102)

![Common-gate amplifier](image)

Fig. 4.48 Common-gate amplifier

Therefore,

(4.103)
Thus, the voltage gain of the common-gate JFET amplifier has the same magnitude as the common-source amplifier but opposite sign; there is no signal inversion in the common-gate amplifier. The input impedance $Z_i$ at the source is given by

$$Z_i = \frac{V_i}{I_i} = \frac{-V_{GS}}{-g_mV_{GS}} = \frac{1}{g_m}. \quad (4.104)$$

Actually, the resistor $R_S$ appears in parallel with $1/g_m$ giving

$$Z_i = \frac{1}{g_m} \parallel R_S. \quad (4.105)$$

**Example 4.15**  For the circuit shown in Fig. 4.48 with $R_L = 966 \ \Omega$, $R_S = 468 \ \Omega$ and $g_m = 5 \ \text{mA/V}$, find the voltage gain and the input impedance.

**Solution**  Using (4.103), the voltage gain is given by $A_V = g_mR_L = 5 \times 0.966 = 4.83$. From (4.105), the input impedance given by $Z_i = 1/g_m \parallel R_S = 1/5 \parallel 0.468 = 140 \ \Omega$.

### 4.9 Depletion MOSFET Common-Source Amplifier

The depletion MOSFET operates in a manner similar to the JFET. In the circuit shown in Fig. 4.49, a common-source MOSFET is considered. The circuit uses no gate–source bias, and therefore, the drain current is equal to $I_{DSS}$. This is allowable since the gate voltage can be both positive and negative for this kind of MOSFET. The equivalent circuit is similar to that for the JFET and is also shown in Fig. 4.49.
The voltage gain is easily shown to be

\[ A_V = \frac{V_o}{V_i} = -g_m r_d / R_L \approx -g_m R_L, r_d \gg R_L. \] (4.106)

If an un-bypassed bias resistor \( R_S \) is included in the source circuit, then the voltage gain becomes

\[ A_V = \frac{g_m r_d / R_L}{1 + g_m R_S}. \] (4.107)

**Example 4.16** For the circuit shown in Fig. 4.49 with \( R_L = 5 \, \text{k} \), \( R_G = 10 \, \text{M} \Omega \) and \( g_m = 5 \, \text{mA/V} \), find the voltage gain and the input impedance.

**Solution** Using (4.106), the voltage gain is given by

\[ A_V = -g_m R_L = 5 \times 5 = -25. \] The input impedance is set by resistor \( R_G = 10 \, \text{M} \Omega \).
This device may be operated in the same manner as a JFET, as shown in Fig. 4.50. Here, \( R_S \) is included in order to reduce the drain current to a value less than \( I_{DSS} \). Because of the bypass capacitor \( C_3 \), the equivalent circuit is the same as that in Fig. 4.49, and therefore, the expressions for voltage gain and input impedance are also the same.

\[ V_{DD} \]
\[ R_D \]
\[ R_G \]
\[ R_S \]
\[ C_1 \]
\[ C_2 \]
\[ C_3 \]
\[ V_i \]
\[ V_D \]

*Fig. 4.50* Depletion MOSFET common-source amplifier with bias resistor

### 4.10 Depletion MOSFET Common-Drain Amplifier

Because of the similarity between the equivalent circuits of the JFET and the depletion MOSFET, the equivalent circuit for the depletion...
MOSFET common-drain configuration shown in Fig. 4.51 follows exactly that for the JFET in Fig. 4.46 and is given in Fig. 4.52. For this circuit,

\[
I_O = h_f I_i + h_v V_o
\]

\[
V_i = V_{GS} + V_o = V_{GS} (1 + g_m R_S).
\] (4.109)
Therefore, the voltage gain is given by

\[
A_V = \frac{V_o}{V_i} = \frac{g_mV_{GS}R_S}{1 + g_mR_S} = \frac{g_mR_S}{1 + g_mR_S}
\]  

(4.110)

which goes to unity if \(g_mR_S \gg 1\). Output impedance \(Z_o\) is given by

\[
Z_o = \frac{R_S}{1 + g_mR_S}.
\]  

(4.111)

Input impedance \(Z_i\) is given by

\[
Z_i = R_G.
\]  

(4.112)

4.11 Depletion MOSFET Common-Gate Amplifier

Again, since the equivalent circuit of the JFET is similar to that for the depletion MOSFET, the equivalent circuit for the depletion MOSFET common-gate configuration is exactly that for the JFET in Fig. 4.48. The MOSFET common-gate amplifier and its equivalent circuit are shown in Fig. 4.53. The voltage gain is given by

\[
A_V = \frac{V_o}{V_i} = g_mR_L
\]  

(4.113)
and the input impedance is given by

\[ Z_i = \frac{1}{g_m} // R_s. \]  

(4.114)

### 4.12 Enhancement MOSFET Common-Source Amplifier

The enhancement MOSFET can also be used in amplifier design. Since the conduction channel has to be created, the device requires a biasing network to overcome the threshold voltage and turn the device on. The circuit of a common-source amplifier using an enhancement MOSFET is shown in Fig. 4.54. The voltage divider arrangement is used. The equivalent circuit for this arrangement is shown in Fig. 4.55.
The analysis of this configuration is straightforward and follows that given for the other FET circuits. The value of $g_m$ is obtained using (3.17) for the drain current given by $I_D = k(V_{GS} - V_T)^2$. Since $g_m$ is
defined by \( g_m = \frac{\Delta I_D}{\Delta V_{GS}} \), its value can be derived by differentiating \( I_D \) with respect to \( V_{GS} \):

\[
g_m = \frac{dI_D}{dV_{GS}} = \frac{d}{dV_{GS}} k(V_{GS} - V_T)^2 = 2k(V_{GS} - V_T). \tag{4.115}
\]

This reduces to

\[
g_m = 2k(V_{GS} - V_T). \tag{4.116}
\]

The value of \( k \) must be determined for a specific operating point using the device specification sheet.

Another biasing arrangement that can be used to bias the enhancement MOSFET is the drain–gate feedback bias shown in Fig. 4.56. The equivalent circuit for this configuration is shown in Fig. 4.57. In order to determine the voltage gain of the circuit, we write the node equation for the drain terminal as

\[
I_i = g_m V_{GS} + \frac{V_o}{r_{d//R_D}}. \tag{4.117}
\]
Fig. 4.56 Common-source amplifier using drain–gate feedback bias

Fig. 4.57 Equivalent circuit of circuit in Fig. 4.56

Also, $V_{GS} = V_i$ and $I_i = \frac{V_i - V_o}{R_G}$. Hence,
\[
\frac{V_i - V_o}{R_G} = g_m V_i + \frac{V_o}{r_d/\|R_D}\]

which yields

\[
V_o \left( \frac{1}{r_d/\|R_D} + \frac{1}{R_G} \right) = V_i \left( \frac{1}{R_G} - g_m \right)
\]

from which the voltage gain \(A_V\) is given by

\[
A_V = \frac{V_o}{V_i} = \frac{1}{\frac{R_G}{V_i} - \frac{g_m}{V_i}} = \frac{1}{\frac{R_G}{\|R_D} + 1} \approx -g_m R_G/\|r_d/\|R_D, g_m \gg \frac{1}{R_G}
\]

In order to find the input impedance to this circuit, we use

\[
I_i = \frac{V_i - V_o}{R_G}
\]

Substituting (4.121) into (4.117) gives

\[
I_i = g_m V_i + \frac{V_i}{r_d/\|R_D} - I_i \frac{R_G}{r_d/\|R_D}
\]

\[
I_i \left( 1 + \frac{R_G}{r_d/\|R_D} \right) = V_i \left( g_m + \frac{1}{r_d/\|R_D} \right).
\]

Therefore, the input impedance \(Z_i = V_i/I_i\) is given by

\[
Z_i = \frac{V_i}{I_i} = \frac{R_G + r_d/\|R_D}{1 + g_m r_d/\|R_D}.
\]

**Example 4.17** The MOSFET shown in Fig. 4.58 has \(k = 0.31 \times 10^{-3} \text{ A/V}^2, V_T = 3.5\text{V} \) and \(V_{GSQ} = 10\text{ V}.\) Determine the voltage gain and input impedance of the circuit.
Solution From (4.116), the transconductance $g_m$ is given by $g_m = 2k(V_{GS} - V_T) = 2 \times 0.31 \times 10^{-3}(10 - 3.5) = 4.03$ mA/V. From (4.120), the expression for the voltage gain of the common-source amplifier in Fig. 4.58 is given by $A_V \approx -g_mR_D, R_D \ll R_G, r_d$. Therefore, $A_V = -4.03 \times 10 \, \text{k} = -40.3$. From (4.124), the input impedance is $Z_i = \frac{R_G+R_D}{1+g_mR_D}, r_d \gg R_D$. This gives $Z_i = \frac{220 \, \text{k}+10 \, \text{k}}{1+40.3} = 5.6 \, \text{k}$. 

*Fig. 4.58 Circuit for Example 4.17*
4.13 Enhancement MOSFET Common-Drain Amplifier

The circuit for an enhancement MOSFET common-drain amplifier is shown in Fig. 4.59, while the equivalent circuit is shown in Fig. 4.60. Apart from the need to exceed the threshold voltage in order to turn on the MOSFET, the arrangement is similar to the common-drain circuit using the depletion MOSFET and, therefore, has similar characteristics.

Fig. 4.59 Common-drain amplifier using enhancement MOSFET
For this circuit,

\[ I_O = h_f I_i + h_o V_o \]

(4.125)

\[ V_i = V_{GS} + V_o = V_{GS} (1 + g_m R_S) \]  

(4.126)

Therefore, the voltage gain is therefore given by

\[ A_V = \frac{V_o}{V_i} = \frac{g_m V_{GS} R_S}{(1 + g_m R_S) V_{GS}} = \frac{g_m R_S}{1 + g_m R_S} \]

(4.127)

which goes to unity if \( g_m R_S \gg 1 \). Output impedance \( Z_o \) is given by

\[ Z_o = \frac{R_S}{1 + g_m R_S} \]

(4.128)

Input impedance \( Z_i \) is given by

\[ Z_i = R_G. \]

(4.129)

### 4.14 Enhancement MOSFET Common-Gate Amplifier

The equivalent circuit for the enhancement MOSFET common-gate amplifier shown in Fig. 4.61(a) is presented in Fig. 4.61(b). This is the same equivalent circuit for the depletion MOSFET common-gate amplifier. The analysis is, therefore, the same.
The voltage gain is given by
\[ A_V = \frac{V_o}{V_i} = g_m R_L \] (4.130)
and the input impedance is given by
\[ Z_i = \frac{1}{g_m} \parallel R_S. \] (4.131)

### 4.15 Applications
Several simple applications involving use of the transistor models are presented in this section.

#### 4.15.1 Linear AC Voltmeter
A simple AC voltmeter can be designed using a BJT in a configuration employing negative feedback, as shown in Fig. 4.62. The circuit consists of a CE amplifier with collector–base feedback biasing. The output of the circuit taken at the transistor collector drives a rectifier bridge
through a coupling capacitor $C_2$ with a moving coil meter connected to the bridge. This ensures that unidirectional current flows through the meter. The output from the bridge is applied at the base of the transistor. This constitutes a feedback loop that helps to overcome the nonlinearity caused by the diode bridge and thereby linearize the meter operation, particularly at low values of input voltage. In order to make the system portable, the power supply is a 9V battery. A collector current of 0.3 mA is used in order to reduce the drain on the battery. For maximum symmetrical swing, $V_{R_1} = 9/2 = 4.5$ V. Hence,

$$R_1 = 4.5 \text{ V/0.3 mA} = 15 \text{ k}.$$  

The associated base current is 0.3/100 = 3 μA, and therefore, $R_2 = (4.5 - 0.7)/3 \mu A = 1.3 \text{ M}$. The input resistor $R_m$ sets the sensitivity of the circuit. The relationship between $V_i$ and the meter current $I_m$ can be found using the equivalent circuit for the system shown in Fig. 4.63. After manipulation, the input resistor $R_m$ is given by

$$R_m = 0.9 \frac{V_{fsd}}{I_{fsd}}$$

where $V_{fsd}$ is the maximum input voltage and $I_{fsd}$ is the maximum value of meter current. Thus, for a maximum voltage of 1 V and a 100-μA microammeter, $R_m$ is given by $R_m = 0.9 \frac{1}{100} \frac{\text{V}}{\mu \text{A}} = 9 \text{ k}$.

The coupling capacitors are chosen to be large.
**Fig. 4.62** Linear AC voltmeter

![Linear AC voltmeter diagram](image)

**Fig. 4.63** Equivalent circuit of Fig. 4.62

*Ideas for Exploration:* Determine a set of values for $R_m$ corresponding to voltage ranges from 1 to 1000 V.

### 4.15.2 Audio Mixer

The circuit of Fig. 4.64 is an audio system that mixes the signals from several sources. The transistor is in the CE configuration and biased using collector–base feedback via $R_3$. There is a resistor $R_2$ that is connected in series with capacitor $C_2$ that places $R_2$ in parallel with $R_3$ for signals only. Using a supply voltage of 15 V and 0.5 mA collector current, the collector resistor $R_4$ is $R_4 = 7.5 \text{ V}/0.5 \text{ mA} = 15 \text{ k}$. Resistor $R_3 = (7.5 - 0.7)/5 \mu\text{A} = 1.5 \text{ M}$. With $R_{1a} = R_{1b} = R_{1c} = 100 \text{ k}$ and $R_2 = 100 \text{ k}$, the equivalent circuit is shown in Fig. 4.65 and yields an output voltage given by $V_o = V_{i1} + V_{i2} + V_{i3}$. 
Ideas for Exploration: (i) Increase the number of inputs to five and derive the relationship between the inputs and the output; (ii) research the related topic of inter-channel crosstalk.

4.15.3 Bootstrapped Source Follower Using a JFET
The circuit of a bootstrapped common-drain or source follower using a JFET is shown in Fig. 4.66. It comprises the voltage divider common-drain circuit of Fig. 4.46 with (i) the introduction of resistor $R_B$ between the transistor gate and the junction of $R_1$ and $R_2$ and (ii) the introduction of capacitor $C_B$ between the transistor source and the junction of $R_1$, $R_2$ and $R_B$. Using the simplified model of the FET, the equivalent circuit representing the bootstrapped circuit is shown in Fig. 4.67. Let the current flowing into the parallel combination of resistors $R' = R_1 || R_2 || R_S$ be $I_x$. Then, from KVL, we have

$$V_i = V_{GS} + I_x R'$$

(4.132)

with

$$V_{GS} = I_i R_B$$

(4.133)

and from KCL, we have

$$I_x = I_i + g_m V_{GS}.$$
Substituting for $I_x$ and $V_{GS}$ into (4.132) and finding the input impedance $Z_i = V_i/I_i$ yields

$$Z_i = V_i/I_i = R_B + (1 + g_m R_B) R'.$$

(4.135)

### 4.15.4 Bootstrapped Source Follower Using a MOSFET

The circuit shown in Fig. 4.68 is a bootstrapped version of the source follower using an enhancement MOSFET from Fig. 4.59. It is similar to the circuit using the JFET and has the same equivalent circuit. The input impedance is therefore.
This research project is the design of a transistor gain tester that enables the current gain of binary junction transistors to be measured. The basic circuit for npn transistors is shown in Fig. 4.69. Using a 9V battery, when switch $S_1$ is closed, resistor $R_1 = 820 \text{k}$ passes a current of $(9 - 0.7)/820 \text{k} = 10 \mu\text{A}$ into the base of the transistor under test. This causes a collector current $I_C = 10 \mu\text{A} \times \beta$, which is measured in milliamperes by the milliammeter. Hence, the current gain $\beta$ is given by $\beta = I_C \text{mA} \times 10^{-3}/10 \mu\text{A} \times 10^{-6} = 100I_C$, where $I_C$ is the actual reading on the milliammeter in milliamperes. Therefore, the current gain of the transistor being tested is obtained by multiplying the reading on the

![Fig. 4.68 Enhancement MOSFET Source Follower](image)

$$Z_i = R_B + (1 + g_m R_B) R'.$$  \hspace{1cm} (4.136)

### 4.15.5 Research Project 1

This research project is the design of a transistor gain tester that enables the current gain of binary junction transistors to be measured. The basic circuit for npn transistors is shown in Fig. 4.69. Using a 9V battery, when switch $S_1$ is closed, resistor $R_1 = 820 \text{k}$ passes a current of $(9 - 0.7)/820 \text{k} = 10 \mu\text{A}$ into the base of the transistor under test. This causes a collector current $I_C = 10 \mu\text{A} \times \beta$, which is measured in milliamperes by the milliammeter. Hence, the current gain $\beta$ is given by $\beta = I_C \text{mA} \times 10^{-3}/10 \mu\text{A} \times 10^{-6} = 100I_C$, where $I_C$ is the actual reading on the milliammeter in milliamperes. Therefore, the current gain of the transistor being tested is obtained by multiplying the reading on the
milliammeter by 100. Resistor $R_3 = 120 \, \Omega$ and diode $D_1$ protect the meter in the event that a shorted transistor is introduced. $R_2 = 330 \, \Omega$ limits the battery current under such a condition.

![Transistor gain tester diagram](image)

Fig. 4.69 Transistor gain tester

*Ideas for Exploration:* (i) Introduce a switch that changes the battery polarity to enable the testing of pnp transistors. (ii) Design a 9V Zener-regulated mains-powered supply to replace the battery in order to prevent inaccuracies arising from a falling battery voltage.

### 4.15.6 Research Project 2

This second research project is the design of an instrument for the determination of $I_{DSS}$ and $V_P$ for JFETs. The basic circuit for testing n-channel JFETs is shown in Fig. 4.70 and comprises the JFET under test with its gate and source connected such that a variable gate–source voltage can be applied via potentiometer $VR_1 = 100 \, k$. In testing, potentiometer $VR_1$ is adjusted so that the gate–source voltage to the FET is zero and the current in the milliammeter measured. Providing
the drain–source voltage exceeds pinch-off, this drain current with zero
gate–source voltage corresponds to $I_{DSS}$. The potentiometer is then
adjusted to apply a negative gate–source voltage to the FET such that an
almost zero current flows through the device as indicated on the
milliammeter. A voltmeter across the gate–source terminals then
measures the gate–source voltage that pinches off the channel, which is
the pinch-off voltage $V_p$.

![JFET tester](image)

**Fig. 4.70** JFET tester

*Ideas for Exploration*: (i) Introduce a switch that changes the battery
polarity to enable the testing of p-channel JFETs. (ii) Explain why this
circuit is very tolerant of a changing supply voltage. (iii) Explore the
development of a circuit using similar ideas for the testing of depletion
MOSFETs.

**Problems**

1. Draw the $h$-parameter equivalent circuit for the CE amplifier
   shown in Fig. 4.71, and determine the voltage gain and input
2. Draw the $h$-parameter equivalent circuit of a CE H-biased amplifier circuit, and derive the expression for the voltage gain, input impedance and output impedance.

3. Draw the equivalent circuit for the amplifier shown in Fig. 4.72 and determine the voltage gain. If a load resistor of 5 k is connected at the output, what will be the new voltage gain?

4. For the circuit in question 3, determine the voltage gain if a 1 k resistor is connected in series with the input.

5. Draw the equivalent circuit for the partially decoupled CE amplifier shown in Fig. 4.73, and determine the voltage gain and the input impedance.

6. Using the partially bypassed configuration in Fig. 4.73 of question 5, design a CE amplifier having a gain of 40, using a 2N3904 npn transistor and an 18-V power supply. Determine the input impedance.

7. Show that bootstrapping can increase the input impedance of a CE amplifier in the partially bypassed configuration. Use this technique to increase the input impedance of the design in question 6.

8. Using the configuration in Fig. 4.74, design a CE amplifier having a gain of 25, using an npn transistor and a 12-V power supply.

9. The CE amplifier in Fig. 4.75 is biased for maximum symmetrical swing. Determine the voltage gain for the circuit and the current gain of the transistor.

10. Using a supply voltage of 16 V, design a collector–base feedback biased CE circuit with fixed gain of 12 using an emitter resistor and a transistor with $h_{fe} = 150$. 
11. For the CC amplifier shown in Fig. 4.76, determine the voltage gain, input impedance and output impedance.
12. Improve the input impedance of the CC amplifier in question 11 using bootstrapping.
13. For the CB amplifier shown in Fig. 4.77, determine the voltage gain, input impedance and output impedance.

For the circuit shown in Fig. 4.78, draw the equivalent circuit. For $R_L = 2 \, \text{k} \Omega$, $R_S = 1 \, \text{k} \Omega$, $R_G = 2 \, \text{M} \Omega$ and $g_m = 8 \, \text{mA/V}$, calculate the voltage gain and input impedance of the circuit.

15. If the bypass capacitor is removed from the circuit, determine the new value of the voltage gain.
16. Draw the equivalent circuit of the common-drain JFET amplifier in Fig. 4.79 and derive its voltage gain.
17. For the circuit of Fig. 4.79, $R_1 = 1.8 \, \text{M} \Omega$, $R_2 = 1.5 \, \text{M} \Omega$, $R_S = 2.2 \, \text{k} \Omega$ and $g_m = 4 \, \text{mA/V}$, find the voltage gain, input impedance and output impedance.
18. For the common-gate amplifier shown in Fig. 4.80, if $R_L = 3.2 \, \text{k} \Omega$, $R_S = 2.5 \, \text{k} \Omega$ and $g_m = 5 \, \text{mA/V}$, find the voltage gain and the input impedance.
19. The common-source depletion-mode MOSFET in Fig. 4.81 has $R_L = 10 \, \text{k} \Omega$, $R_G = 10 \, \text{M} \Omega$ and $g_m = 9 \, \text{mA/V}$. Draw the equivalent circuit and determine the voltage gain.
20. Draw the equivalent circuit for the circuit in Fig. 4.81 with a bias resistor inserted in the source circuit.
21. Draw the equivalent circuit of the depletion MOSFET common-drain amplifier.
22. Draw the equivalent circuit and derive the voltage gain and input impedance of the depletion MOSFET common-gate amplifier.

23. Draw the equivalent circuit for the enhancement mode MOSFET common-source amplifier shown in Fig. 4.82. Hence, derive the expression for the voltage gain.

24. Using the equation for the drain current, derive an expression for $g_m$.

25. Draw the equivalent circuit for the enhancement MOSFET common-drain amplifier and derive the voltage gain.

26. Draw the equivalent circuit for the common-gate enhancement MOSFET amplifier and determine the voltage gain and input impedance.

27. If the gate of an n-channel JFET is connected to the source, the gate–source voltage will be held at zero, and therefore, if the drain–source voltage exceeds the pinch-off voltage, the drain current will be constant at $I_{DSS}$. Explain how this arrangement can be used as a constant current source.

28. Is this arrangement possible with a p-channel JFET and if so how?

29. Discuss the use of an n-channel enhancement mode MOSFET in the source follower mode in place of an emitter follower BJT in enhancing a Zener diode regulator.

30. Is this arrangement possible with a p-channel enhancement mode MOSFET and if so how?
Fig. 4.71  Circuit for Question 1
Fig. 4.72  Circuit for Question 3
Fig. 4.73 Circuit for Question 5
Fig. 4.74  Circuit for Question 8
Fig. 4.75 Circuit for Question 9
**Fig. 4.76** Circuit for Question 11

**Fig. 4.77** Circuit for Question 13
Fig. 4.78  Circuit for Question 14
Fig. 4.79 Circuit for Question 16
Fig. 4.80  Circuit for Question 18
Fig. 4.81  Circuit for Question 19
Fig. 4.82 Circuit for Question 23

Bibliography


In this chapter, several transistor circuit configurations are considered. These circuits generally involve more than one transistor and can be implemented in a wide range of applications as well as perform some special functions. In this chapter, the design and application of many of these circuits will be discussed. After completing the chapter, the reader will be able to:

- Explain the operation of cascaded amplifiers, in particular two common emitter amplifiers, and determine overall voltage gain and other characteristics.
- Design several multitransistor amplifier circuits using BJTs and FETs.
- Explain the operation of and utilize a range of special transistor circuits in practical applications.
- Design simple electronic switches using BJTs and FETs.
- Utilize the JFET as a voltage-controlled resistor.

5.1 Cascaded Amplifiers
The single transistor amplifier has been considered in Chaps. 2–4. The BJT single transistor amplifier produces a higher voltage gain than its FET counterpart, because of the higher transconductance of the BJT as compared with the FET. In either case, if a higher voltage gain is required than is achievable using a single device, then a cascade connection of two single-stage amplifiers can be used.

Consider the block diagram of a cascade amplifier shown in Fig. 5.1. Here the output of amplifier $A_1$ feeds directly into the input of amplifier $A_2$. The overall gain $G$ of the cascaded system is

$$G = \frac{V_o}{V_i} = \frac{V_o}{V_i} \times \frac{V_1}{V_i} = G_1 \times G_2$$

(5.1)

where $G_1$ is the gain of amplifier $A_1$ and $G_2$ is the gain of amplifier $A_2$. Equation (5.1) indicates that the gain $G$ of the cascaded amplifier is the product of the gains of the individual amplifiers. This holds true for any number of amplifiers. However, Eq. (5.1) assumes no interaction between the cascaded amplifiers, that is, the gain amplifier $A_1$ is unaffected by amplifier $A_2$ and vice versa. This assumption holds true for operational amplifiers since the output impedance of these devices is quite low. However, it does not necessarily hold for voltage amplifiers based on discrete BJTs where the output impedance may be higher. In multistage amplifiers using BJTs, there is considerable interaction between these stages. In particular, the input impedance of the succeeding stage changes the effective value of the load of the preceding stage thereby changing its gain.

![Fig. 5.1 Cascaded amplifiers](image)

Consider the two-stage amplifier in Fig. 5.2 comprising two cascaded common emitter amplifiers. Here, capacitor $C_2$ couples the output of the first amplifier built around transistor $Tr_1$ to the input of the second amplifier built around transistor $Tr_2$. Because this capacitor and other resistors are involved, this type of coupling is referred to as RC coupling.
The voltage gain $G_1$ of the first stage for a signal going from the base to the emitter of $Tr_1$ is given by

$$G_1 = -g_{m1}\overline{R_{L1}}$$  (5.2)

where $\overline{R_{L1}}$ is the effective load of $Tr_1$. Because of the presence of $Tr_2$, this load is made up of $R_{L1}$ along with the load presented by the input to $Tr_2$ which involves $R_3$, $R_4$, and $h_{ie2}$ associated with $Tr_2$. [It will be shown shortly that $\overline{R_{L1}} = R_{L1}\parallel R_3\parallel R_4\parallel h_{ie2}$.] Thus, the voltage gain of $Tr_1$ is reduced because of the loading effect resulting from the input to $Tr_2$. However, the gain $G_2$ of $Tr_2$ is given by

$$G_2 = -g_{m2}R_{L2}$$  (5.3)

and the overall gain $G$ is given by

$$G = G_1 \times G_2 = g_{m1}g_{m2}\overline{R_{L1}}R_{L2}$$  (5.4)

This gain can be as large as 1000 and higher. Thus, despite the loading effect of $Tr_2$, the cascading of two BJT amplifier stages can produce high gains.
Example 5.1  Draw the equivalent circuit of the two-stage amplifier in Fig. 5.3. Determine the voltage gain $V_o/V_i$ and, hence, the current gain $I_o/I_i$. Assume $h_{fe} = 100$ for both transistors.
Solution  The equivalent circuit is shown in Fig. 5.4. The voltage gain is given by \( \frac{V_o}{V_i} = A_{V1} \times A_{V2} \) where \( A_{V1} \) is the voltage gain of \( Tr_1 \) and \( A_{V2} \) is the voltage gain of \( Tr_2 \). In order to proceed, the values of \( h_{ie1} \) for \( Tr_1 \) and \( h_{ie2} \) for \( Tr_2 \) must be determined. Let \( V_{B1} \) and \( V_{B2} \) be the DC voltages at the bases of the two transistors. Then, because of the voltage divider, \( V_{E1} = 4 \) and \( I_{C1} = 4/4 = 1 \) mA. Thus, \( h_{ie1} = \frac{100}{40 \times 1} = 2.5 \) k. Similarly, \( V_{B2} = \frac{37}{163 + 37} \times 20 = 3.7 \) V giving \( V_{E2} = 3 \), \( I_{C2} = 3/6 = 0.5 \) mA and \( h_{ie2} = \frac{100}{40 \times 0.5} = 5 \) k. The load \( R_{L1} \) of \( Tr_1 \) is \( R_{L1} = 8 \) k/\( 37 \) k/\( 163 \) k/\( h_{ie2} = 8 \) k/\( 37 \) k/\( 163 \) k/\( 5 \) k = 2.8 k. Hence, the gain \( A_{V1} \) of \( Tr_1 \) is \( A_{V1} = -40I_{C1}R_{L1} = -40 \times 1 \times 2.8 = -112 \). The load \( R_{L2} \) of the second transistor is \( R_{L2} = 10 \) k/\( 8 \) k = 4.4 k. Therefore, the voltage gain \( A_{V2} \) of \( Tr_2 \) is given by \( A_{V2} = 40I_{C2}R_{L2} = -40 \times 0.5 \times 4.4 = -88 \).
Hence, the overall voltage gain $A_V$ is $A_V = A_{V1} \times A_{V2} = -112 \times -88 = 9856$. In order to determine the current gain $I_o/I_i$, we note that $rac{V_o}{V_i} = \frac{I_oR_i}{I_iZ_i}$

where $R_L$ is the 8 k resistor into which $I_o$ flows and $Z_i$ is the input impedance at the base of $Tr_1$. $Z_i$ at the base of $Tr_1$ is $Z_i = 47 k/153 k//h_{ie1} = 47 k/153 k//2.5 k = 2.3 k$. Rearranging gives $rac{I_o}{I_i} = \frac{V_o}{V_i} \times \frac{Z_i}{R_L} = 9856 \times \frac{2.3 k}{8 k} = 2834$.

![Fig. 5.4 Equivalent circuit of two-stage amplifier](image)

**Example 5.2** Draw the equivalent circuit of the two-stage amplifier in Fig. 5.5. Determine the voltage gain $V_o/V_s$ and, hence, the current gain $I_o/I_s$. Assume $h_{fe} = 120$ for both transistors.
Fig. 5.5 Two-stage common emitter amplifier

Solution  The equivalent circuit is shown in Fig. 5.6. The voltage gain is given by $\frac{V_o}{V_s} = \rho \times A_{V1} \times A_{V2}$, where $\rho$ is the factor by which the input signal is attenuated before it arrives at the base of $Tr_1$, $A_{V1}$ is the voltage gain of $Tr_1$, and $A_{V2}$ is the voltage gain of $Tr_2$. In order to proceed, the values of $h_{ie1}$ and $h_{ie2}$ must be determined. Let $V_{B1}$ and $V_{B2}$ be the DC voltages at the bases of the two transistors. Then, because of the voltage divider, $V_{B1} = \frac{37}{300} \times 30 = 3.7$ V. Hence, $V_{E1} = 3$ and $I_{C1} = 3/6 = 0.5$ mA.

Thus, $h_{ie2} = \frac{100}{40 \times 0.5} = 5$ k. Similarly, $V_{B2} = \frac{23.5}{150} \times 30 = 4.7$ V giving $V_{E2} = 4$, $I_{C2} = 4/(3.6 + 0.4) = 1$ mA and $h_{ie2} = \frac{120}{40 \times 1} = 3$ k. The load $R_{L1}$ of $Tr_1$ is $R_{L1} = 6$ k//23.5 k//126.5 k//($h_{ie2} + h_{je2}$ 400) = 6 k//23.5 k//126.5 k//($3$ k + $120 \times 400$) = 4.2 k. Hence, the gain $A_{V1}$ of $Tr_1$ is $A_{V1} = -40 I_{C1} R_{L1} = -40 \times 0.5 \times 4.2 = -84$. The load $R_{L2}$ of the second
transistor is \( R_{L2} = 12 \, k\Omega / 12 \, k = 6 \, k \). Therefore, the voltage gain \( A_{V2} \) of \( Tr_2 \) is given by 
\[
A_{V2} = \frac{-R_{L2}}{400 + h_{ie2} / h_{fe2}} = \frac{6 \, k}{400 + 3 \, k / 120} = -14.1.
\]
The input impedance \( Z_i \) at the base of \( Tr_1 \) is \( Z_i = 37 \, k\Omega / 263 \, k\Omega / h_{ie1} = 5 \, k \). Hence, the attenuation factor \( \rho \) is given by 
\[
\rho = \frac{Z_i}{2.5 \, k + Z_i} = \frac{5 \, k}{7.5 \, k} = 0.67.
\]
Therefore, the overall voltage gain \( A_V \) is 
\[
A_V = -\rho \times A_{V1} \times A_{V2} = 0.67 \times 84 \times 14.1 = 794.
\]
In order to determine the current gain \( I_0 / I_S \), we note that 
\[
\frac{V_O}{V_S} = \frac{I_0 R_L}{I_S (R_S + Z_i)}
\]
where \( R_L \) is the 12 k resistor into which \( I_0 \) flows and \( R_S \) is the 2.5k series resistor at the input to \( Tr_1 \). Rearranging this gives 
\[
\frac{I_0}{I_S} = \frac{V_O}{V_S} \times \frac{R_S + Z_i}{R_L} = 794 \times \frac{(2.5 \, k + 5 \, k)}{12 \, k} = 496.
\]

**Fig. 5.6** Equivalent circuit of two-stage common emitter amplifier

Another interesting two-transistor circuit involves the use of a common collector amplifier to reduce the loading on the output of a common emitter amplifier. The circuit is shown in Fig. 5.7. Here, the common emitter amplifier \( Tr_1 \) is followed by a common collector amplifier \( Tr_2 \). A feature of this circuit is the use of the collector of \( Tr_1 \) to bias transistor \( Tr_2 \) by direct connection, thereby eliminating the need for biasing components and capacitive coupling between the two transistors. Such an arrangement is referred to as **direct coupling** and, when used throughout an amplifier, confers the advantage of enabling the amplifier to respond down to DC. Since the input impedance

\[ Z_{i2} = [h_{ie2} + (1 + h_{fe2})R_5] \] to \( Tr_2 \) is high, the load on \( Tr_1 \) is small so that the effective collector resistance for \( Tr_1 \) is \( R_3/Z_{i2} \approx R_3 \). Hence, the gain of the first stage is preserved at \( G_1 = -g_{m1}R_3 \). Since the second stage is an emitter follower, the gain of this stage is approximately unity and therefore the overall gain \( G \) is \( G = -g_{m}R_3 \). This circuit has the additional advantage of low output impedance because of the common collector output amplifier. Its value \( Z_o \) is given by

\[
Z_o = \frac{h_{ie2} + R_3}{1 + h_{fe}} // R_5
\]

(5.5)

**Fig. 5.7** Common emitter amplifier with emitter follower output

**Example 5.3** Using the two-stage design in Fig. 5.7, design a two-stage amplifier having the ability to drive low-impedance loads.

**Solution** The design of the first stage follows the steps for the standard common emitter stage. For a 20-V supply, the design approach of section (Sect. 2.4 in Chap. 2) yields \( R_1 = 174 \, k \), \( R_2 = 26 \, k \), \( R_3 = 9 \, k \), and
$R_4 = 2\ \text{k}$. For this circuit, the collector voltage of $Tr_1$ is 11 V. This is, therefore, the base voltage of $Tr_2$ resulting in an emitter voltage for $Tr_2$ of 10.3 V. Therefore, if we choose a current of 10 mA for $Tr_2$ in order to ensure a large current drive capability, then $R_5 = 10.3/10\ \text{mA} = 1\ \text{k}$.

**Example 5.4**  Modify the design in Example 5.3 in order to set the voltage gain at 50.

**Solution**  In order to lower the voltage gain to 50, an un-bypassed resistor $R_6$ is introduced in the emitter of $Tr_1$ as shown in Fig. 5.8. The voltage gain now becomes $A_V = \frac{R_3}{R_6 + r_e}$ where $r_e = 1/40I_C = 1/40 = 25\ \Omega$.

Hence, $50 = \frac{9\ \text{k}}{R_6 + 25}$ giving $R_6 = 155\ \Omega$.

![Common emitter amplifier with reduced gain](image)

An emitter follower can also be used to preserve the gain of a single FET amplifier while providing a reduced output impedance. Such a circuit is
shown in Fig. 5.9. The FET $Tr_1$ is a common source amplifier with a high input impedance, the exact value for which is established by bias resistor $R_1$.

\[ \text{Fig. 5.9 Common source JFET amplifier with emitter follower output} \]

**Example 5.5**  Design a two-stage amplifier using the topology of Fig. 5.9.

**Solution**  The design of the JFET stage follows the steps used in the design of the common source JFET amplifier in Chap. 3. The values obtained for a 18V supply and a 1 mA quiescent current are $R_1 = 1 \, M$, $R_2 = 2 \, k$, and $R_3 = 8 \, k$. The DC voltage at the drain of $Tr_1$ is 10 V. Therefore, the base of the BJT is 10 V giving 9.3 at the emitter. Choosing a collector current of 5 mA for large current drive capability, $R_4 = 9.3/5 \, mA = 2 \, k$.

The circuit of Fig. 5.10 utilizes a common base amplifier in the first stage and a common collector amplifier in the second stage. This circuit produces the same voltage gain as that in Fig. 5.7 using a common
emitter amplifier in the first stage but does not produce signal inversion. Also, its input impedance is significantly lower than that of Fig. 5.7.

**Fig. 5.10** Two-stage amplifier design

**Example 5.6** Using the circuit configuration in Fig. 5.10, design a two-stage amplifier using an 18V supply.

**Solution** The design follows exactly the design of the circuit of Fig. 5.7 except that capacitor $C_1$ is grounded and the input signal is applied through an ungrounded capacitor $C_2$. In other words, the design of Fig. 5.7 can be converted to that in Fig. 5.10 by simply adjusting capacitors $C_1$ and $C_2$ as done previously.

The configuration in Fig. 5.11 involves the collector-base feedback biasing common emitter amplifier with an emitter follower output that prevents loading on the amplifying stage. The voltage at the collector of $Tr_1$ is usually $V_{cc}/2$ for maximum symmetrical swing and hence the determination of $R_3$ easily follows as $R_3$ equals $(V_{cc}/2 - 0.7)$ divided by the quiescent collector current of $Tr_2$. 

![Two-stage amplifier design](image-url)
5.1.1 Direct Coupled High-Gain Configurations

All of the direct coupled configurations discussed thus far give gains in the range of 100–300. Even though the configurations comprise two transistors, this gain is provided by a single common emitter stage. In order to achieve higher gains as discussed previously, at least two stages must provide gain. The circuit shown in Fig. 5.12 comprises two common emitter amplifiers that have direct coupling between them with the collector of the first stage $Tr_1$ being connected to the base of the second stage $Tr_2$. Resistor $R_3$ provides bias stability in $Tr_2$ while resistor $R_4$ provides bias to $Tr_1$ in a manner that is essentially collector-base feedback bias for this stage. However, by connecting resistor $R_4$ at the emitter of $Tr_2$ instead of the collector of $Tr_1$, transistor $Tr_2$ is also included in the bias-stabilizing feedback loop. As a result, bias stability for the two transistors is achieved since any quiescent current change in either transistor is corrected by the loop. Note that for signals, capacitor $C_3$ grounds the emitter of $Tr_2$ thereby disconnecting the feedback loop.

The equivalent circuit is shown in Fig. 5.13. The voltage gain of the first stage is $A_{V1} = -40I_{C1}R_1 || h_{ie2}$, while the gain of the second stage is
\[ I_x = I_i + g_m V_{GS} \]. Hence, the overall gain is the product of these two gains, and this can be quite high.

![Direct coupled high-gain amplifier](image1)

**Fig. 5.12** Direct coupled high-gain amplifier

![Equivalent circuit of direct coupled high-gain amplifier](image2)

**Fig. 5.13** Equivalent circuit of direct coupled high-gain amplifier

**Example 5.7** Using the configuration in Fig. 5.12, design a direct coupled amplifier with high gain.

**Solution** Using a 20-V supply, since the two stages have voltage gain, it follows that the voltage swings at the collector of \( Tr_2 \) are greater than those at the collector of \( Tr_1 \). Therefore, maximum symmetrical swing
consideration are more important for \( Tr_2 \) than \( Tr_1 \). Applying the design techniques of Chap. 2 for a common emitter amplifier, let the emitter voltage of \( Tr_2 \) be \( V_{CC}/10 = 20/10 = 2 \) V. Choosing 2 mA quiescent current for this stage, then \( R_3 = 2 \) V/2 mA = 1 k. For maximum symmetrical swing, the voltage drop across \( R_2 \) is \( (20 - 2)/2 = 9 \) V. Hence, \( R_2 = 9 \) V/2 mA = 4.5 k. The voltage at the base of \( Tr_2 \) is the same voltage at the collector of \( Tr_1 \), which is 2.7 V. Choosing a quiescent current in \( Tr_1 \) of 1 mA, then \( R_1 = (20 - 2.7)/1 \) mA = 17.3 k. Finally, \( R_4 \) is calculated from \( (2 - 0.7)/R_4 = 1 \) mA/100 where the current gain of \( Tr_1 \) is taken as 100. This gives \( R_4 = 130 \) k. The gain for this circuit is about 6000.

### 5.1.1.1 Bootstrapping

A method of achieving high gain in a single common emitter stage is to increase the value of the load resistance. This can be accomplished for signals by the *bootstrapping* method used in Chap. 4 to increase amplifier input impedance. The method is shown in Fig. 5.14. Here, the resistor \( R_1 \) is the load resistor in an amplifier stage with a signal \( V_i \) driving this resistor and an amplifier \( A \) whose gain \( \rho \) is less than unity such as an emitter or source follower. The resistor is split into two resistors \( R_{1a} \) and \( R_{1b} \) with the output of the amplifier \( A \) driving the junction of the two resistors. For this arrangement, the current \( I_R \) flowing into resistor \( R_{1a} \) is

\[
I_R = \frac{(V_i - V_o)}{R_{1a}} \tag{5.6}
\]

where \( V_o = \rho V_i \).
Hence, the effective resistance seen by the input signal $V_i$ is

$$R'_{1a} = \frac{V_i}{I_R} = R_{1a}/(1 - \rho) \tag{5.7}$$

Since $\rho < 1$, it follows that $R'_{1} > R_{1a}$. For example, for $\rho = 0.95$, then

$$R'_{1} = \frac{R_{1a}}{1 - 0.95} = 20R_{1a}.$$  

Therefore, for $R_{1a} = 2$ k say, then

$$R'_{1} = 20 \times 2 \text{ k} = 40 \text{ k}.$$  

Thus, the effective resistance of $R_{1}$ as seen by the signal can be made quite large by this method.

The application of this technique to a common emitter amplifier is shown in Fig. 5.15. This configuration consists of a common emitter driving a common collector. The collector resistor $R_{1}$ of the first stage is split into $R_{1a}$ and $R_{1b}$, and capacitor $C_{3}$ connects the emitter of $Tr_{2}$ to the junction of the two resistors. Its reactance at the lowest frequency of interest must be less than $R_{1a}/(R_{1b} + h_{fe2}R_{2})$. Since the other end of resistor $R_{1b}$ is connected to the base of $Tr_{2}$, this resistor is therefore bootstrapped. The effect is that an increased value of collector resistance is presented to $Tr_{1}$, resulting in a high gain for this stage. This gain is preserved by $Tr_{2}$, which has a high input impedance since it is configured as an emitter follower. The voltage gain is about 2000.
Example 5.8  Using the configuration in Fig. 5.15, design a direct coupled amplifier with high gain.

Solution  Let $V_{CC} = 20$ V. Since only the first stage has gain, then maximum symmetrical swing is applied to this stage. Using a collector current of 1 mA in $Tr_1$, then for maximum symmetrical swing, $R_1 = 10$ V/1 mA = 10 k. Splitting this into two resistors then, $R_{1a} = R_{1b} = 5$ k. The emitter voltage of $Tr_2$ is $10 - 0.7 = 9.3$ V. Using a current of 2 mA in $Tr_2$, then $R_2 = 9.3/2 = 4.7$ k. For $R_3$, $(9.3 - 0.7)/R_3 = 1$ mA/100 giving $R_3 = 860$ k. In evaluating the gain of the circuit, we first note that $R_{1a}$ is in parallel with $R_2$ and part of the emitter load of $Tr_2$. Hence, the effective resistance seen by $Tr_2$ emitter is $4.7k//5k = 2.4$ k. Therefore, the voltage gain of $Tr_2$ is $g_mR_E/(1 + g_mR_E) = 40 \times 2 \times 2.4/(1 + 40 \times 2 \times 2.4) = 0.995$. Therefore,
This very high resistance is presented to the transistor collector. Unfortunately, it is not the only resistance seen by $Tr_1$ collector; there are two others. The first of these is the input impedance of the emitter follower $Tr_2$, which is $h_{fe} \times 2.4 \text{ k} = 240 \text{ k}$. The second is the output impedance $1/h_{oe}$ of $Tr_1$, which we have generally omitted because it is large compared with other resistors. However, this is no longer the case here. From the specifications for the 2N3904, this value is of the order of 100 k. Hence, the effective collector load of $Tr_1$ is $1M/240k/100k = 66k$. Therefore, the voltage gain of $Tr_1$ is $40 \times 1 \times 66 = 2640$.

This bootstrapping arrangement can also be used to increase the gain of a JFET common source amplifier as shown in Fig. 5.16a. This configuration is similar to Fig. 5.15, except that the JFET with fixed biasing replaces the BJT in the first stage.

**Fig. 5.16** Increasing the gain of a JFET amplifier with bootstrapping

**Exercise 5.1** Analyze the design shown in Fig. 5.16b involving a JFET having $V_p = -3 \text{ V}$ and $I_{DSS} = 3 \text{ mA}$. 
5.2 Darlington Pair

An important two-transistor circuit is the Darlington pair shown in Fig. 5.17. It consists of two BJTs in which the two collectors are connected while the emitter of the first feeds the base of the second. The arrangement acts as a single transistor with base B (the base of the first transistor), collector C (the two connected collectors), and emitter E (the emitter of the second transistor). This unit has an enhanced current gain that is approximately the product of the current gain of the individual transistors. In order to see this, consider the Darlington pair in Fig. 5.17. For this,

\[ I_{E1} = I_{C1} + I_{B1} \]
\[ I_{C1} = \beta_1 I_{B1} \] (5.8)

\[ I_{E1} = I_{C1} + I_{B1} \]
\[ I_{C1} = \beta_1 I_{B1} \] (5.9)

![Darlington pair diagram](image)

**Fig. 5.17** Darlington pair

But \( I_{B2} = I_{E1} \) and \( I_{C} = I_{C1} + I_{C2} \). Therefore,

\[ (5.10) \]
Thus, for the Darlington pair,

\[ I_C = \beta_D I_B \]  \hspace{1cm} (5.12)

where \( \beta_D = \beta_1 \beta_2 \) and \( I_E = (1 + \beta_D) I_B \). Therefore, the Darlington pair functions as though it is a single transistor with very high current gain \( \beta_D \). It is possible to obtain two BJTs forming a Darlington pair in a single package. The MPSA29 is an example of such a device. This transistor has a typical current gain of 10,000.

In order to determine the voltage gain and the input impedance of the Darlington Pair in the common emitter configuration, consider the equivalent circuit of the arrangement as shown in Fig. 5.18. The input voltage is given by

\[ V_i = I_{b1} h_{ie1} + I_{b2} h_{ie2} \]  \hspace{1cm} (5.13)
Fig. 5.18 Darlington pair in a common emitter amplifier

From the equivalent circuit,

\[ I_{b2} = (1 + h_{fe1}) I_{b1} \]  \hspace{1cm} (5.14)

and therefore (5.13) becomes

\[ V_i = I_{b1} \left( h_{ie1} + (1 + h_{fe1}) h_{ie2} \right) \]  \hspace{1cm} (5.15)

Hence, the input impedance is given by

\[ Z_i = V_i / I_{b1} = h_{ie1} + (1 + h_{fe1}) h_{ie2} \]  \hspace{1cm} (5.16)

Therefore, the input impedance of the Darlington pair is enhanced by a factor of the current gain of the first transistor as compared to a single device. The output voltage is given by

\[ V_o = - \left( h_{fe1} I_{b1} + h_{fe2} I_{b2} \right) R_L = - \left[ h_{fe1} + h_{fe2} \left( 1 + h_{fe1} \right) \right] I_{b1} R_L \]  \hspace{1cm} (5.17)

Therefore, the voltage gain is given by

\[ A_V = V_o / V_i = - \frac{(h_{fe1} + h_{fe2} \left( 1 + h_{fe1} \right)) R_L}{h_{ie1} + (1 + h_{fe1}) h_{ie2}} \]  \hspace{1cm} (5.18)

For \( h_{fe1} h_{ie2} \gg h_{ie1} \), this reduces to

\[ \text{(5.19)} \]
Thus, the voltage gain of the Darlington pair is similar to that of a single transistor. In the presence of an un-bypassed emitter resistor $R_e$, Eq. (5.15) for the input voltage becomes

$$V_i = I_{b1} \left[ h_{i e1} + \left( 1 + h_{f e1} \right) h_{i e2} + \left( 1 + h_{f e1} \right) \left( 1 + h_{f e2} \right) R_e \right]$$

From this, the input impedance is given by

$$Z_i = V_i/I_{b1} = h_{i e1} + \left( 1 + h_{f e1} \right) h_{i e2} + \left( 1 + h_{f e1} \right) \left( 1 + h_{f e2} \right) R_e \approx h_{f e1} h_{f e2} R_e \quad (5.21)$$

and the voltage gain is given by

$$A_V = V_o/V_i = \frac{-\left( h_{f e1} + h_{f e2} \left( 1 + h_{f e1} \right) \right) R_L}{h_{i e1} + \left( 1 + h_{f e1} \right) h_{i e2} + \left( 1 + h_{f e1} \right) \left( 1 + h_{f e2} \right) R_e} \quad (5.22)$$

This reduces to

$$A_V \approx \frac{-R_L}{R_e}, h_{f e2} R_e \gg h_{i e2} \quad (5.23)$$

**Example 5.9** Design a common emitter amplifier using a Darlington package having $\beta_D = 1000$ and a 24V supply Calculate the voltage gain of your circuit.

**Solution** For the circuit in Fig. 5.19, choose $I_{Cq} = 1$ mA for good $\beta_D$ and frequency response. Using rule-of-thumb (2.41), $V_{b e} = 24/10 = 2.4$ V. Hence, $R_e = 2.4/1$ mA = 2.4 k, and for maximum symmetrical swing,

$$R_L = \frac{24-2.4}{1 \text{ mA} \times 2} = 10.8 \text{ k}\Omega.$$  

$V_{b q} = V_{b e} + 2V_{b e} = 3.8$ V and

$$I_R = 10I_{b q} = 10 \times 1 \text{ mA} / 1000 = 0.01 \text{ mA}. \text{ Therefore, } R_2 = \frac{3.8 \text{ V}}{0.01 \text{ mA}} = 380 \text{ k}\Omega$$

and $R_1 = \frac{24-3.8}{0.01 \text{ mA}} = 2.02 \text{ M}\Omega$. The resulting voltage gain is

$$A_V = -40I_C R_L = -40 \times 1 \text{ mA} \times 10.8 \text{ k} = -432.$$  

To complete the design,
large coupling capacitors, say 47 μF, are used at the input and output. Note that the resistors $R_1$ and $R_2$ are effectively in parallel with the input signal. Thus, while their values must be sufficiently low to ensure that $I_R \geq 10I_B$ for bias stability, they normally cannot be too low since they will load down the input signal. However, because of the Darlington pairs, it is possible to use $I_R = 50I_{Bq} = 50 \times 1 \text{ mA} / 1000 = 0.05 \text{ mA}$. Then, $R_2 = \frac{3.8 \text{ V}}{0.05 \text{ mA}} = 76 \text{ kΩ}$ and $R_2 = \frac{3.8 \text{ V}}{0.01 \text{ mA}} = 380 \text{ kΩ}$. These values of resistors are still reasonably high.

![Circuit for Example 5.10](image)

**Fig. 5.19** Circuit for Example 5.10

**Example 5.10** For the circuit in Fig. 5.19 of Example 5.9, determine the gain if the bypass capacitor $C_3$ is removed.

**Solution** From (5.23), the voltage gain if $C_3$ is removed is

$$A_V \approx -\frac{R_f}{R_E} = -\frac{10.8 \text{ kΩ}}{2.4k} = -4.5.$$

**Example 5.11** Modify the circuit in Example 5.10 to achieve a gain of 20.
Solution Using (5.23), the voltage gain of 20 is achieved by including an un-bypassed resistor $R_e$ such that $A_V \approx \frac{R_e}{R_e} = \frac{10.8 \, \text{k}}{R_e} = 20$ giving $R_e = 540 \, \Omega$. In order to accommodate this resistor in series with $R_E$, this resistor is reduced to $R_E = 2.4 \, \text{k} - 0.54 \, \text{k} = 1.9 \, \text{k}$.

5.2.1 Darlington Pair in Common Collector Configuration

We wish now to determine the voltage gain and the input impedance of the Darlington pair in the *common collector* configuration. Consider the equivalent circuit of the arrangement as shown in Fig. 5.20.

![Darlington pair in common collector configuration](image)

*Fig. 5.20* Darlington pair in common collector configuration

From the equivalent circuit, the input voltage is given by

$$V_i = I_{b1}h_{ie1} + I_{b2}h_{ie2} + (1 + h_{fe})I_{b2}R_E$$

But

$$I_{b2} = (1 + h_{fe})I_{b1}$$

Hence,

$$V_i = I_{b1}h_{ie1} + (1 + h_{fe})I_{b2}R_E$$

(5.24)

(5.25)

(5.26)
The output voltage is given by
\[ V_o = (1 + h_{fe2}) I_{b2} R_E = (1 + h_{fe1})(1 + h_{fe2}) I_{b1} R_E \] (5.27)

Hence, the voltage gain is given by
\[ A_V = \frac{V_o}{V_i} = \frac{(1 + h_{fe1})(1 + h_{fe2}) I_{b1} R_E}{[h_{ie1} + (1 + h_{fe1}) h_{ie2} + (1 + h_{fe1})(1 + h_{fe2})] I_{b1}} \] (5.28)

This reduces to
\[ A_V = \frac{V_o}{V_i} = \frac{(1 + h_{fe1})(1 + h_{fe2}) R_E}{[h_{ie1} + (1 + h_{fe1}) h_{ie2} + (1 + h_{fe1})(1 + h_{fe2})] R_E} \] (5.29)

which can be about 0.99. This gain is slightly higher than that of a single-transistor emitter follower, which is \((1 + h_{fe}) R_E / (h_{ie} + (1 + h_{fe}) R_E)\). The input impedance is given by
\[ Z_i = V_i / I_{b1} = h_{ie1} + (1 + h_{fe1}) h_{ie2} + (1 + h_{fe1})(1 + h_{fe2}) R_E \approx h_{fe1} h_{fe2} R_E \] (5.30)

which is quite high.

**Example 5.12**  Design a common collector amplifier using a Darlington package having \(\beta_D = 1000\) and a 24V supply. Calculate the input impedance of your circuit.

**Solution**  For the circuit in Fig. 5.21, choose \(I_{CQ} = 5\) mA in order to supply an external load. For maximum symmetrical swing, \(V_{RE} = 24/2 = 12\) V. Hence, \(R_E = 12/5\) mA = 2.4 k. \(V_{BQ} = V_{RE} + 2V_{BE} = 13.4\) V and \(I_R = 10I_{BQ} = 10 \times 5\) mA/1000 = 0.05 mA. Therefore,
\[ R_2 = \frac{3.8\ V}{0.01\ mA} = 380\ k \text{ and } R_2 = \frac{3.8\ V}{0.01\ mA} = 380\ k. \]

To complete the design, large coupling capacitors, say 47 µF, are used at the input and output. The input impedance is
\[ R_1//R_2//1000R_E = 268\ k//212\ k//1000 \times 2.4\ k = 113\ k. \]
Example 5.13  Apply bootstrapping to the input of the circuit of Example 5.12 and estimate the final input impedance.

Solution  The bootstrapped case is shown in Fig. 5.22. The voltage gain of the Darlington pair is about 0.99. Hence, a value of $R_B$ of 100 k will present an impedance to the input signal of $R_B/(1 - 0.99) = 10$ M. This value is in parallel with the input impedance seen at the transistor base, which is about $\beta_D R_E = 5000 \times 2.4$ k = 12 M. The input impedance is therefore $10$ M//12 M = 5.5 M.
5.3 Feedback Pair

The feedback pair or compound Darlington is a two-transistor configuration that behaves in a manner similar to the Darlington pair. It comprises an npn transistor and a pnp transistor—the emitter of the npn connected to the collector of the pnp and the collector output of the npn connected to the base of the pnp. The arrangement shown in Fig. 5.23 functions effectively as an npn transistor. The PNP version is also shown in Fig. 5.23.
Consider the circuit shown in Fig. 5.23.

\[
I_{E1} = I_{C1} + I_{B1} \\
I_{C1} = \beta_1 I_{B1} \\
\]

\[
I_{E1} = I_{C1} + I_{B1} \\
I_{C1} = \beta_1 I_{B1} \\
\]

But \( I_{C1} = I_{B2} \) and \( I_E = I_{E1} + I_{C2} \). Hence,

\[
I_C = I_{E2} \\
= (1 + \beta_2) I_{B2} \\
= (1 + \beta_2) \beta_1 I_{B1} \\
\approx \beta_1 \beta_2 I_{B1} \\
\]

Also,

\[
I_E = \beta_2 I_{B2} + (1 + \beta_1) I_{B1} \\
= \beta_1 \beta_2 I_{B1} + (1 + \beta_1) I_{B1} \\
= (1 + \beta_1 \beta_2) I_{B1} \\
\]

Thus, for the feedback pair,

\[
(5.31) \quad (5.32) \quad (5.33) \quad (5.34) \quad (5.35)
\]
\[ I_C = \beta_F I_B \]

where \( \beta_F = \beta_1 \beta_2 \) and \( I_E = (1 + \beta_F)I_B \).

The voltage gain and input impedance of the feedback pair in the common emitter configuration are now determined. Consider the equivalent circuit of the arrangement as shown in Fig. 5.24. The input voltage is given by

\[ V_i = I_{b1} h_{ie1} \]  

(5.36)

Hence, the input impedance is given by

\[ Z_i = \frac{V_i}{I_{b1}} = h_{ie1} \]  

(5.37)

This is the same as the single transistor. The output voltage is given by

\[ V_o = \left(1 + h_{fe2}\right)I_{b2}R_L \]  

(5.38)

From the equivalent circuit,

\[ I_{b2} = -h_{fe1} I_{b1} \]  

(5.39)

and therefore (5.38) becomes
Therefore, the voltage gain is given by

\[ A_V = \frac{V_o}{V_i} = \frac{-h_{fe1} (1 + h_{fe2}) R_L}{h_{ie1}} = -h_{fe2}g_m R_L \]  

(5.41)

This result indicates that the voltage gain of the feedback pair in the common emitter configuration is that of the first transistor \((-g_m R_L)\), multiplied by the current gain of the second transistor. This suggests gains of the order of 20,000! In practice, however, the output resistance \(1/h_{oe1}\) of the first transistor, which was omitted from the analysis, limits the achievable gain. In order to evaluate the effect of this parameter, we re-introduce it into the equivalent circuit for \(Tr_1\). The effect is that all of the collector current of \(Tr_1\) does not flow into the base of \(Tr_2\); some of this current is lost through \(1/h_{oe1}\). Using the current divider theorem, Eq. (5.39) becomes

\[ I_{b2} = -h_{fe1} I_{b1} \frac{1}{1/h_{oe1} + [h_{ie2} + (1 + h_{fe2}) R_L]} \]  

(5.42)

where the term in square brackets in the denominator is the input impedance at the base of \(Tr_2\). Using the modified Eq. (5.33) for \(I_{b2}\), the expression for the voltage gain becomes

\[ A_V = -h_{fe2}g_m R_L \frac{1}{1/h_{oe1} + [h_{ie2} + (1 + h_{fe2}) R_L]} \]  

(5.43)

For \(h_{fe2} \gg 1\), this reduces to

\[ A_V = -h_{fe2}g_m R_L \frac{1}{1 + h_{oe1} (h_{ie2} + h_{fe2} R_L)} \]  

(5.44)

If \(h_{fe2} R_L \gg h_{ie2}\), then (5.44) further reduces to

\[ A_V = -h_{fe2}g_m R_L \frac{1}{1 + h_{oe1} (h_{ie2} + h_{fe2} R_L)} = \frac{h_{fe2}g_m R_L}{1 + h_{oe1} h_{fe2} R_L} \approx -g_m R_L \]  

(5.45)
Since $1/h_{oe1}$ is usually larger than $R_L$, the gain of the feedback pair in the common emitter configuration is higher than the gain of the Darlington pair (or a single transistor) in the same configuration. This very interesting result seems rarely to appear in textbooks.

**Example 5.14** Determine the voltage gain for the feedback pair in the common emitter configuration in Fig. 5.25, where the first transistor has a current of 0.7 mA.

![Circuit for Example 5.14](image)

**Solution** The 2N3904 transistor in the first stage of the feedback pair has $h_{oe1}$ of 1 to 40 μmhos. Using $h_{oe1} = 20$ μS, then

$1/h_{oe1} = 1/20 \times 10^{-6} = 50 \text{ k}$, which is greater than the load resistance of 5 k. Therefore, the voltage gain of the circuit is given by

$A_V = -g_{m1}1/h_{oe1} = -40 \times 2 \times 50 = -4000$. 
Note that the gain of a single transistor with the same collector current 2 mA operating into the same load resistor $R_L = 5 \text{k} \Omega$ is

$$A_V = -g_{m1}R_L = -40 \times 2 \times 5 = -400,$$

which is an order of magnitude lower than 4000. In the presence of an un-bypassed emitter resistor $R_e$, Eq. (5.36) for the input voltage becomes

$$V_i = I_{b1} \left[ h_{ie1} + \left( 1 + h_{fe1} + h_{fe1}h_{fe2} \right) \right] R_e$$  \hspace{1cm} (5.46)

From this, the input impedance is given by

$$Z_i = \frac{V_i}{I_{b1}} = h_{ie1} + \left( 1 + h_{fe1} + h_{fe1}h_{fe2} \right) R_e \approx h_{fe1}h_{fe2}R_e$$  \hspace{1cm} (5.47)

Thus, both the Darlington pair and the feedback pair have high current gains $\beta_F = \beta_1\beta_2$. The feedback pair has the advantage of having only one $V_{BE}$ voltage drop between the base and emitter, while the Darlington pair has two. Also, in the common emitter configuration, the voltage gain of the feedback pair is significantly higher than that of the Darlington pair. However, the Darlington pair tends to have a better frequency response.

The configuration of the feedback pair may be used to enhance the effective transconductance of a JFET. Thus, a JFET can replace the first BJT in the circuit while retaining the second BJT as shown in Fig. 5.26. The result is that the overall gain of the circuit in a common source configuration increases from $-g_{m1}R_L$ to $-h_{fe2}g_{m1}R_L$ where $g_{m1}$ is the transconductance of the JFET. However, as occurred in the feedback pair involving two BJTs, the drain resistance of the JFET will limit the gain increase. Resistor $R_B$ is used to provide adequate bias current to the JFET.
**Example 5.15** Design a common source amplifier using a JFET-BJT feedback pair in the topology shown in Fig. 5.26. Use a 20V supply and an n-channel JFET having $V_P = -2$ V and $I_{DSS} = 6$ mA. Determine the voltage gain of the circuit.

**Solution** We follow the design procedure for a self-biased common source amplifier in Chap. 3. Using $I_{DSS} = 6$ mA, $V_P = -3$ V and $I_D = 1$ mA in Shockley’s equation gives

$$V_{GS} = \left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)V_P = \left(1 - \sqrt{\frac{1\text{ mA}}{6\text{ mA}}}\right)(-3) = (1 - 0.4)(-2) = -1.2 \text{ V}$$

Hence, $I_D R_S = 1.2$ V giving $R_S = 1.2$ V/1 mA = 1.2 k. For maximum symmetrical swing with $V_{DD} = 20$ V, we allow for the 0.7 V across $R_B$. 

---

**Fig. 5.26** Feedback pair using JFET and BJT in common source amplifier
Hence, \( R_L = \frac{(20-1.2-0.7)/2}{1 \text{ mA}} = 9 \text{ k}\). Resistor \( R_B = 0.7 \text{ V}/1 \text{ mA} = 700 \text{ \Omega} \). The input impedance of the JFET is greater than \( 10^8 \text{ \Omega} \), and, therefore, \( R_G \) is chosen to be 1 M\(\Omega\). From (3.8), \( g_m \) is given by

\[
g_m = \frac{-2I_{DSS}}{V_P} \sqrt{\frac{I_D}{I_{DSS}}} = -2 \frac{\sqrt{I_D/I_{DSS}}}{V_P} = -2 \frac{\sqrt{1 \text{ mA} \times 6 \text{ mA}}}{2} = -2 \times \frac{2.45}{2} = 2.45 \text{ mA/V}
\]

. Hence, the voltage gain \( A_V \) is given by \( A_v \approx -g_m R_D = -2.45 \times 50 \text{ k} = -122.5 \).

### 5.3.1 Feedback Pair in Emitter Follower Configuration

We now determine the voltage gain and the input impedance of the feedback pair in the *common collector* configuration. Consider the equivalent circuit of the arrangement as shown in Fig. 5.27.

![Feedback pair in common collector configuration](image)

Fig. 5.27 Feedback pair in common collector configuration

From the equivalent circuit, the input voltage is given by

\[
V_i = I_{b1} h_{ie1} + \left[ (1 + h_{fe1}) I_{b1} - h_{fe2} I_{b2} \right] R_E
\]  \hspace{1cm} (5.48)

But

\[
R_E
\]  \hspace{1cm} (5.49)
The output voltage is given by
\[ V_i = I_{b1} \left[ h_{ie1} + \left( 1 + h_{fe1} + h_{fe1}h_{fe2} \right) R_E \right] \] (5.50)

Hence, the voltage gain is given by
\[ A_V = \frac{V_o}{V_i} = \frac{1 + h_{fe1} + h_{fe1}h_{fe2}}{h_{ie1} + \left( 1 + h_{fe1} + h_{fe1}h_{fe2} \right) R_E} \] (5.51)

which is almost exactly unity: a near-perfect emitter follower! The input impedance is given by
\[ Z_i = V_i/I_{b1} = h_{ie1} + \left( 1 + h_{fe1} + h_{fe1}h_{fe2} \right) R_E \approx h_{fe1}h_{fe2}R_E \] (5.53)

which also is quite high and can become as high as 10 M or higher with bootstrapping.

The feedback pair may be adjusted to provide gain in a manner that is different from the common emitter configuration discussed so far. This is done by the introduction of resistors as shown in Fig. 5.28. It is sometimes called the series feedback pair because it involves the application of a kind of negative feedback referred to as voltage-series feedback. It comprises an npn transistor \( Tr_1 \) operating in the common emitter mode with the emitter resistor un-bypassed. The output of \( Tr_1 \) is coupled to another common emitter transistor \( Tr_2 \) this employing a pnp transistor.
The unique arrangement in this circuit is the connection of the collector resistor $R_5$ to the emitter of transistor $Tr_1$ rather than to ground. The gain can be found by considering the equivalent circuit shown in Fig. 5.29. Here, the bias components $R_1$, $R_2$, and $R_3$ have been omitted for simplicity. From this,

$$V_o = -h_{fe2} I_{b2} R_5 + \left[ \left(1 + h_{fe1} \right) I_{b1} - h_{fe2} I_{b2} \right] R_4$$

(5.54)
Noting that $I_{b2} = -h_{fe1} I_{b1}$, (5.39) reduces to

$$V_o = h_{fe1} h_{fe2} I_{b1} R_5 + \left[ (1 + h_{fe1}) I_{b1} + h_{fe1} h_{fe2} I_{b1} \right] R_4$$  \hspace{1cm} (5.55)

At the input,

$$V_i = I_{b1} h_{ie1} + \left[ (1 + h_{fe1}) I_{b1} + h_{fe1} h_{fe2} I_{b1} \right] R_4$$  \hspace{1cm} (5.56)

Therefore, the voltage gain $A_V = V_o/V_i$ is given by

$$A_V = \frac{h_{fe1} h_{fe2} R_5 + \left( 1 + h_{fe1} + h_{fe1} h_{fe2} R_4 \right)}{h_{ie1} + \left( 1 + h_{fe1} + h_{fe1} h_{fe2} \right) R_4}$$  \hspace{1cm} (5.57)

Since $h_{fe1} h_{fe2} \gg 1 + h_{fe1}$ and assuming $h_{fe1} h_{fe2} R_4 \gg h_{ie1}$, then (5.57) reduces to

$$A_V = 1 + R_5/R_4$$  \hspace{1cm} (5.58)

A practical implementation of this basic circuit is shown in Fig. 5.30. Resistors $R_1$, $R_2$, and $R_4$ provide voltage-divider bias to $Tr_1$ while resistor
$R_3$ provides bias current for $Tr_1$ as the base current of $Tr_2$ is generally not sufficient.

![Practical feedback pair with gain](image)

**Fig. 5.30** Practical feedback pair with gain

**Example 5.16** Design a feedback pair using Fig. 5.30 to provide a fixed gain of 5 using a 20V supply.

**Solution** Let the collector current of each transistor be 1 mA. Then, $R_3 = 0.7\ V/1\ mA = 700\ \Omega$. For bias stability of $Tr_1$, let the emitter voltage be $V_{CC}/10 = 20/10 = 2\ V$. Then, noting that the collector currents of both transistors flow into $R_4$, the value of this resistor is $R_4 = 2\ V/2\ mA = 1\ k$. For maximum symmetrical swing, the voltage at the collector of $Tr_2$, which is the output must be $2 + (20 - 2)/2 = 11$. From this, $R_5 = 9\ V/1\ mA = 9k$. This gives a gain of $A_V = 1 + R_5/R_4 = 10$. In order to achieve a gain of 5, a 5k portion of $R_5 = 9k$ can be bypassed with a large capacitor leaving 4k in the signal path. This results in $A_V = 1 + R_5/R_4 = 1 + 4 k/1 k = 5$. Also, using $I = 1\ mA/10 = 0.1\ mA$ in resistors $R_1$ and $R_2$ for bias stability gives $R_1 = 173\ k$ and $R_2 = 27\ k$. 
The signal gain of this basic circuit may be changed by connecting series-connected resistor and capacitor in parallel with either $R_4$ for increased gain or $R_5$ for decreased gain as shown in Fig. 5.31. The feedback pair utilizing a JFET for the first transistor can also produce gain by the introduction of resistors $R_4$ and $R_5$ as shown in Fig. 5.32. The effective gain is $A_V = 1 + R_5/R_4$.

![Feedback pair with variable gain](image)
**Fig. 5.32** BJT-JFET feedback pair with variable gain

**Example 5.17** Determine the gain of the JFET-BJT feedback arrangement in Fig. 5.33.
Solution Using $A_V = 1 + R_S/R_A$, the gain of this amplifier is $A_V = 1 + 10^4/100 = 101$.

5.4 Current Sources
A current source is a current supply that maintains its current value, regardless of the load. This implies infinite output impedance. However, a practical current source has a finite output resistance $R$ as shown in Fig. 5.34. The value of $R$ is generally high: $R \rightarrow \infty$ corresponds to an ideal current source. While the terminals of a voltage source should in general not be short-circuited lest an infinite current flows, the terminals AB of the current source should in general not be open-circuited lest an infinite voltage develops across its terminals. Current sources are widely
used in electronic circuits design and are particularly important in integrated circuit design. They can be realized using BJT$s$ and FETS.

![Practical current source](image)

**Fig. 5.34** Practical current source

### 5.4.1 BJT Current Source 1

A constant current source using a BJT is shown in Fig. 5.35. It consists of a transistor $Tr_1$ with a resistor $R_E$ connecting the emitter to ground and its base fixed at a potential $V_{BB}$ by a suitable voltage source as shown in Fig. 5.35a. It follows therefore that

$$V_{RE} = (V_{BB} - V_{BE}) = I_E R_E$$  \hspace{1cm} (5.59)

where $I_E$ is the emitter current in the transistor. Therefore,
The voltage \( V_{BB} \) can be supplied by a Zener diode as shown in Fig. 5.35b. Here, \( V_{BB} = V_Z \) and \( R_Z \) is chosen such that the Zener diode is properly reverse-biased.

**Example 5.18** Calculate the constant current \( I_C \) in the circuit of Fig. 5.35b for \( V_Z = 6.2 \), \( R_Z = 1 \) k and \( R_E = 5.5 \) k, and determine the current through the Zener diode.

**Solution** The voltage \( V_{RE} \) across \( R_E \) is given by \( V_{RE} = 6.2 - 0.7 = 5.5 \) V. Hence, \( I_C = 5.5 \text{ V/}5.5 \text{ k} = 1 \) mA. The current \( I_Z \) in the Zener is given by
\[ I_Z = \frac{(15 - 6.2)}{1 \text{k}} = 8.8 \text{ mA}. \]

### 5.4.2 BJT Current Source 2

Another BJT constant current source utilizes two BJTs. The configuration is shown in Fig. 5.36. The base emitter function of \( Tr_2 \) maintains a voltage of 0.7 V across the resistor \( R_1 \) thereby yielding a current

\[ I_R = \frac{0.7}{R_1} \quad (5.61) \]

![Diagram of two-transistor current source](image)

**Fig. 5.36** Two-transistor current source

Ignoring the base currents of the two transistors, the current \( I_{R1} \) is equal to the emitter current of \( Tr_1 \) and hence

\[ (5.62) \]
\[ I_1 = I_{R_1} = 0.7/R_1 \]

\( R_2 \) supplies current to the base of \( Tr_1 \) and the collect of \( Tr_2 \).

**Example 5.19** Using the configuration in Fig. 5.36, design a constant current source that produces a current of 1 mA from a 12-V supply.

**Solution** For a current of 1 mA, \( R_1 = 0.7 \text{ V}/1 \text{ mA} = 700 \Omega \). For proper operation of \( Tr_2 \), choose \( I_2 = 1 \text{ mA} \). Then, \( R_2 = (12 - 1.4)/1 = 10.6 \text{ k}\Omega \). Resistor \( R \) represents the load through which the constant current flows.

### 5.4.3 BJT Current Source 3

A third BJT constant current source shown in Fig. 5.37 can be described as a true two terminal arrangement as its two terminals are floating.

![Four-transistor current source](image)

*Fig. 5.37* Four-transistor current source

It is an arrangement of two of the two-transistor current sources in Fig. 5.36 but of opposite polarities; one two-transistor current source is built around transistors \( Tr_1 \) and \( Tr_2 \) while the other is made up of
transistors $Tr_3$ and $Tr_4$. Thus, a current $I_{R1}$ through resistor $R_1$ is given by $I_{sc} = -h_feI_b$. This current flows in through terminal 1, through $Tr_3$ and $Tr_1$ and out through terminal 2. Similarly, a current $I_{R1}$ through resistor $R_2$ is given by $I_{sc} = -h_feI_b$. This current flows in through terminal 1, through $Tr_4$ and $Tr_2$ and out through terminal 2. Hence, the total current $I_T$ through the arrangement is the sum of these two currents and is given by

$$I_T = V_{be} \left( \frac{1}{R_1} + \frac{1}{R_2} \right)$$

If $R_1 = R_2 = R$, this reduces to

$$I_T = V_{be} \left( \frac{1}{R_1} + \frac{1}{R_2} \right) = 2V_{be}/R$$

Discrete complementary transistors such as the 2N3904 and 2N3906 or the MPQ6502 silicon quad complimentary package containing 2 npn and 2 pnp transistors can be used to implement this circuit configuration.

**Example 5.20** Using the circuit in Fig. 5.37, design a two-terminal constant current source to deliver a constant current of 2 mA.

**Solution** From Eq. (5.64), $I_T = 2$ mA = 2(0.7)/$R$. This gives $R = R_1 = R_2 = 700 \, \Omega$.

**5.4.4 JFET Current Source 1**

The JFET functions as an extremely effective constant source when operated above pinch-off. Thus, in an n-channel JFET for $V_{GS} = 0$, for example, and $V_{DS} > V_P$, the drain current is constant at $I_{DSS}$. This constant current value is that achieved in the circuit shown in Fig. 5.38a. Here, $V_{GS} = 0$ and $I_D = I_{DSS}$ for $V_{DS} > V_P$. Note that this arrangement constitutes a two-terminal device. If the gate-source voltage is made negative, then the saturation drain current is reduced, and hence, a new constant current results. This arrangement is shown in Fig. 5.38b, where the resistor $R_S$ included in the source circuit produces $V_{GS} = -I_D R_S$. Hence, a
variable constant current two-terminal source can be achieved by making \( R_S \) variable. The exact value of \( I_D \) corresponding to a particular value of \( R_S \) can be found using Shockley’s equation, which is given by

\[
I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2
\]  

\( (5.65) \)

**Fig. 5.38** JFET constant current source

**Example 5.21** Using a JFET having \( V_P = -5 \) V and \( I_{DSS} = 8 \) mA, design a constant current source with current value 2 mA.

**Solution** Using Shockley’s equation for \( I_D = 2 \) mA, we have

\[
2 = 8 \left(1 - \frac{V_{GS}}{5}\right)^2
\]

Solving for \( V_{GS} \) gives \( V_{GS} = -2.5 \) V. Since \( I_D R_S = 2.5 \), then

\[ R_S = 1.25 \text{k} \]

The JFET connected as a constant current source is available commercially and is referred to as a constant current diode or current-regulating diode. It can operate for voltages ranging from 2 to 300 V.
When operated with reverse polarity, the constant current diode conducts as a junction diode, and therefore two such devices can be connected in series (one with normal polarity and the other with reverse polarity) to regulate alternating current. Siliconix manufactures two-terminal FET constant current diodes in plastic packages with currents ranging from 0.24 mA (J500) to about 4.7 mA (J511) and in metal TO-18 packages with currents ranging from 1.6 mA (CR160) to 4.7 mA (CR470). Central semiconductor offers the CCL0035-CCL5750 series with currents from 35 μA to 6 mA with peak voltage ratings of 100 V.

### 5.4.5 JFET Current Source 2

A JFET current source allowing two-directional current flow is shown in Fig. 5.39. It utilizes the basic configuration in Fig. 5.38b but with two JFETs. For current flow $I_{12}$ from terminal 1 to terminal 2, $Tr_1$ operates in the constant current mode with current flowing from drain to source of $Tr_1$ through $R_1$ while $Tr_2$ operates with a forward-biased gate-source junction through which the current flows to terminal 2. For current flow $I_{21}$ from terminal 2 to terminal 1, $Tr_2$ now operates in the constant current mode with current flowing from drain to source of $Tr_2$ through $R_2$ while $Tr_1$ operates with a forward-biased gate-source junction through which the current flows to terminal 1. Current $I_{12}$ is set by resistor $R_1$ using Shockley’s equation (5.65) as before while current $I_{21}$ is set by resistor $R_2$. These currents will be approximately equal if $R_1 = R_2$. The JFETs may be the n channel 2N3819 or matched JFETs in a dual package such as the 2N5199.
Fig. 5.39 Two-JFET constant current source

5.5 Current Mirror

The circuit shown in Fig. 5.40 is called a current mirror (based on a circuit developed by Bob Widlar) since the current established in $Tr_1$ via resistor $R_1$ is mirrored in transistor $Tr_2$ and, hence, flows through $R$ regardless of its value. The circuit can therefore function as an effective constant current source. The current through $R_1$ is given by
Transistors $Tr_1$ and $Tr_2$ have the same base-emitter voltage since their base-emitter junctions are connected in parallel. If we assume the two transistor are matched (i.e., have approximately the same characteristics), it follows that they both have the same emitter/collector currents, that is, $I = I_2$. Since $I = \beta I_B$,

$$I = I_1 - 2I_B \approx I_1$$  \hspace{1cm} (5.67)

Hence,

$$I_2 = I \approx I_1$$  \hspace{1cm} (5.68)

A better current mirror is the Wilson current mirror shown in Fig. 5.41. This is a three-transistor arrangement that is more accurate than the current mirror just considered. For this circuit,

$$I_1 = \frac{V_{cc} - V_{BE}}{R_1}$$  \hspace{1cm} (5.69)
Now, $Tr_1$ and $Tr_2$ again have the same collector currents $I_C$ and base currents $I_B$. For $Tr_3$, the emitter current is given by

$$I_{E3} = \beta I_B + 2I_B = (2 + \beta) I_B$$  \hspace{1cm} (5.70)

Hence,

$$I_{B3} = \frac{I_{E3}}{1 + \beta} = \frac{2 + \beta}{1 + \beta} I_B \approx I_B$$  \hspace{1cm} (5.71)

Therefore,

$$\quad$$  \hspace{1cm} (5.72)

*Fig. 5.41* Wilson current mirror
\[ I_1 = I_{C1} + I_B = I_C + I_B \]

Now,
\[ I_{sc} = -h_{fe}I_b. \]  \hspace{1cm} (5.73)

But,
\[ I_{E3} = I_{C2} + 2I_B \]  \hspace{1cm} (5.74)

Therefore,
\[ I_2 = I_{C2} + 2I_B - I_B = I_C + I_B \]  \hspace{1cm} (5.75)

Hence,
\[ I_1 = I_2 \]  \hspace{1cm} (5.76)

**Example 5.22**  Design a Wilson current mirror to deliver a constant current of 0.5 mA using a 24V supply.

**Solution**  Using Eq. (5.69), \( R_1 = (V_{CC} - 2V_{BE})/I_1 \). Since \( I_2 = 0.5 \) mA, then \( I_1 = 0.5 \) mA, and therefore, \( R_1 = (24 - 1.4)/0.5mA = 4.2k \).

**Example 5.23**  In Fig. 5.42, determine \( I_1, I_2, V_1, \) and \( V_2 \).
**Solution**  The current through the 19.3 k resistor in the collector of $Tr_1$ is $I(19.3 \; k) = (20 - 0.7)/19.3 \; k = 1 \; mA$. Since $Tr_1$ and $Tr_2$ form a current mirror, $I_1 = I = 1 \; mA$. Also, $Tr_3$ and $Tr_4$ form a current mirror, and therefore, the current through the 11.1 k resistor is equal to $I_1$.

Therefore, the voltage across this resistor is $V(11.1 \; k) = 1 \; mA \times 11.1 \; k = 11.1 \; V$. Hence, $V_1 = 11.1 - 0.7 = 10.4 \; V$. The current through $Tr_5$ is $I(Tr_5) = V_1/20.8 \; k = 10.4/20.8 = 0.5 \; mA$. This current develops a voltage drop across the 6 k resistor in the collector of $Tr_5$ given by $V(6 \; k) = 0.5 \; mA \times 6 \; k = 3 \; V$. As a result, the voltage at the base of $Tr_6$ is $V_B(Tr_6) = 20 - 3 = 17 \; V$ giving $V_2 = 17 - 0.7 = 16.3 \; V$.

Finally, $I_2 = 16.3 \; V/32.6 \; k = 0.5 \; mA$.

### 5.6 $V_{BE}$ Multiplier
The $V_{BE}$ multiplier is a single transistor circuit that effectively multiplies the base-emitter voltage of a transistor. It is sometimes referred to as a variable Zener. The circuit is shown in Fig. 5.43.

![Fig. 5.43 VBE multiplier](image)

Here, the base-emitter voltage of $Tr_1$ sets a fixed voltage 0.7 V across $R_2$ thereby producing a current $I_{R_2} = 0.7/R_2$. If the base current of $Tr_1$ is small compared with $I_{R_2}$, then $I_{R_1} \approx I_{R_2}$. Hence,

$$V_{R_1} = I_{R_1}R_1 = 0.7 \frac{R_1}{R_2} \quad (5.77)$$

Therefore,

$$V_Z = V_{R_1} + V_{R_2} = 0.7 + 0.7 \frac{R_1}{R_2} = 0.7 \left(1 + \frac{R_1}{R_2}\right) = \left(1 + \frac{R_1}{R_2}\right) V_{BE} \quad (5.78)$$

Thus, the $V_{BE}$ of $Tr_1$ is multiplied by a factor $(1 + R_1/R_2)$, setting a voltage $V_Z$ across the transistor. The circuit, therefore, functions as a Zener diode. Note that any increase in $I_R$ will increase the voltage across $R_2$, which, in turn, will tend to increase $V_{BE}$. This will then turn the
transistor further on thereby increasing $I_C$ and hence diverting the additional current through the transistor.

**Example 5.24** Determine values for $R_1$ and $R_2$ such that the voltage across the transistor in the $V_{BE}$ multiplier of Fig. 5.43 is 2.8 V.

**Solution** From Eq. (5.78), for $R_2 = 1 \text{k}$ then $2.8 = \left(1 + \frac{R_1}{R_2}\right)0.7$. This gives $R_1 = 3 \text{k}$.

### 5.7 Cascode Amplifier

An important amplifier circuit configuration utilizing multiple transistors is the cascode amplifier shown in Fig. 5.44. In this circuit, a common emitter amplifier $Tr_1$ drives a common base amplifier $Tr_2$. The base of $Tr_2$ is held at a potential $V_B$, which can be provided by a Zener diode or other voltage source arrangement. $Tr_1$ is shown here utilizing fixed biasing, but other biasing schemes can be used. The input impedance of $Tr_2$ is $r_{e2}$, and this is the load of $Tr_1$.

![Cascode Amplifier Diagram](image-url)
Therefore, the gain of common emitter amplifier $Tr_1$ is

$$A_{V1} = -\frac{h_{fe1}r_{e2}}{h_{ie1}} \approx \frac{r_{e2}}{r_{e1}}$$  \hspace{1cm} (5.79)$$

where

$$r_{e1} \approx \frac{h_{ie1}}{h_{fe1}}$$  \hspace{1cm} (5.80)$$

The gain of the second-stage $Tr_2$ is given by

$$A_{V2} = +\frac{h_{fe2}R_L}{h_{ie2}} \approx \frac{R_L}{r_{e2}}$$  \hspace{1cm} (5.81)$$

The overall gain $A_V$ of the circuit is, therefore,

$$A_V = A_{V1} \times A_{V2} = \frac{r_{e2}}{r_{e1}} \times \frac{R_L}{r_{e2}} = \frac{R_L}{r_{e1}} = g_{m1}R_L$$  \hspace{1cm} (5.82)$$

where $g_{m1} = 1/r_{e1}$. The input impedance of the circuit is that of $Tr_1$ in the common emitter configuration, which, in this case, is $h_{ie1}/R_B$. Because of the presence of $Tr_2$, the configuration has the transfer characteristic of a common emitter amplifier but the output characteristic (high output impedance) of a common base amplifier. Note that voltage divider biasing may be applied to $Tr_1$ and the voltage $V_B$ may be provided by a Zener or a potential divider with appropriate grounding capacitor.

One major advantage of the configuration is that since the collector of $Tr_1$ is held at an almost constant voltage, the Miller effect (multiplication of the collector-base capacitance $C_{cb}$ of $Tr_1$) is reduced (this is discussed in Chap. 7). The result is that the effect of $C_{cb}$ is minimized and results in an improved frequency response for the circuit. Another major advantage of this circuit is the reduction of early effect (modulation of the collector-base capacitance) distortion arising from the reduction of the voltage change at the collector of $Tr_1$. 
Example 5.25 Using the configuration shown in Fig. 5.45, design a cascode amplifier circuit. Use $V_{CC} = 24$ V.

![Practical cascode amplifier circuit](image)

**Solution** The practical circuit is shown in Fig. 5.45. Here, the diodes $D_1$ and $D_2$ fix the voltage at the base of $Tr_2$ at 1.4 V, and $R_D$ supplies current to the diodes. Choose this current to be about 5 mA, and then $R_D = \frac{24-1.4}{5 \text{mA}} = 4.5$ kΩ. Choose $I_{Cq}(Tr_2) = 1$ mA. The maximum peak-to-peak voltage swing for this transistor is approximately $24 - 1.4 = 22.6$ V. Therefore, for maximum symmetrical swing, $R_L = \frac{22.6}{2} / 1 \text{mA} = 11.3$ kΩ.

Using $\beta(Tr_1) = 100$, $R_B = \frac{24-0.7}{(1 \text{mA}/100)} = 2.3$ MΩ. Voltage gain for this circuit is $A_V = -40I_cR_L = -40 \times 1 \times 11.3 = -452.$
A modified cascode amplifier utilizing a BJT and an FET, which does not require a bias voltage $V_B$ is shown in Fig. 5.46. It functions essentially as a three-terminal device. It is self-biasing, provided the BJT collector current is such that the resulting FET gate-source voltage is sufficient to keep the BJT out of saturation. A third configuration utilizing two FETS in the configuration in Fig. 5.46 is possible. It is also self-biasing provided the gate-source voltage of the second FET ($Tr_2$) exceeds the pinch-off voltage of the first ($Tr_1$), thereby keeping it operating in the saturation region. All of these cascode circuits can be used to produce very high output impedance current sources.

**Fig. 5.46** Modified cascode amplifier

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## 5.8 Improved Emitter Follower

The emitter follower has a low output impedance, which enables it to drive low-impedance loads without a reduction of the output voltage. The configuration also has high current drive capability and is therefore widely used in the output stage of amplifiers. One drawback of the circuit discussed in Fig. 2.55 in Chap. 2 is its inability to deliver full
output voltage swing on both half-cycles of a sinusoidal waveform. Specifically, an emitter follower using an npn transistor can deliver an output voltage into a load $R_L$ limited only by the power supply voltage. However, on the negative half-cycle, the output voltage $V_{O^-}$ is limited to

$$V_{O^-} = I_{Cq}R_E \parallel R_L$$

(5.83)

where $I_{Cq}$ is the quiescent current in the transistor. This situation can be improved by replacing the emitter resistor $R_E$ by a constant current source as shown in Fig. 5.47. In this circuit, all of the current $I_{Cq}$ is available for sinking load current so that the peak negative output voltage increases to

$$V_{O^-} = I_{Cq}R_L$$

(5.84)

![Improved emitter follower](image)
The constant current source can be any of those discussed earlier.

Example 5.26  Design an improved emitter follower using the circuit of Fig. 5.47.

Solution  A possible configuration is shown in Fig. 5.48. The constant current source is implemented around $Tr_2$ with diodes $D_1$ and $D_2$ setting the fixed voltage across resistor $R_3$ and the transistor base-emitter junction. We choose $I_{cq} = 2$ mA so that the circuit can drive low-impedance loads. Then, $R_3 = 0.7 \, \text{V}/2 \, \text{mA} = 350 \, \Omega$. Resistor $R_2$ supplies current to the diodes, and if we allow about 5 mA, then $R_2 = (15 - 1.4)/5 \, \text{mA} = 2.7 \, \text{k}$. Finally, resistor $R_1$ supplies bias current into $Tr_1$ and a value of about 10 k ensures that the resulting offset voltage is small.
An even better arrangement is the complimentary emitter follower circuit shown in Fig. 5.49 utilizing complimentary transistors. Here, the emitter resistor or constant current source is replaced by another transistor in emitter follower configuration but having opposite polarity. On the positive half-cycle, the npn transistor as before delivers a positive-going output voltage and sources a high current, while on the negative half-cycle, the pnp transistor delivers a negative-going output voltage and sinks a high current. Proper operation requires that a bias voltage be applied between the two transistor base terminals so that the two transistors are turned on during the quiescent state. This circuit is discussed more fully in Chap. 10.

**Fig. 5.48** Circuit of improved emitter follower

**Fig. 5.49** Complimentary symmetry emitter follower

### 5.9 Differential Amplifier
One of the most important and widely used circuits is the differential amplifier or “long tail” pair shown in Fig. 5.50. It comprises two transistors of the same polarity connected at their emitters where a constant current source is connected to supply bias current to each. Each transistor is essentially in a common emitter mode with an input signal supplied to its base and an output signal taken at its collector. The system operates in the following manner: Assuming the input to $Tr_2$ is set to zero, as the input signal $V_{i1}$ to $Tr_1$ increases positively, the base-emitter voltage drop $V_{be1}$ of $Tr_1$ increases and $V_{be2}$ of $Tr_2$ decreases. The result of this is an increase in the collector current through $Tr_1$, which, because of the constant current source, causes a corresponding decrease in the collector current of $Tr_2$. Therefore, the collector voltage of $Tr_1$ goes down while that of $Tr_2$ goes up, by the same magnitude. If $V_{i1}$ increases negatively, the reverse occurs resulting in a decrease in the collector current of $Tr_1$ and an increase in the collector current of $Tr_2$. This, in turn, results in an increase in the voltage at the collector of $Tr_1$ and a decrease in the voltage at the collector of $Tr_2$. 
The effect of the input signal \( V_{i1} \) then is to produce an inverted signal voltage at the collector of \( Tr_1 \) and an in-phase signal voltage at the collector of \( Tr_2 \). For signals \( V_{i1} \) and \( V_{i2} \) at both inputs, \( (V_{i1} - V_{i2}) \) is the differential input voltage, and \( (V_{o1} - V_{o2}) \) is the differential output voltage. Since there are two inputs and two outputs, the amplifier is said to have a double-ended input and a double-ended output. It is important to note that the system does not respond to a common mode signal, that is, a signal common to both inputs. To see this, we tie both inputs together and apply a signal, the constant current source prevents any change in collector current and hence there is no output signal in response. The circuit may be simplified by replacing the constant
current source with a resistor from the connected emitters to the negative supply. Also, if an output is needed from one collector only, then the resistor in the collector of the unused output may be removed and replaced by a short circuit. This modified circuit is shown in Fig. 5.51. A more complete discussion of the differential amplifier is presented in Chap. 7.

![Modified differential amplifier](image)

**Fig. 5.51** Modified differential amplifier

### 5.10 BJT Switch

The binary junction transistor can function as a switch, which is an important application in which a voltage supply is connected across a load. In this mode, the transistor is operated either in saturation (fully on), in which case the voltage drop across it is quite small, or in cut-off...
(fully off), in which case the current through the device is virtually zero. The basic circuit is shown in Fig. 5.52.

![Transistor switch diagram](image)

**Fig. 5.52 Transistor switch**

As we have seen before in the common emitter configuration, with the load resistor $R_L$ collector current and collector-emitter voltage operate along a load line such that if the base current (or base-emitter voltage) is at zero, the transistor is off and the collector voltage is at its maximum value the supply voltage. The collector current is then the very small collector leakage current $I_{CEO}$. If the base current is increased, then the collector current increases correspondingly thereby causing the collector-emitter voltage to fall. If the base current is increased sufficiently, the collector-emitter voltage falls to a very small value referred to as the saturation voltage $V_{CESat}$, which is typically $V_{CESat} \approx 0.2 \text{ V}$ with $V_{BEsat} \approx 0.7 \text{ V}$. The collector current is then at its maximum value $I_C \approx V_{CC}/R_L$ limited only by the resistor $R_L$, and the transistor is said to be in saturation. These ON–OFF regions are shown in the output characteristics in Fig. 5.53.
Thus, when functioning as an amplifier, the transistor operates in the active region where it is never in saturation or in cut-off so that full reproduction of the amplified signal is assured. However, when operated as a switch, the transistor is driven into either the fully ON state by supplying sufficient base current or the fully OFF state by reducing the base current to zero. This switching can be conveniently done by the application of a positive-going voltage pulse to the transistor base terminal through the base resistor $R_B$. When the voltage pulse is at zero, no base current flows into the transistor, and therefore, it is off. Since there is no collector current, no voltage therefore appears across $R_L$. When the voltage pulse goes positive, base current is injected into the transistor via the resistor $R_B$, and the transistor is switched on. As a result, almost the full supply voltage appears across the load resistor. The value of resistor $R_B$ determines the actual value of base current that flows and must therefore be carefully chosen. The input voltage that
switches the transistor on and off is often supplied by a digital circuit such as a microcomputer or other logic circuit where the voltage switches from zero corresponding to logical 0 and +5 V corresponding to logical 1.

Let the magnitude of the positive switching voltage be $V_L$. We now determine the value of the resistor $R_B$ for the transistor to be fully turned on when the input voltage is at $V_L$. Under full saturation, the collector-emitter voltage is at its saturation value, and most of the supply voltage is across $R_L$. Thus, the collector current at saturation is given by

$$I_{C_{sat}} = \frac{V_{CC} - V_{CE_{sat}}}{R_L} \approx \frac{V_{CC}}{R_L} \quad (5.85)$$

The value of base current, which flows when $V_i = V_L$, is given by

$$I_{B_{sat}} = \frac{V_L - V_{BE_{sat}}}{R_B} = \frac{V_L - 0.7}{R_B} \quad (5.86)$$

To ensure that the transistor is driven into saturation, $I_{B_{sat}} \geq \frac{I_{C_{sat}}}{\beta}$, which from (5.85) and (5.86) yields

$$\frac{V_L - 0.7}{R_B} \geq \frac{V_{CC}}{\beta R_L} \quad (5.87)$$

This reduces to

$$R_B \leq \frac{V_L - 0.7}{I_{C_{sat}}/\beta} = \frac{V_L - 0.7}{V_{CC}/R_L/\beta} \quad (5.88)$$

**Example 5.27**  A bipolar junction transistor is being used to switch 16 V across a 5 k load. Using an npn transistor with $\beta = 100$, design a simple switching circuit based on the circuit in Fig. 5.52 that is fully on when driven by a 5-V input.

**Solution**  The value of the collector current when the transistor is saturated is given by $I_{C_{sat}} = 16/5 = 3.2$ mA. Hence, the required input
resistor $R_B$ is given by $R_B \leq \frac{16\cdot0.7}{3.2\text{ mA}/100} = 478\text{ k}\Omega$. Use a 400 k\Omega to ensure that the transistor is saturated. This lower value of $R_B$ will result in a somewhat higher value of base current than that calculated for saturation.

5.10.1 BJT Device Switching
The power dissipated when the transistor is off is approximately zero because of the very small collector leakage current that flows through the transistor even though the collector-emitter voltage is large. The power dissipated when it is on is also very small because the collector-emitter voltage is very small even though the collector current is large. There can however be significant power dissipation in the transistor during the transition from one state to the other. In order to minimize this dissipation, the switching needs to take place rapidly. The actual switching time—the time between the application of the base voltage and the changed state of the transistor—is heavily influenced by junction capacitors within the transistor, specifically the collector-base capacitor and the base-emitter capacitor as shown in Fig. 5.54.
Consider the application of a voltage pulse through resistor $R_B$ to the transistor base as shown in Fig. 5.54. Because of the presence of the base-emitter junction capacitor $C_{BE}$, the input voltage does not cause an instantaneous rise in the base-emitter voltage, and, as a result, the collector-emitter voltage does not change instantaneously. This capacitor must be charged through $R_B$ such that the base-emitter voltage rises to approximately 0.7 V and this causes a delay after which the collector-emitter voltage starts to fall. The time duration between the application of the voltage pulse and the fall of the collector-emitter voltage from $V_{CC}$ to 0.9$V_{CC}$ is referred to as delay time $t_d$. During the time the transistor was off with the base at zero volts, the collector-base junction capacitor $C_{CB}$ was charged to $V_{CC}$ through the load resistor $R_L$, and this capacitor voltage appears across the transistor collector. Therefore, as the collector voltage falls in response to the base-emitter voltage, this junction capacitor must be discharged through the transistor in order that the collector voltage continues to fall. This further delays the decrease of the collector-emitter voltage, which
eventually reaches its saturation value $V_{CEsat}$. The time taken for the collector voltage to fall from $0.9V_{CC}$ to $0.1V_{CC}$ is referred to as the fall-time $t_f$, and the sum of the delay time and the fall time is the turn-on time $t_{on}$.

After the collector voltage attains its saturation value, the collector current cannot be further increased, and therefore any additional increase in the base current will result in excess charge storage in the base region of the transistor. When the input voltage pulse is reduced to zero, the need to remove this excess charge results in a delay in the turning off of the transistor. The base-emitter capacitor $C_{BE}$ must be discharged through $R_B$ so that the base-emitter voltage can fall and turn-off can begin. The time duration between the removal of the voltage pulse and the rise of the collector-emitter voltage to $0.1V_{CC}$ is the storage delay $t_S$. After this time, the transistor begins to turn off and the collector voltage rises. The rate of rise is limited by the recharging of the collector-base junction capacitor, which takes place through the load resistor $R_L$. The time taken for the collector voltage to rise from $0.1V_{CC}$ to $0.9V_{CC}$ is the rise time $t_R$, and the sum of the storage time and the rise time is called the turn-off time $t_{off}$. A plot of transistor switching voltages is shown in Fig. 5.55. Typical values for the turn-on times is 65 ns and turn-off time is 240 ns.
**5.10.2 BJT Switching Applications**

Several applications of the transistor switch are possible. Two examples are shown in Figs. 5.56 and 5.57. In the first, the transistor is used to switch on a small incandescent lamp. Here, the lamp replaces the load resistor in the basic circuit. When the input voltage goes high, the transistor is turned on, and the full supply voltage is placed across the lamp causing it to light. The current through the lamp on turn-on needs to be known so that the base resistor can be determined. The transistor must be able to handle the current load, and many small-to-medium power transistors will suffice. Because the value of $R_B$ depends on the transistor current gain and this parameter is variable, the minimum specified current gain value should be used in the calculation.
Example 5.28  A microcomputer operating on 5 V is being used to control a low-power incandescent lamp in an industrial application involving a supply of 12 V and a 12 V, 10 mA lamp. Calculate resistor $R_B$ such that this circuit is functional.
Solution  When the transistor is saturated, the value of the collector current is 10 mA. Hence, using a 2N3904 small signal transistor with $\beta = 100$, the required input resistor $R_B$ is given by

$$R_B \leq \frac{12-0.7}{10 \text{ mA}/100} = 113 \text{ k}\Omega.$$  Use a 100 kΩ to ensure that the transistor is saturated. If a Darlington pair with $\beta = 10,000$ is used, then

$$R_B \leq \frac{12-0.7}{10 \text{ mA}/100,000} = 1.1 \text{ M}\Omega.$$  This higher value of resistor would mean that the current being drawn from the output port of the microcomputer is significantly reduced and this is very desirable.

In the second application in Fig. 5.57, the transistor load is a relay coil, which, when activated, closes a set of contacts. This arrangement enables complete isolation between the transistor circuit and the circuit in which the contacts are connected. Again, the current through the coil when the full supply is applied needs to be known in order to calculate $R_B$. This circuit needs a diode across the coil as shown. This is because high voltages are generated in a coil when the current through the coil is suddenly interrupted. These voltages can result in the destruction of the transistor. The diode provides a current path such that these voltages do not damage the transistor.

5.11 FET Switch

Like the BJT, the FET can be operated as a switch. This can be done by controlling the gate-source voltage of the FET. In the case of an n-channel JFET, for example, the device is switched ON when the gate-source voltage is zero and the drain-source voltage is less than the pinch-off voltage. Under these conditions, the channel is conducting and no pinch-off has occurred. The device is OFF when the gate-source voltage is negative with a magnitude equal to the pinch-off voltage. In such a case, the channel is pinched off by the negative gate-source voltage, and therefore, no drain current flows for any value of drain-source voltage. The basic switching circuit is shown in Fig. 5.58 with these conditions illustrated in the output characteristics shown in Fig. 5.59. In order that the ON condition be operational, the value of load resistor $R_L$ must be such that the resulting drain current is less than $I_{DSS}$.
the maximum possible drain current, that is, $V_{DD}/R_L \leq I_{DSS}$ or $R_L \geq V_{DD}/I_{DSS}$. This ensures that the device stays in the linear or ohmic region where the channel resistance is of the order of hundreds of ohms and does not enter the saturation region. Resistor $R_G$ provides the gate-source connection necessary for application of the gate-source voltage while having a high input impedance to prevent loading the input voltage source.

*Fig. 5.58* Basic JFET switch
As in the case of the BJT, the junction capacitors of the JFET, namely, the gate-source capacitor and the drain-gate capacitor, heavily influence the switching times of the device. In Fig. 5.58, consider the application of a negative-going voltage pulse. Initially, the voltage is zero and the FET is ON. As the voltage pulse goes negative, in order that the device starts to turn off, the gate-source junction capacitor must be charged to beyond pinch-off. The absence of any resistor in the gate lead means that the delay caused by this charging action is small. Once the device starts to turn off, the rise of the drain voltage will be limited by the increase of the voltage across the drain-gate capacitor, which must be charged through $R_L$, which largely determines the rise time. The resulting delay is more significant than that caused by the charging of the gate-source capacitor. When the input voltage returns to zero, the reverse occurs. In order that the device starts to turn ON, the gate-source capacitor must be discharged, and this introduces a turn-on delay. After this occurs, the drain current will increase, and the drain voltage will fall. The drain-gate
capacitor will discharge through the FET channel, and since the channel resistance $r_D$ in the linear region is low, the fall time is low. Thus, since $R_L > r_D$ the turn-off time is much shorter than the turn-on time.

### 5.11.2 MOSFET Switch

In the case of the n-channel enhancement-type MOSFET shown in Fig. 5.60, a zero gate-source voltage corresponding to the switch off means that there is no channel conduction and hence the device is off. A positive gate-source voltage greater than the threshold voltage (corresponding to switch on) turns on the device and conduction results. For the depletion-type MOSFET, a zero gate-source voltage is insufficient to turn it off; a negative gate-source voltage is necessary for turn-off. The need for a bipolar signal for turn-on and turn-off in the case of the depletion-type MOSFET makes this MOSFET less useful as a switch than the enhancement type where only one signal polarity is necessary for turn-on and turn-off.
The enhancement MOSFET switch has large power capability and very high input impedance, which make it very suitable for connection to microcontroller or other logic circuit output in order to control high-power systems. However, the +5 V may be insufficient to overcome the threshold voltage of the MOSFET to turn it on. This problem may be solved by cascading a BJT switch and a MOSFET switch as shown in Fig. 5.61. Turning off the BJT applies +12 V to the gate of the MOSFET and turns it on. The input of the MOSFET can be damaged by electrostatic discharge. In order to protect the gate from over-voltage, a Zener diode clipping circuit $D_1$ can be used as shown in Fig. 5.61. An over voltage at the input will force the Zener diode into conduction thereby limiting the gate voltage. The excessive voltage is then dropped across $R_2$.

5.12 Voltage-Controlled Resistor
As has been already observed, the FET operates as a linear resistor in the ohmic region to the left of the pinch-off locus in Fig. 5.62. By varying the gate-source voltage, the value of this resistance can be varied.
thereby making the FET a voltage-controlled resistor. This action is evident in Fig. 5.63 for an n-channel JFET where for drain-source voltage less than the pinch-off voltage represented on the locus, the slope of the curves and hence the channel resistance vary with the gate-source voltage.

\[ I_D \text{(mA)} \]

\[ V_{GS}=0V \]

\[ -0.5V \]

\[ -1V \]

\[ -1.5V \]

\[ -2V \]

\[ -2.5V \]

\[ V_{DS}(\text{volts}) \]

**Fig. 5.62** \( I_D \) vs. \( V_{DS} \) of JFET
As $V_{GS}$ is made more negative, the curves become flatter corresponding to a higher resistance. An approximate value of this resistance can be obtained from Shockley’s equation

$$\text{(5.89)}$$
This resistance $r_d$ is given by

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Using $r_o = V_{DS}/I_{DSS}$, this can be written as

$$r_d = \frac{V_{DS}}{I_D} = \frac{V_{DS}}{I_{DSS}} \cdot \frac{1}{\left(1 - \frac{V_{GS}}{V_P}\right)^2}$$

(5.90)

Thus, minimum $r_d$ corresponds to $V_{GS} = 0$ and is determined by the geometry of the FET. A device having a channel with small cross-sectional area will exhibit high $r_o$ and low $I_{DSS}$. A family of n-channel FETs designed for use as voltage-controlled resistors is available from Siliconix. These devices have $r_o$ of between 20 and 4000 $\Omega$ with the VCR2N in the range 20$\Omega$–60$\Omega$, the VCR4N in the range 200$\Omega$–600$\Omega$ and the VCR7N in the range 4–8 k. One application of the VCR is a voltage-controlled attenuator shown in Fig. 5.64. By changing the negative gate-source voltage, the resistance $r_d$ varies resulting in an output signal $V_o$ given by $V_o = V_i \frac{r_d}{R + r_d}$.

A requirement of this circuit is that the voltage across the FET does not exceed the pinch-off voltage so that the device remains in the linear region.

Fig. 5.64 Voltage-controlled attenuator using VCR
5.13 Applications
Several circuits implementing multiple transistors and FETS are discussed in this section.

5.13.1 Microphone Preamplifier 1
A simple microphone preamplifier is shown in Fig. 5.65. It comprises a common emitter amplifier using a small-signal transistor followed by an emitter follower amplifier to provide a low output impedance. Using the design technique developed in Chap. 2, resistors $R_1$ and $R_2$ set the base voltage of $Tr_1$ to about 1.7 V. This along with $R_3$ establishes a quiescent current of 1 mA in $Tr_1$. Biasing $Tr_1$ for maximum symmetrical swing requires that resistor $R_4$ be 4 k. Selecting $R_5$ as 1 k sets a current in $Tr_2$ of 5 mA. The capacitor values are large to allow adequate low-frequency response.

![Fig. 5.65 Microphone preamplifier 1](image)
Ideas for Exploration: (i) Re-design the circuit using the 2N3906 pnp transistor, and compare the performance of the two circuits.

5.13.2 Microphone Preamplifier 2

Figure 5.66 shows the circuit of another microphone preamplifier. It employs a collector-base feedback-biased common emitter amplifier around $Tr_1$ and an emitter follower to reduce the loading on the collector of $Tr_1$ and reduce the output impedance of the circuit. For maximum symmetrical swing, the voltage across $R_2$ must be $9/2 = 4.5$ V. Using a collector current of 1 mA for $Tr_1$, then $R_2 = 4.5/1$ mA $= 4.5$ k. Using $\beta = 100$ for $Tr_1$, then the associated base current is $1$ mA/100 = $10$ $\mu$A. Hence, $R_1 = (4.5 - 0.7)/10$ $\mu$A $= 380$ k. Since the base of $Tr_2$ is directly connected to the collector of $Tr_1$, then the emitter of $Tr_2$ is at $4.5 - 0.7 = 3.8$ V. Choosing a current of 2 mA for $Tr_2$ to enable sufficient drive current for external loads, then $R_3 = 3.8/2$ mA $= 1.9$ k.

![Figure 5.66 Microphone preamplifier 2](image)

Ideas for Exploration: (i) Re-design the circuit using the 2N3906 pnp transistor, and compare the performance of the two circuits.

5.13.3 Logic Probe
This circuit shown in Fig. 5.67 is a logic probe that enables the determination of the state of a logic signal that can attain either a high state (+5 V) or a low state (0 V). Probe P2 is connected to the earth of the logic circuit, while probe P1 is connected to the logic signal. When there is no signal at P1 (floating probe), provided $V_{CC}$ is less than the sum of the voltage drops across the LEDs and the transistor base-emitter voltages, both transistors will be off and, hence, so will both LEDs. When P1 goes to a high state that exceeds the turn-on voltage of $Tr_1$ (0.7 V) and the red LED (1.7 V), which is approximately 2.4 V, then the red LED will turn on. $Tr_2$ will remain off. When P1 goes to a low voltage that is less than $V_{CC} - 2.8$, then there will be sufficient voltage across the GREEN LED (2.1 V) and the base-emitter junction of $Tr_2$ to turn them on. Resistors $R_3$ and $R_4$ serve to limit the current, and resistors $R_1$ and $R_2$ limit the base current into the transistors. Using a supply voltage of $V_{CC} = 3$ V, maximum input voltage of 5 V, and maximum LED current of 10 mA, then $R_3 = (5 - 0.7 - 1.7)/10$ mA $= 260$ Ω, where the LED voltage is 1.7 V. For low input voltage of zero and allowing an LED current of 2 mA, then $R_4 = (3 - 0.7 - 2.1)/2$ mA $= 100$ Ω. Resistors $R_1$ and $R_2$ can be about 1 k each in order to protect the transistor inputs from over-voltage.

![Fig. 5.67 Logic probe](image-url)
Ideas for Exploration: (i) Re-design the circuit to operate with a 9V battery.

5.13.4 Telephone Use Indicator
This circuit shown in Fig. 5.68 indicates telephone usage and is an improvement on the single-transistor telephone monitor of Fig. 2.65 in Chap. 2. When the telephone is in use, diode $D_5$ (red LED) is on and diode $D_6$ (green LED) is off. When the telephone is not being used, diode $D_5$ (red LED) is off and diode $D_6$ (green LED) is on. The diode bridge ensures that the DC signal into the transistor from the telephone line is always of the same polarity, regardless of the polarity orientation of the connection to the telephone line. With the telephone on hook, the telephone circuit is open and 48 V from the telephone exchange will appear across tip (T) and ring (R). This voltage is applied to potential divider $R_4$ and $R_5$ producing a voltage drop across $R_5$ that turns on transistor $Tr_2$ and hence also LED $D_6$ (green). For $R_5 = 2.2 \, k$ and $R_4 = 47 \, k$, the voltage across $R_5$ is $\{2.2/(47 + 2.2)\} \times 48 = 2.1 \, V$, which will ensure that $Tr_2$ turns on. During operation, this voltage will be limited to less than this value as $Tr_2$ turns on and current flows through $R_4$. Resistor $R_3$ limits the current through LED $D_6$ and a value of $R_3 = 27 \, k$ restricts the transistor collector current to about 2 mA. With $Tr_2$ saturated, its collector voltage is low, and hence transistor $Tr_1$, whose base is connected to $Tr_2$ collector via $R_2$, is off. As a result, LED $D_5$ is off. When the handset is lifted, the telephone circuit is closed and as a result of line resistance, the voltage across tip and ring will drop to about 9 V. This causes the voltage across resistor $R_5$ to fall to about 0.4 V. This causes $Tr_2$ to turn off. A current will now flow through the path $R_3, D_6, R_2$ into the base of $Tr_1$. For $R_2 = 27 \, k$, the value of this current is $(9 - 2.1 - 0.7)/54 \, k = 115 \, \mu A$. This current is not sufficient to light $D_6$, which therefore goes off. Transistor $Tr_1$ will now turn on with a collector current given by $115 \, \mu A \times \beta(Tr_1)$ which for $\beta = 100$ is 11.5 mA. However, resistor $R_1 = 1 \, k$ in the collector circuit of $Tr_1$ will limit this current to less than $9 \, V/1 \, k = 9 \, mA$. This will cause diode $D_5$ to turn on.
Ideas for Exploration: (i) Compare this system with the telephone monitor circuit in Chap. 2.

5.13.5 FET Cascode Amplifier

This amplifier shown in Fig. 5.69 utilizes two-junction field effect transistors in a cascode configuration similar to that of Sect. 5.7 using BJTs. Field effect transistor $Tr_1$ operates in the normal common source mode with resistors $R_1$ and $R_2$ selected according to the design rules in Chap. 3. Note that the gate of $Tr_1$ is held at zero volts by $R_1$ and current through $R_2$ causes the voltage at the source of $Tr_1$ to go positive thereby reverse-biasing the gate-source junction of $Tr_1$ and limiting the drain current to a selected value. The voltage $V_{G(Tr_2)}$ at the gate of $Tr_2$ set by $R_3$ and $R_4$ is equal to the drain-source voltage across $Tr_1$. Thus, if the voltage at the source of $Tr_1$ is $\Delta V$, then the voltage at the source of $Tr_2$ is $V_{G(Tr_2)} + \Delta V$. Finally, the load resistor $R_5$ is determined to ensure maximum symmetrical swing.
Ideas for Exploration: (i) Modify the circuit by using a JFET for Tr₂ that has a sufficient gate-source voltage to enable self-biasing of Tr₂ and the operation of Tr₁ in the saturation region. This would mean that components R₃, R₄, and C₂ would not be needed and the gate of Tr₂ would be connected to the source of Tr₁.
5.13.6 BJT Cascode Amplifier

The amplifier shown in Fig. 5.70 utilizes two binary junction transistors in a cascode configuration similar to that of Sect. 5.7 using BJTs but biased in a more conventional manner. Transistor $Tr_1$ operates in the normal common emitter mode. Choosing a quiescent current of 2 mA and using one tenth of the supply voltage as the emitter voltage of $Tr_1$ (2 V), resistor $R_5 = 1$ k. Allowing 1 V across $Tr_1$ for proper operation, for maximum symmetrical swing, the voltage across $R_4$ and $Tr_2$ is $(20 - 3)/2 = 8.5$ V. Therefore, $R_4 = 8.5/2 = 4.3$ k. Since the resistor chain $R_1$-$R_2$-$R_3$ is supplying base current to two transistor, we let the current $I$ down this chain be one-fifth (instead of one-tenth) of the collector current giving $I = 0.4$ mA. Since the emitter of $Tr_1$ is at 2 V, the base of $Tr_1$ is at 2.7 V and, hence, $R_3 = 2.7$ V/0.4 mA = 6.8 k. Since the voltage at the emitter of $Tr_2$ is 3 V, the base of $Tr_2$ is 3.7 V and, therefore, the voltage across $R_2$ is 1 V. Hence, $R_2 = 1$ V/0.4 mA = 2.5 k. The voltage across $R_1$ is 20 – 3.7 = 16.3 V and, hence, $R_1 = 16.3$/0.4 mA = 40.8 k. The gain of this circuit is given by $-40 \times 2$ mA $\times 4.3$ k = 344 = 51 dB, and its upper cut-off frequency was measured at 19 MHz.
**Ideas for Exploration:**

(i) Modify the circuit by using a JFET for $Tr_2$ that has a sufficient gate-source voltage to enable self-biasing of $Tr_2$ and the operation of $Tr_2$ in the active region. This would mean that capacitor $C_2$ would not be needed though it can be retained to provide supply filtering to the base of $Tr_1$. The gate of $Tr_2$ would then be connected to the emitter of $Tr_1$. 

*Fig. 5.70* BJT cascode amplifier
5.13.7 Touch-Sensitive Indicator

The next system to be discussed is a circuit that switches on when touched. The circuit is shown in Fig. 5.71. It consists of two transistors arranged such that the emitter of the first is connected to the base of the second (Darlington pair). There are current limiting resistors in the collector of each transistor with the second transistor including an LED in its collector. Touching the base and supply voltage simultaneously will cause a small current to flow in the base of $Tr_1$ where it is amplified by a factor of the transistor current gain. This amplified current now flows into the base of $Tr_2$ and is amplified further by a factor equal to the transistor current gain. The result is that a tiny current into the circuit at the base of $Tr_1$ is amplified by a factor of about $100 \times 100 = 10^4$ and results in a significant current flowing in the collector of $Tr_2$. The LED in the collector of $Tr_2$ is therefore illuminated. $R_2$ is determined by the current level required to turn on the LED. Thus, for a 9V supply and allowing about 15 mA to activate the LED, $R_2 = (9 - 2.1)/15 \text{ mA} = 460 \Omega$. Using the minimum value of the transistor current gain, the maximum current in $Tr_1$ is given by $15 \text{ mA}/100 = 0.15 \text{ mA}$. Hence, $R_1 = 9/0.15 \text{ mA} = 60 \text{ k}$. A value of 47 k is suitable.

![Fig. 5.71 Touch-sensitive indicator](image-url)
Ideas for Exploration: (i) Replace resistor $R_2$ and the LED by a relay coil (with protection diode), and use the circuit to switch on a mains connected device.

### 5.13.8 Electromagnetic Field Detector

This circuit is an enhancement of that in Fig. 5.71 and detects electromagnetic fields associated with house wiring, static electricity, and other sources. The circuit is shown in Fig. 5.72 and bears some similarity to a Darlington pair. It consists of three transistors arranged such that the emitter of the first is connected to the base of the second and the emitter of the second connected to the base of the third. There are current-limiting resistors in the collector of each transistor with the final transistor including an LED in its collector. Any current induced in the base of $\text{Tr}_1$ is amplified by a factor of the transistor current gain. This amplified current now flows into the base of $\text{Tr}_2$ and is amplified further by a factor equal to the transistor current gain. This amplification is continued in $\text{Tr}_3$ with the result that a tiny current into the circuit at the base of $\text{Tr}_1$ is amplified by a factor of about $100 \times 100 \times 100 = 10^6$ results in a significant current flowing in the collector of $\text{Tr}_3$. The LED in the collector of $\text{Tr}_3$ is therefore illuminated. $R_3$ is determined by the current level required to turn on the LED. Thus, for a 9V supply and allowing about 15 mA to activate the LED, $R_3 = (9 - 2.1)/15 \text{ mA} = 460 \ \Omega$. Using the minimum value of the transistor current gain, the maximum current in $\text{Tr}_2$ is given by $15 \text{ mA}/100 = 0.15 \text{ mA}$. Hence $R_2 = 9/0.15 \text{ mA} = 60 \text{ k}$ A value of 47 k is suitable. Similarly, $R_1 = 9/0.0015 \text{ mA} = 6 \text{ M}$, and a value of 1 M is suitable.
5.13.9 Nickel-Cadmium Battery Charger

The circuit on Fig. 5.73 is that of a nickel-cadmium battery charger. These batteries require a constant current for a fixed period for proper recharging. The circuit comprises an unregulated supply from a 40 V centre-tapped transformer that provides about \(20 \sqrt{2} = 28\) V across the filter capacitor \(C_1\). A value of 1000 \(\mu\)F ensures very little fall in voltage as currents up to 100 mA are drawn from the supply. Diodes \(D_3\) and \(D_4\) provide a fixed voltage at the base of \(Tr_1\) such that there is a 0.7 V across resistor \(R_2\). This results in a constant current of \(0.7/R_2\) in the collector of \(Tr_1\). The value of \(R_2\) is determined by the constant current to be supplied. For 50 mA, \(R_2 = 0.7/50\ mA = 14\ \Omega\). Resistor \(R_1\) supplies current to diodes \(D_3\) and \(D_4\) and to the base of \(Tr_1\). For 5 mA through these diodes, \(R_1 = (28 – 1.4)/5\ mA = 5.3\ k\). This constant current source can accommodate increase in battery voltage up to about 20 V. Significant heat is dissipated in the transistor, so it should be a power transistor such as the 2N3055 and should be mounted on a heatsink in order to dissipate the heat. Note that the system does not have an end-of-charge feature to turn off the system. This has to be done manually.
Ideas for Exploration: (i) Recalculate the value of $R_2$ in order to charge batteries requiring different charging currents and introduce a single-pole multi-throw switch to enable easy changing of the charging current.

5.13.10 Audio Level Meter

This circuit shown in Fig. 5.74 is an audio level meter that measures the amplitude of an audio signal coming from a preamplifier, which is in the range 20Hz–20kHz. It utilizes two common emitter stages that amplify the audio signal. For the first stage, choosing a collector current of 0.5 mA and allowing 1 V at the emitter of $Tr_1$, the resistance of $VR_1$ is $1 \, \text{V}/0.5 \, \text{mA} = 2 \, \text{k}$. A 2 k potentiometer is used and connected in the manner shown to enable variation of the gain of this stage. The voltage at the base of $Tr_1$ is 1.7 V. Let the current down the $R_1$-$R_2$ chain be 0.05 mA, which is one-tenth the collector current. Then, $R_1 = 1.7/50 \, \mu\text{A} = 34 \, \text{k}$ and $R_2 = (12 - 1.7)/0.05 \, \text{mA} = 206 \, \text{k}$. The available voltage swing at the collector of $Tr_1$ is $12 - 1 = 11 \, \text{V}$. Hence, for maximum swing, $R_3 = 5.5/0.5 \, \text{mA} = 11 \, \text{k}$. In the second transistor, choosing a collector current of 0.5 mA, then for maximum symmetrical swing $R_6 = 6/0.5 = 12 \, \text{k}$. The associated base current is $0.5 \, \text{mA}/100 = 5 \, \mu\text{A}$. Therefore, $R_5 = (6 - 0.7)/5 \, \mu\text{A} = 1 \, \text{M}$. Resistor $R_4$ is selected to allow calibration for full-scale deflection using $VR_1$. A value $R_4 = 10 \, \text{k}$ is used. At the input, $C_1 = 10 \, \mu\text{F}$ couples signals into the system. At the output of $Tr_2$, capacitor $C_4 = 10 \, \mu\text{F}$ couples the signal to
the diode bridge, which allows unidirectional current flow through the microammeter. The high output impedance (12 k) of the second stage ensures that there is a controlled current flow through the microammeter. During operation with $C_2$ large (100 μF), $VR_1$ is adjusted such that a 100 mV input signal results in full-scale deflection of the meter (100 μA).

![Audio level meter diagram](image)

**Fig. 5.74** Audio level meter

**Ideas for Exploration:** (i) Introduce a resistor in series with capacitor $C_1$ that allows the system to be driven by the output of a power amplifier where the output voltage goes up to 50 V corresponding to power amplifiers with outputs just over 100 W.

### 5.13.11 Speaker to Microphone Converter

The circuit in Fig. 5.75 converts a loudspeaker into a very sensitive microphone. Transistor $Tr_1$ is connected in the common base mode with collector-base feedback biasing while $Tr_2$ is connected as an emitter follower to provide a low output impedance. A current of 1 mA in $Tr_1$ means that $R_3 = 4$ k results in 5 V at the collector of the transistor. Resistor $R_1 = 500$ Ω ensures that the signal input is not shorted to ground. This means that the transistor emitter is at 0.5 V. Hence, $R_2 = (9 - 4 - 0.7 - 0.5)/5 \mu A = 760$ k. A transistor current gain of 200 is
assumed. Resistor $R_2$ may need to be adjusted for different gains. $Tr_1$ collector voltage of 5 V results in the emitter voltage of $Tr_2$ as 4.3 V. For 2 mA in $Tr_2$, $R_4 = 4.3 \text{ V}/2 \text{ mA} = 2.2 \text{ k}$. Capacitors $C_1$ and $C_2$ are coupling capacitors, while capacitor $C_3$ grounds the base of $Tr_1$ for operation as a common base amplifier.

![Speaker to microphone converter](image)

**Fig. 5.75** Speaker to microphone converter

*Ideas for Exploration:* (i) Compare this circuit with the speaker-to-microphone circuit of Chap. 2; (ii) introduce bootstrapping of a fraction of $R_3$ in order to increase the gain of the circuit thereby making the system an even more sensitive microphone.

### 5.13.12 Sound to Light Converter

This circuit in Fig. 5.76 converts sound to light signals. An electret microphone at the input converts sound into an electrical signal that is fed into transistor $Tr_1$ via capacitor $C_1$. $Tr_1$ is connected as a simple common emitter amplifier with collector-base feedback. The collector current is set at 2 mA to ensure that sufficient drive current is available to drive the four connected transistors. For maximum symmetrical swing, the voltage across $R_3$ is 4.5 V. Hence $R_3 = 4.5 \text{ V}/2 \text{ mA} = 2.2 \text{ k}$. Resistor $R_2 = (4.5 - 0.7)/0.02 \text{ mA} = 190 \text{ k}$ where a current gain of 100 is used. The collector of $Tr_1$ is direct coupled to $Tr_2 - Tr_5$, each of which has
an LED in the collector and a 1 k resistor in the emitter. This ensures that the input impedance to these transistor amplifiers is high (better than 100 k), thereby allowing \( Tr_1 \) to drive several such transistors. This resistor also serves to define the current in each of these transistors in response to the signal from \( Tr_1 \). These LEDs vary in brightness in response to the input from the microphone.

![Sound to light converter](image)

**Fig. 5.76** Sound to light converter

*Ideas for Exploration:* (i) Replace the microphone by the output from the auxiliary output from a cell phone, and observe the effect of playing music through the system. The lights should respond to the varying music signal amplitude.

### 5.13.13 Low Drift DC Voltmeter

The circuit in Fig. 5.77 is that of a low drift voltmeter. It is an improved version of the JFET voltmeter introduced in Chap. 3 as it is less subject to drift. It comprises two 2N3919 JFETs connected as a differential amplifier so that any drift occurs in both devices with little effect on the system. Resistors \( R_7 = 68 \, k \) and \( R_8 = 33 \, k \) provide a reference point G as zero potential such that, with a 12 V supply, point A is at +8 V and point B is at −4 V. The gates of both JFETS are at zero potential and for a drain current of 1 mA, Shockley’s equation gives \( V_{GS} = -2.8 \, V \). Hence, with a −4 V potential, resistor \( R_5 \) plus part of the resistance of \( VR_2 \) is given by
(2.8 − (−4))V/1 mA = 6.8 k. The same calculation holds for \( R_6 \) plus part of the resistance of \( VR_2 \). Choose \( VR_2 = 10 \) k. Then, half of this plus \( R_5 = 1.8 \) k gives the required 6.8 k. Similarly, \( R_6 = 1.8 \) k. Resistor \( R_4 = 100 \) k protects the gate of the input device, while \( R_1 = 1.8 \) M, \( R_2 = 180 \) k, and \( R_3 = 20 \) k form an input attenuator. Potentiometer \( VR_2 \) zeros the meter for zero input voltage. For a 0.5 V signal at the gate of the FET, most of this is dropped across the meter circuit. Hence, the resistance \( VR_1 \) in series with the meter is given by \( VR_1 = 0.5 \) V/100 \( \mu \)A = 5 k. This potentiometer must be adjusted for full-scale deflection with 0.5 V at the input.

![Figure 5.77 Low drift DC voltmeter](image)

*Ideas for Exploration:* (i) Re-design the system to operate from a 9 V battery for portability.

### 5.13.14 AC Millivoltmeter

The AC voltmeter of Chap. 4 (Fig. 4.62) had a full-scale deflection for 1 V. In order to increase the sensitivity, a second amplifying stage must be added as shown in Fig. 5.78. For quiescent current stability in the output stage, let the emitter voltage be 2 V. Choosing a collector current of
0.5 mA for low-current operation, then $R_6 = 4 \, \text{k}$, and with maximum symmetrical swing, $R_5 = 3.5/0.5 \, \text{mA} = 7 \, \text{k}$. Let the collector current of $Tr_1$ be 0.5 mA. Setting $R_4 = 1.5 \, \text{k}$ in order to achieve a high input impedance to $Tr_1$, then the voltage at the emitter or $Tr_1$ is $0.5 \, \text{mA} \times 1.5 \, \text{k} = 0.75 \, \text{V}$. Noting that the base current of $Tr_1$ is 0.005 mA, this gives $R_2 = (2 - 1.45)/0.005 \, \text{mA} = 110 \, \text{k}$. The voltage at the base of $Tr_2$ is 2.7 V. Hence, $R_3 = (9 - 2.7)/0.5 \, \text{mA} = 12.6 \, \text{k}$. Resistor $R_A = 1 \, \text{k}$ is made variable in order to set the f.s.d. input signal amplitude. For signals, it is effectively in parallel with $R_4$ giving $R = R_4//R_A$. Using equivalent circuit representation, the value of this resistor $R$ for full-scale deflection with an input signal $V_i$ is given by $R \approx 0.75 \frac{V_i}{I_m}$. Thus for $I_m = 100 \, \mu\text{A}$ and $V_i = 100 \, \text{mV}$, $V_{B1} = \frac{37}{300} \times 30 = 3.7 \, \text{V}$. The correct value is likely to be lower than this and is attained by adjusting $R_A$. Resistor $R_1 = 1 \, \text{k}$ provides some level of protection to the input transistor from overvoltage.
Ideas for Exploration: (i) Introduce an attenuator to extend the range of the meter to 100 V.

5.13.15 High-Power Zener Diode

The high-power Zener diode circuit shown in Fig. 5.79 increases the power rating of the power Zener diode of Fig. 2.67 in Chap. 2. It achieves this by including a medium power transistor $Tr_1$ such as the 2N3053 to drive the power transistor $Tr_2$, which can be an MJ2955. Again, $R_1$ sets the current through the Zener diode $D_1$ at $0.7/R_1$ and $R_2$ sets the current through $Tr_1$ at $0.7/R_2$. The effective Zener voltage of the system is $V'_z = V_z + 0.7$. The advantage of this circuit over that in Fig. 2.67 is the base current of the power transistor $Tr_2$ flows through $Tr_1$ while the base current of the power transistor $Tr_1$ in Fig. 2.67 is supplied by the Zener diode. Hence, higher currents through the system can be accommodated. $R_1 = 700\ \Omega$ sets the Zener diode current at $1\ \text{mA}$ and $R_2 = 1\ \text{k}$ sets the collector current of $Tr_1$ at $0.7\ \text{mA}$. Most of the current through the system is bypassed by $Tr_2$. 

![Circuit Diagram](image)
**Ideas for Exploration:** (i) Utilize the system in a high-current regulated power supply; (ii) Redesign the circuit to use an npn power transistor such as the 2N3055 for \( Tr_2 \) and a suitable pnp medium power transistor for \( Tr_1 \).

### 5.13.16 Improved Audio Mixer

This circuit in Fig. 5.80 is that of an improved audio mixer. It is an improved version of the audio mixer presented in Fig. 2.66 in Chap. 2. This circuit also uses a common base amplifier to enable the mixing of signals from several sources. It consists of transistor \( Tr_1 \) in which the base is held at a fixed voltage 3.3 V using a zener diode instead of the two forward-biased diodes. Current through the Zener diode is supplied from a 15-V supply through a resistor \( R_5 \). Transistors \( Tr_2 \) and \( Tr_3 \) form a current source that provides a constant current to the emitter of transistor \( Tr_1 \). The high impedance of this current source ensures that all input signals through resistors \( R_1, R_2, R_3 \) do enter the low-impedance input of \( Tr_1 \). The constant current value flowing through \( Tr_2 \) and hence \( Tr_3 \) is set by \( R_6 \). Using \( R_3 = 330 \, \Omega \) gives a current of \( 0.7/R_6 = 0.7/330 = 2 \) mA. Choosing a current of 1 mA in \( Tr_3 \), then \( R_7 = (3.3 - 0.7 - 0.7)/1 \) mA = 1.9 k. Allowing 4 mA into the zener diode, then \( R_5 = (15 - 3.3)/(4 \) mA + 1 mA) = 2.3 k. Capacitor \( C_5 \) ensures that the transistor base is grounded for signals. For maximum symmetrical swing, the quiescent voltage across \( R_4 \) must be equal to the quiescent collector-emitter voltage of \( Tr_1 \) giving \( V_{CE}(Tr_1) = V_{R_4} = (15 - 0.7 - 0.7)/2 = 6.8 \) V.

Hence, \( R_4 = 6.8/2 \) mA = 3.4 k. Input and output coupling capacitors \( C_1 \) to \( C_4 \) are chosen to be large values for good low-frequency response. The input impedance at the emitter is \( 1/40I_C = 1/40 \times 2 \) mA = 12.5 Ω, which is very low. By choosing signal input resistors \( R_1 \) to \( R_3 \) to be much greater than 12.5 Ω say 10 k, very good signal mixing occurs at the transistor emitter with very low channel interaction (cross-talk). Additional inputs can be introduced if required.
5.13.17 Research Project 1

The circuits considered up to this point generally utilize small signal transistors. This project involves the design of an amplifier using the design principals presented thus far that will accept signal from a source such as the auxiliary output of a cell phone and drive a loudspeaker to give audible output. This is a prelude to the particularly interesting subject of power amplifier design, which will be fully introduced in Chap. 9. The circuit is shown in Fig. 5.81. It comprises a common emitter amplifier using a small signal transistor $Tr_1$, driving a power transistor $Tr_2$ also connected in the common emitter mode. $Tr_2$ drives an 8 Ω loudspeaker connected in its collector circuit. Resistor $R_3$ should result in about 120 mA in the collector of $Tr_2$. This will produce about 50 mW
into an 8 Ω loudspeaker. Some experimentation here with the value of $R_3$ may be necessary. The power transistor can be a 2N3055. It should be mounted on a small heatsink in order to dissipate any heat produced. Note also that the collector current of the power transistor flows through the speaker resulting in a permanent displacement of the speaker cone. It should be noted that speakers with small diameters do not operate well under this condition.

![Low-power amplifier](image)

**Fig. 5.81** Low-power amplifier

*Ideas for Exploration:* (i) Replace the power transistor by a power Darlington such as the MJ3000. Resistor $R_3$ would have to be increased for the same value of collector current. The Darlington will provide a higher input impedance which reduces loading on $Tr_1$ and thereby increase the sensitivity of the system, that is, a lower signal voltage will drive the system; (ii) introduce a volume control by including a potentiometer $VR_1 = 10 \, k$ at the input. The signal source then drives the potentiometer and the potentiometer wiper is connected to the amplifier input as shown in Fig. 5.82; (iii) using the MOSFET amplifier of Fig. 3.57 in Chap. 3, replace the power BJT and implement the power amplifier.
Fig. 5.82  Low-power amplifier with volume control

5.13.18 Research Project 2

This project is a further development of the crystal radio project. The system from Chap. 2 where a germanium transistor was used instead of a germanium diode is employed here as the input signal source to the low-power amplifier of research project 1 discussed earlier. The combined system is shown in Fig. 5.83. Capacitor $C_3$ must be about 470 pF and filters the carrier from the modulated radio frequency signal. Capacitor $C_4$ provides power supply decoupling such that the inductance associated with the power leads does not affect the system performance. Its value can be about 100 μF. Resistor $R_1$ in the previous system is here replaced by potentiometer $VR_1 = 10$ k.
Ideas for Exploration: (i) Experiment by reducing the length of the antenna; (ii) introduce a radio frequency signal booster as shown in Fig. 5.84. This simple circuit (used in Chap. 3) uses an MPF102 or other suitable JFET in the common source mode. Resistor $R_1 = 1 \text{ M}$ ensures that the gate is grounded for JFET biasing. $C_1 = C_2 = 1000 \text{ pF}$ are coupling capacitors which can be small since the circuit is operating at high frequencies (540–1600 kHz).
The inductor $L_1 = 500 \ \mu\text{H}$ at 1 MHz say has a reactance $X_L = 2\pi f L = 3.1 \ \text{k}$. Therefore, with $g_m \approx 5 \ \text{mA/V}$ for the MPF102, the circuit gain for signals at 1 MHz is $g_m X_L = 5 \ \text{mA} \times 3.1 \ \text{k} = 15.5$. Capacitor $C_3 = 0.1 \ \mu\text{F}$ provides decoupling of the power supply to ensure reduced noise. The antenna to this circuit can now be a portable telescopic type. The output of this RF signal booster goes to the tank circuit of the advanced crystal radio in Fig. 5.81 and replaces the long-wire antenna previously used.

**Problems**

1. Draw the equivalent circuit of the two-stage amplifier in Fig. 5.85. Determine the voltage gain $V_o/V_s$ and, hence, the current gain $I_o/I_s$. Assume $h_{fe} = 100$ for both transistors.

2. Draw the equivalent circuit of the two-stage amplifier in Fig. 5.86. Determine the voltage gain $V_o/V_s$ and, hence, the current gain $I_o/I_s$. Assume $h_{fe} = 200$ for both transistors.

3. Draw the equivalent circuit of the two-stage amplifier in Fig. 5.87. Determine the voltage gain $V_o/V_s$ and, hence, the current gain $I_o/I_s$. Assume $h_{fe} = 500$ for both transistors.
Assume $h_{fe} = 100$ for both transistors.

4. Draw the equivalent circuit of the two-stage amplifier in Fig. 5.88. Determine the voltage gain $V_o/V_s$ and, hence, the current gain $I_o/I_s$. Assume $h_{fe} = 100$ for both transistors.

5. Using the two-stage design in Fig. 5.7 and a 40-V supply, design a two-stage amplifier that can drive a low-impedance load. Determine the voltage gain of the amplifier. Determine the value of the resistor that can be introduced in the emitter of the first stage as shown in Fig. 5.8 in order to lower the voltage gain to −25.

6. Design a two-stage amplifier having a JFET input stage using the topology of Fig. 5.9 and a 25-V supply. Use a JFET with $V_P = -5$ V and $I_{DSS} = 5$ mA. Determine the voltage gain of the circuit, and state the main advantage of the JFET stage.

7. Design a low input impedance two-stage amplifier using the circuit of Fig. 5.10 and a 20-V supply. Determine the input and output impedances as well as the voltage gain.

8. Using the configuration in Fig. 5.89, design a direct coupled amplifier with high gain. Use a supply voltage of 26 V, and calculate the gain of your circuit.

9. Explain the principle of bootstrapping, and use the technique to increase the gain of the circuit in Question 8.

10. Replace the transistor in the first stage of Fig. 5.89 by a JFET, and re-design the circuit.

11. Design a common emitter amplifier using a pnp Darlington package having $\beta_D = 2000$ and a 30-V supply. Calculate the voltage gain of your circuit.

12. Introduce partial bypassing of the emitter resistor in Question 11 in order to achieve a gain of 50. Show that the current gain of a Darlington pair is approximately
13. equal to the product of the current gains of the two transistors making up the pair.

14. Design a common collector amplifier using a Darlington package having $\beta_D = 1000$ and a 32-V supply. Calculate the input impedance of your circuit.

15. Apply bootstrapping in order to increase the input impedance of the circuit and estimate the value of this impedance.

16. Show that current gain of a feedback pair is approximately equal to the product of the current gains of the two transistors making up the pair.

17. Derive the voltage gain of a feedback pair in a common emitter configuration, and show that it is significantly higher than either the Darlington pair or a single BJT.

18. Design a circuit using BJTs in a feedback pair to have a gain of 8. Use a supply voltage of 15 V.

19. Repeat the design in Question 18 with a JFET as the input transistor.

20. Using the configuration in Fig. 5.90, design a constant current source that produces a current of $I = 5$ mA from a 15-V supply.

21. Using the basic circuit of Question 20, show how a pnp transistor can be used to supply a constant current to a grounded load.

22. Using the configuration in Fig. 5.91, design a constant current source that produces a current of 0.5 mA from a 15-V supply.

23. Repeat the design in Question 22 using pnp transistors.

24. Using a JFET having $V_P = -4$ V and $I_{DSS} = 4$ mA, design a constant current source with current value 1 mA. Determine the current if $R_S = 0$. 
25. Design a two-transistor current mirror giving a constant current of 0.5 mA using a 12-V supply.
26. Design a Wilson current mirror to deliver a constant current of 1.5 mA using a 16-V supply.
27. In Fig. 5.92, determine $I_1$, $I_2$, $V_1$, and $V_2$.
28. In Fig. 5.93, determine $I_1$, $I_2$, $I_3$, and $I_4$.
29. In Fig. 5.94, determine $I_1$, $I_2$, $V_3$, and $V_4$.
30. In Fig. 5.95, determine $I_1$, $I_2$, $I_3$, and $I_4$.
31. Using the circuit of Fig. 5.96, design a cascode amplifier to operate from a 32-V supply, and determine the voltage gain of the circuit.
32. Using a bipolar 15-V supply, set up a two-transistor differential amplifier with each transistor having 1 mA quiescent current. Use matched transistors and equal collector resistors and design for maximum symmetrical swing.
33. A bipolar junction transistor is being used to switch 12 V across a 10 k load. Using an npn transistor with $\beta = 150$, design a simple switching circuit that is fully on when driven by a 5-V input.
34. Using an enhancement MOSFET design a switch to drive a 12-V 5 mA relay from a 12-V supply. The device has a threshold voltage of 3 V.
35. Investigate the properties and characteristics of a negative temperature coefficient thermistor. Using such a thermistor and the circuit shown in Fig. 5.97, design a heat sensing system that sounds an alert when the ambient temperature reaches a particular value.
Fig. 5.85 Circuit for Question 1
**Fig. 5.86** Circuit for Question 2

**Fig. 5.87** Circuit for Question 3
Fig. 5.88  Circuit for Question 4

Fig. 5.89  Circuit for Question 8
Fig. 5.90  Circuit for Question 20
Fig. 5.91 Circuit for Question 22
Fig. 5.92 Circuit for Question 27
Fig. 5.93  Circuit for Question 28
Fig. 5.94 Circuit for Question 29
Fig. 5.95  Circuit for Question 30
Fig. 5.96 Circuit for Question 31
Fig. 5.97  Circuit for Question 35

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6. Frequency Response of Transistor Amplifiers

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In the previous chapters, we discussed the mid-frequency performance of an amplifier. At these frequencies, the coupling and bypass capacitors pass the signals virtually unimpeded, while the transistor junction capacitors are considered as open circuits. The BJT and FET models served as useful tools to analyze these circuits. The performance at low and high frequencies however requires further consideration. In the case of the low frequencies, the effect of the coupling and bypass capacitors needs to be determined, while at high frequencies the response which is largely determined by transistor junction capacitances needs to be ascertained. In this chapter, therefore, more complex equivalent circuits are introduced in order to examine the full frequency response characteristics of BJTs and FETs. While the analysis is done using the JFET, it also applies in general to the MOSFET. After completing this chapter, the reader will be able to:

- Determine the low-frequency response of transistor amplifiers
- Determine the high-frequency response of transistor amplifiers
6.1 BJT Low-Frequency Response

In the previous chapters on the BJT and the FET, all coupling and bypass capacitors were chosen to be large such that these capacitors represented short-circuits to the signal currents passing through them. If, however, the signal frequency is sufficiently low, the reactance of these capacitors becomes significant and can affect signal levels in the circuit. In this section, the circuits are analyzed in order to determine the effect of the capacitors so that appropriate values may be chosen for optimum circuit response. In preparation for doing so, we consider the RC circuit in Fig. 6.1 with an input sinusoidal signal $V_i$ and an output signal $V_o$. The reactance of the capacitor in the complex frequency domain $s$ is $1/sC$ where $s = j\omega$ and $\omega$ is the angular frequency that is related to frequency $f$ by $\omega = 2\pi f$. The transfer function $V_o/V_i$ for the circuit is given by

$$A_V = \frac{V_o}{V_i} = \frac{R}{R + 1/sC} = \frac{sCR}{1 + sCR}$$

![Fig. 6.1 CR circuit](image)

The magnitude of this transfer function is given by

$$|A_V| = \frac{1}{\sqrt{1 + (\omega R C)^2}}$$
From (6.2), when \( \omega CR \gg 1 \), then \( |A_V| = 1 \) and when \( \omega CR \ll 1 \), then \( |A_V| = \omega CR \). Thus for \( \omega CR \ll 1 \), converting \( |A_V| \) to decibels using \( |A_V| \text{ dB} = 20 \log |A_V| \), we have

\[
|A_V| \text{ dB} = 20 \log \omega CR = 20 \log \omega + 20 \log CR
\]  \hspace{1cm} (6.3)

This can be written as

\[
|A_V| \text{ dB} = 20 \log f + 20 \log 2\pi CR = 20 \log f - 20 \log f_o
\]  \hspace{1cm} (6.4)

where \( f_o = 1/2\pi RC \) corresponding to \( \omega_o = 1/RC \). Equation (6.4) is that of a straight line on a \( |A_V| \text{ dB} - \log f \) graph with slope + 20 dB/decade and \( |A_V| \text{ dB} = 0 \) at \( f = f_o \) as shown in Fig. 6.2. On the same graph, we have \( |A_V| = 1 \) for \( \omega CR > 1 \) which is equivalent to \( f > f_o \). At \( f = f_o \),

\[
|A_V| = \frac{\omega CR}{\sqrt{1 + \omega^2 C^2 R^2}} = \frac{1}{\sqrt{1 + 1}} = 1/ \sqrt{2} = 0.707 = -3 \text{ dB}
\]  \hspace{1cm} (6.5)
This response is that of a high-pass filter and is essentially the response of input and output coupling capacitors at low frequencies. We now consider these responses.

### 6.1.1 Input Coupling Capacitor

Consider the fixed-bias common emitter amplifier circuit shown in Fig. 6.3 where a coupling capacitor $C_i$ passes the input signal $V_i$ into the base of the transistor. The $h$-parameter equivalent circuit is shown in Fig. 6.4 with the coupling capacitor $C_i$ included. The reactance of the capacitor in the complex frequency domain $s$ is $1/sC_i$ where $s = j\omega$ and $\omega$ is the angular frequency that is related to frequency $f$ by $\omega = 2\pi f$. From the equivalent circuit,

$$V_i = I_b (h_{ie} + 1/sC_i)$$  \hspace{1cm} (6.6)

$$V_o = -I_b h_{fe} R_L$$  \hspace{1cm} (6.7)
Therefore, the voltage gain $A_V$ is given by
\[ A_V = \frac{V_o}{V_i} = -\frac{h_{fe}R_L I_b}{(h_{ie} + 1/sC) I_b} = -\frac{h_{fe}R_L sC_i}{1 + sC_i h_{ie}} \]  \hspace{1cm} (6.8)

In order to plot the gain magnitude \(|A_V|\) against frequency \(f\), consider the following:

\[ |A_V| = \left| \frac{-h_{fe}R_L sC_i}{1 + sC_i h_{ie}} \right| = \left| \frac{-h_{fe}R_L sC_i}{1 + sC_i h_{ie}} \right| = \frac{h_{fe}R_L \omega C_i}{\sqrt{1 + \omega^2 C_i^2 h_{ie}^2}} \]  \hspace{1cm} (6.9)

When \(\omega C_i h_{ie} \gg 1\), then

\[ |A_V| \rightarrow \frac{h_{fe}R_L \omega C_i}{\omega C_i h_{ie}} = \frac{h_{fe}R_L}{h_{ie}} \]  \hspace{1cm} (6.10)

which is the common emitter mid-frequency gain when \(C_i\) is treated as a short-circuit derived in Chap. 4. The magnitude of this gain converted to decibels is given by

\[ |A_V|_{dB} = 20 \log \left(\frac{h_{fe}R_L}{h_{ie}}\right) \]  \hspace{1cm} (6.11)

Now let \(\omega_L = 1/C_i h_{ie}\) which means \(f_L = 1/2\pi C_i h_{ie}\). Then \(\omega C_i h_{ie} \gg 1\) corresponds to \(\omega \gg \omega_L\) or \(f \gg f_L\). For \(\omega C_i h_{ie} \ll 1\) which corresponds to \(\omega \ll \omega_L\) or \(f \ll f_L\), then

\[ |A_V| = \frac{h_{fe}R_L}{h_{ie}} \omega C_i h_{ie} = \frac{h_{fe}R_L \omega}{h_{ie} \omega_L} \]  \hspace{1cm} (6.12)

which in decibels becomes

\[ |A_V|_{dB} = 20 \log \left(\frac{h_{fe}R_L \omega}{h_{ie} \omega_L}\right) = 20 \log \left(\frac{h_{fe}R_L f}{h_{ie} f_L}\right) \]  \hspace{1cm} (6.13)

This can be written as

\[ |A_V|_{dB} = 20 \log f + 20 \log \frac{h_{fe}R_L}{h_{ie}} - 20 \log f_L \]  \hspace{1cm} (6.14)
On a $|A_V|_{\text{dB}}$ vs. log $f$ plot, (6.14) represents a straight line of slope 20 which at $f = f_L$ gives $|A_V|_{\text{dB}} = 20 \log \frac{h_{fe}R_L}{h_{ie}}$, where it intersects the line (6.11). The slope has units dB/decade and is 20 dB/decade since for every decade or for a factor of 10 increase in the frequency, the gain increases by 20 dB which is itself a factor of 10. Finally, from (6.8),

$$A_V(s) = -\frac{h_{fe}R_L sC_i}{1 + sC_i h_{ie}} = -\frac{h_{fe}R_L}{h_{ie}} \frac{sC_i h_{ie}}{1 + sC_i h_{ie}} \tag{6.15}$$

At $f = f_L$ corresponding to $\omega = \omega_L$, (6.15) becomes

$$A_V(f_L) = -\frac{h_{fe}R_L}{h_{ie}} \frac{j\omega C_i h_{ie}}{1 + j\omega C_i h_{ie}} = -\frac{h_{fe}R_L}{h_{ie}} \frac{j}{1 + j} \tag{6.16}$$

$$g_m = \frac{-2I_{DSS}}{V_P} \left(1 - \frac{V_{GS}}{V_P}\right) = -2 \cdot \frac{10}{-8} \left(1 - \frac{2.34}{8}\right) = 1.77 \text{ mA/V.} \tag{6.17}$$

This gives

$$|A_V(f_L)|_{\text{dB}} = \left[20 \log \left(\frac{h_{fe}R_L}{h_{ie}}\right) - 3\right]_{\text{dB}} \tag{6.18}$$

Therefore, at the frequency $f = f_L$, the magnitude of the gain falls by 3 dB from its mid-band value. This frequency is referred to as the low-frequency cut-off, and the reduction in gain as the frequency falls below this frequency arises because of the effect of the coupling capacitor. The frequency response plot for this circuit is shown in Fig. 6.5.
Thus, the value of $C_i$ sets the lower cut-off frequency of the common emitter amplifier of Fig. 6.3 and is given by

$$f_L = \frac{1}{2\pi h_{ie} C_i}$$

(6.19)

In general, the lower cut-off frequency $f_L$ should be lower than some value $f_{L}^*$. Hence

$$C_i \geq \frac{1}{2\pi h_{ie} f_{L}^*}$$

(6.20)

**Example 6.1** For the amplifier circuit shown in Fig. 6.6 which is biased for maximum symmetrical swing, determine a suitable value of coupling capacitor to realize a maximum lower cut-off frequency of 50 Hz.
**Solution** Since the circuit is biased for maximum symmetrical swing, it follows that \( V_{CEq} = 24/2 = 12 \text{ V} \), and hence \( I_{Cq} = 12 \text{ V}/12 \text{ k} = 1 \text{ mA} \). This gives \( h_{ie} = h_{fe}/40I_C = 100/40 \times 1 \text{ mA} = 2.5 \text{ k} \). Noting that \( h_{ie} \ll R_B \), it follows from (6.20) that 
\[
C_i \geq \frac{1}{2\pi h_{ie} f_L} = \frac{1}{2\pi \times 2.5 \times 10^3 \times 50} = 1.27 \text{ } \mu\text{F}
\]
We therefore choose \( C_i = 2 \text{ } \mu\text{F} \).

We wish to note two additional points. The first is that if the common emitter amplifier uses voltage divider biasing instead of fixed biasing involving base resistors \( R_1 \) and \( R_2 \), then \( h_{ie} \) must be changed to \( h_{ie}//R_1//R_2 \) since these two resistors are generally within an order of magnitude of \( h_{ie} \). More generally, if \( Z_i \) is the input impedance of the amplifier, then it is easily shown that the formula for the lower cut-off frequency becomes

\[
(6.21)
\]
The second point is that if the signal source is driving the amplifier through a resistor $R_S$, then the voltage gain becomes

$$A_V(s) = -\frac{h_{fe}R_L sC_i}{1 + sC_i (R_S + h_{ie})} = -\frac{h_{fe}R_L}{R_S + h_{ie}} \frac{sC_i (R_S + h_{ie})}{1 + sC_i (R_S + h_{ie})}$$  \hspace{1cm} (6.22)

from which $f_L$ is given by

$$f_L = \frac{1}{2\pi (R_S + h_{ie}) C_i}$$  \hspace{1cm} (6.23)

and the mid-band gain becomes

$$A_V = -\frac{h_{fe}R_L}{R_S + h_{ie}}$$

### 6.1.2 Output Coupling Capacitor

Consider now the common emitter amplifier in Fig. 6.7 with output coupling capacitor $C_o$ connected to an external load $R_X$. In order to determine the effect of capacitor $C_o$ on the low-frequency response of the amplifier, $C_i$ is assumed to be very large.
From the $h$-parameter equivalent circuit shown in Fig. 6.8,

\[ V_i(s) = I_b h_{ie} \]  \hspace{1cm} (6.24)

\[ Z_i = h_{ie} || R_B . \]  \hspace{1cm} (6.25)

where

\[ I_o = -I_b h_{fe} \frac{R_L}{R_L + 1/sC_o + R_X} = -\frac{h_{fe} I_b sC_o R_L}{1 + sC_o (R_L + R_X)} \]  \hspace{1cm} (6.26)
Hence, the gain is given by

$$A_V = \frac{I_o R_X}{I_b h_{ie} h_{fe}} = -\frac{h_{fe} I_b s C_o R_L}{1 + s C_o (R_L + R_X)} \cdot \frac{R_X}{I_b h_{ie}} = -\frac{h_{fe} R_L}{h_{ie}} \cdot s C_o R_L$$

(6.27)

After manipulation, (6.27) becomes

$$A_V = -\frac{h_{fe} R_L}{h_{ie}} \cdot s C_o (R_L + R_X)$$

\[ \frac{1}{1 + s C_o (R_L + R_X)} \]

(6.28)

where \( R_L = R_L // R_X \). Thus the mid-frequency gain is \(-\frac{h_{fe} R_L}{h_{ie}}\) and the lower cut-off frequency \( f_L \) is given by

$$f_L = \frac{1}{2\pi (R_L + R_X) C_o}$$

(6.29)

If the output of the amplifier drives the input of a second amplifier with input impedance \( Z_i \) instead of an external load, then (6.29) becomes

$$f_L = \frac{1}{2\pi (R_L + Z_i) C_o}$$

(6.30)
6.1.3 Emitter Bypass Capacitor
The most effective biasing scheme used with the common emitter amplifier is the voltage divider biasing shown in Fig. 6.9. This circuit includes an input coupling capacitor $C_i$, an output coupling capacitor $C_o$, and a bypass capacitor $C_E$. The low-frequency effects of $C_i$ and $C_o$ have already been determined. In order to determine the effect of $C_E$, $C_i$, and $C_o$ are assumed to be very large, and therefore, can be replaced by short-circuits. Capacitor $C_E$ ensures that the emitter of the transistor is grounded for signal voltages. However, as the signal frequency falls, the reactance of $C_E$ increases, and this capacitor no longer represents a signal short-circuit.

![Fig. 6.9 Voltage divider-biased common emitter amplifier](image-url)
Consider the equivalent circuit shown in Fig. 6.10. Here

\[ V_i(s) = I_b h_{ie} + (1 + h_{fe}) R_E / \frac{1}{1 + s C_E} = h_{ie} I_b + (1 + h_{fe}) I_b \frac{R_E}{1 + s C_E R_E} \quad (6.31) \]

\[ I_1 = I_{R_1} = 0.7 / R_1 \quad (6.32) \]

**Fig. 6.10** Equivalent circuit including bypass capacitor

Therefore, the voltage gain is given by

\[ A_V(s) = -\frac{h_{fe} R_L}{h_{ie} + (1 + h_{fe}) \frac{R_E}{1 + s C_E R_E}} \quad (6.33) \]

After manipulation, this becomes

\[ A_V(s) = -\frac{h_{fe} R_L}{h_{ie} + (1 + h_{fe}) R_E} \frac{(1 + s C_E R_E)}{1 + \frac{s C_E R_E h_{ie}}{h_{ie} + (1 + h_{fe}) R_E}} \quad (6.34) \]

Noting that \( 1 + h_{fe} \approx h_{fe} \) and \( h_{ie} / h_{fe} = r_e \), then
In general, \( R_E \gg r_e \) and therefore \( R_E // r_e \approx r_e \). Hence (6.35) becomes

\[
A_V(s) = -\frac{R_L}{r_e} \frac{1 + s C_E R_E}{1 + s C_E R_E r_e}
\]

(6.36)

A frequency response plot of (6.36) is shown in Fig. 6.11.

![Frequency response plot showing the effect of CE](image)

**Fig. 6.11** Frequency response plot showing the effect of \( C_E \)

Note that the magnitude of the mid-frequency gain is \( R_L / r_e \) which starts to fall as frequency decreases at

\[
f_1 = \frac{1}{2\pi C_E r_e}
\]

(6.37)

However, at \( f_2 = \frac{1}{2\pi C_E R_E} \) the gain tends to \( \frac{R_L}{r_e} \). Since \( R_E \gg r_e \), then \( f_1 > f_2 \) and frequency \( f_L = f_1 \) approximately represents the lower cut-off frequency resulting from \( C_E \).
Example 6.2  Determine $C_E$ for the common emitter amplifier in Fig. 6.12 in order to produce a lower cut-off frequency of less than 50 Hz. Assume all coupling capacitors are large.

![Common emitter amplifier](image)

**Fig. 6.12**  Common emitter amplifier

**Solution**  \( f_L = \frac{1}{2\pi C_E r_e} \leq 50 \text{ Hz} \). Therefore \( C_E \geq \frac{1}{2\pi r_e 50} \). For this circuit, the voltage \( V_B \) at the base of the transistor is 

\[
V_B = \frac{26 \text{k}}{174 \text{k} + 26 \text{k}} \times 20 = 2.6 \text{ V}
\]

Hence the emitter voltage \( V_E = 2 \text{ V} \) giving

\[
I_C = \frac{2}{2 \text{k}} = 1 \text{ mA} \quad \text{and} \quad r_e = \frac{1}{40I_C} = \frac{1000}{40} = 25 \text{ Ω}.
\]

This gives

\[
C_E \geq \frac{1}{2\pi r_e 50} = \frac{1}{2 \times \pi \times 25 \times 50} = 127 \text{ μF}.
\]

Use \( C_E = 150 \text{ μF} \).

**Exercise 6.1**  For the case where the common emitter amplifier is driven through a source resistor \( R_S \), show that the frequency \( f_L \) becomes
In practice, in the voltage divider-biased common emitter amplifier, the coupling and bypass capacitors all influence the low-frequency response of the amplifier. In the determination of these capacitor values, one approach is to use $C_E$ to set $f_L$, $C_E$ being the largest of the capacitors, and select $C_i$ and $C_o$ sufficiently large such that the associated cut-off frequencies are well below that created by $C_E$.

**Example 6.3** Determine the capacitors $C_i$, $C_E$, and $C_o$ in the circuit of Fig. 6.13. To give $f_L = 50$ Hz. Assume $h_{fe} = 100$.

**Solution** For this circuit, $I_C = 1$ mA and hence $r_e = 25$ Ω and $h_{ie} = 2.5$ k. Using (6.21),

$$C_i = \frac{1}{2\pi Z_i \times 50},$$

where $Z_i = R_1//R_2//h_{ie} = 26 \text{k}//174 \text{k}//2.5 \text{k} = 2.25 \text{k}$. Hence

$$C_i = \frac{1}{2\pi \times 2.25 \text{k} \times 50} = 1.4 \text{ µF}.$$
Finally using (6.37),

\[ C_o = \frac{1}{2\pi(9.12 \text{ k})_{50}} = 0.15 \ \mu\text{F}. \]
\[ C_E = \frac{1}{2\pi \times 25 \times 50} = 127 \ \mu\text{F}. \]

Since \( C_E \) is the largest capacitor, we use this to determine the lower cut-off frequency and choose it to be \( C_E = 150 \ \mu\text{F}. \)

We then select the other two capacitors to be about ten times the calculated values so that the resulting cut-off frequencies are well below \( f_L = 50 \ \text{Hz}. \) Hence \( C_i = 15 \ \mu\text{F} \) and \( C_o = 2 \ \mu\text{F}. \)

### 6.2 FET Low-Frequency Response

The determination of the coupling and bypass capacitors in a common source FET amplifier is similar to the common emitter BJT amplifier. Consider the common source JFET amplifier shown in Fig. 6.14. Similar to the BJT, the lower cut-off frequency set by \( C_i \) is given by

\[ f_L = \frac{1}{2\pi R_G C_i} \]  

(6.38)

where \( R_G \) replaces \( h_{ie} \) and again \( C_i \) and \( R_G \) together form a high-pass filter. Similarly, the lower cut-off frequency created by the output coupling capacitor \( C_o \) is given by

\[ f_L = \frac{1}{2\pi (R_L + R_X) C_o} \]  

(6.39)
In order to determine the bypass capacitor $C_S$, the equivalent circuit shown in Fig. 6.15 needs to be analyzed. Thus

$$V_i = V_{GS} + g_m V_{GS} R_S / \left[ 1 / s C_S \right] = V_{GS} + g_m V_{GS} \frac{R_S}{1 + s C_S R_S}$$  \hspace{1cm} (6.40)$$

$$A_{V1} = -40 I_{C1} R_1 \parallel h_{ie2}$$  \hspace{1cm} (6.41)$$
Fig. 6.15 Equivalent circuit of common source JFET amplifier

Therefore

\[ A_V(s) = \frac{g_m R_L/\parallel R_X}{1 + g_m R_S/(1 + sC_S R_S)} \]  \quad (6.42)

After manipulation, this becomes

\[ A_V(s) = \frac{g_m R_L/\parallel R_X}{1 + g_m R_S} \cdot \frac{1 + sC_S R_S}{1 + sC_S R_S/(1 + g_m R_S)} \]  \quad (6.43)

Thus, at low frequencies

\[ A_V \rightarrow -g_m R_L/\parallel R_X. \]

From (6.43), there is a pole at

\[ f_L = \frac{1 + g_m R_S}{2\pi R_S C_S} \]  \quad (6.44)

and a zero at \( f_2 = \frac{1}{2\pi R_S C_S} \). Since \( f_L > f_2 \), the lower cut-off frequency is determined by \( f_L \). The frequency response plot is shown in Fig. 6.16.
6.3 Hybrid-Pi Equivalent Circuit

The most widely used model for transistor high-frequency behavior is the hybrid-pi equivalent circuit shown in Fig. 6.17. This model was first published by L.J. Giaceletto in the RCA Review of 1954. The resistor \( r_{bb'} \) is the ohmic base resistance, \( r_{cb'} \) is the collector-base resistor which is quite large (several megohms), while capacitors \( C_{b'e} \) and \( C_{b'c} \) are the emitter-base and collector-base junction capacitors, respectively.
At low frequencies, since $r_{bb'}$ is small and $r_{cb'}$ is large, the hybrid-pi equivalent circuit becomes that shown in Fig. 6.18. This is very similar to the $h$-parameter low-frequency equivalent circuit of Chap. 4 where

$$h_{ie} = r_{bb'} + r_{b'e}$$  \hspace{1cm} (6.45)$$

$$1/h_{oe} = r_{ce}$$  \hspace{1cm} (6.46)$$

and

$$g_m V_{b'e} = h_{fe} i_b$$  \hspace{1cm} (6.47)$$
The effect of eliminating $r_{cb'}$ in the hybrid-pi equivalent circuit is essentially the same as neglecting $h_{re}$ in the $h$-parameter equivalent circuit.

In the hybrid-pi equivalent circuit, the resistance $r_{cb'}$ is usually neglected giving the equivalent circuit in Fig. 6.19 where resistor $R_L$ is the usual collector resistor. The capacitance $C_{b'c}$ is the capacitance between the collector-base junction of the transistor. The reverse bias on this junction creates a depletion region at the junction with charges at the boundaries of the region. The effect is that of a capacitor whose value varies with the magnitude of the reverse bias $V_{cb}$ at the junction. $C_{b'c}$ varies between 0.8 and 50 pF. The capacitance $C_{b'c}$ is the capacitance between the base-emitter junction. This capacitance arises as a result of a mechanism referred to as diffusion capacitance. This phenomenon occurs because of time delay during the diffusion of majority carriers from the emitter of the transistor to the base region. This delay mechanism limits the rate at which the carriers can move between the emitter and base regions and constitutes a capacitance. Its value depends on the emitter DC current $I_E$, increasing with this current as charge increases. $C_{b'c}$ ranges between approximately 20 pF and
0.01 μF. Its value is typically 100 times greater than $C_{be}$. The simplified hybrid-pi circuit of Fig. 6.19 is used to examine the high-frequency behavior of the transistor.

![Fig. 6.19 Simplified BJT hybrid-pi equivalent circuit](image)

### 6.3.1 Single Pole Transfer Function

In discussing the high-frequency response of single-stage transistor amplifiers, the voltage gain expressions $A_V = V_o/V_S$ will often reduce to a transfer function of the form

$$A_V(j\omega) = \frac{k}{1 + jf/f_o} \quad (6.48)$$

where $k$ is the low-frequency gain of the amplifier stage and $f_o$ is the frequency of the pole. In order to represent this transfer function on a frequency response plot, we express the magnitude in decibels given by

$$|A|_{\text{dB}} = 20 \log |A| = 20 \log k - 20 \log |1 + jf/f_o| \quad (6.49)$$

This reduces to

$$|A|_{\text{dB}} = 20 \log k, f \ll f_o \quad (6.50)$$

$$|A|_{\text{dB}} = 20 \log k, f \ll f_o \quad (6.51)$$
Using these equations, $|A|_{DB}$ is plotted against $\log f$. For frequencies $f$ well below the pole frequency such that $f \ll f_o$, the response approaches the horizontal line $|A|_{DB} = 20 \log k$. For frequencies well above the pole frequency such that $f \gg f_o$, the response approaches the line whose slope is $-20$ dB/decade. These lines are shown in Fig. 6.20. Note that at $f = f_o$, both lines intersect since they both have the same magnitude value $|A|_{DB} = 20 \log k$. For the transfer function, at $f = f_o$,

$$|A| = \frac{k}{\sqrt{1 + (f/f_o)^2}} = \frac{k}{\sqrt{1 + 1}} = k/\sqrt{2} = 0.707 \times k$$

(6.52)

**Fig. 6.20** Frequency response plot of single-stage amplifier

Hence

(6.53)
Thus at the pole frequency, the magnitude of the transfer function drops to 0.707 of its low-frequency value \( k \), i.e., by 3 dB as shown in Fig. 6.20.

Consider now the short-circuit current gain \( \beta \), which is defined as

\[
\beta(j\omega) = \frac{I_c}{I_b}
\]

(6.54)

This parameter is actually frequency-dependent and its value can be found using the hybrid-pi equivalent circuit. Shorting the collector and emitter yields the equivalent circuit of Fig. 6.21 where \( C_{b'c} \) is now placed in parallel with \( C_{b'c} \):

\[|A|_{dB} = 20 \log |A| = 20 \log k - 20 \log \sqrt{2} = 20 \log k - 3\]

\[
V_{GS} = I_i R_B 
\]

(6.55)

\[
I_b = \frac{V_{b'e}}{Z_{b'e}} 
\]

(6.56)

where

(6.57)
\[ Z_{b'e} = r_{b'e} \left( \frac{1}{s(C_{b'e} + C_{b'c})} \right) = \frac{r_{b'e}}{1 + sr_{b'e}(C_{b'e} + C_{b'c})} \]

Hence

\[ \beta(j\omega) = g_m Z_{b'e} = \frac{g_m r_{b'e}}{1 + sr_{b'e}(C_{b'e} + C_{b'c})} = \frac{\beta_o}{1 + jf/f_\beta} \quad (6.58) \]

where

\[ \beta_o = g_m r_{b'e} \approx h_{fe} \quad (6.59) \]

and

\[ f_\beta = \frac{1}{2\pi r_{b'e}(C_{b'e} + C_{b'c})} \quad (6.60) \]

Equation (6.58) is of the single pole form (6.48). The quantity \( \beta_o \) is referred to as the low-frequency beta or \( h_{fe} \) that we have used in our BJT \( h \)-parameter analysis. Also, \( f_\beta \) is called the beta cut-off frequency. It is that frequency at which the magnitude of \( \beta \) falls to 3 dB down from the low-frequency value \( \beta_o \). From (6.58), the frequency \( f_T \) at which \( \beta \) goes to unity is given by

\[ 1 = \frac{\beta_o f_\beta}{jf_T}, \quad f \gg f_\beta \quad (6.61) \]

Hence

\[ |1| = \left| \frac{\beta_o f_\beta}{jf_T} \right| = \beta_o \frac{f_\beta}{f_T} \quad (6.62) \]

giving

\[ f_T = \beta_o f_\beta \quad (6.63) \]

or

\[ f_T = \frac{\beta_o}{2\pi r_{b'e}(C_{b'e} + C_{b'c})} \quad (6.64) \]
The frequency $f_T$ is called the transition frequency or gain-bandwidth product of the transistor. Figure 6.22 illustrates $f_\beta$ and $f_T$.

![Diagram of frequency response plot of the magnitude of $\beta$](image)

*Fig. 6.22* Frequency response plot of the magnitude of $\beta$

Since $C_{b'e} \gg C_{b'e}$, (6.64) becomes

$$f_T = \frac{\beta_o}{2\pi r_{b'e} C_{b'e}} \quad (6.65)$$

But

$$r_{b'e} \approx h_{ie} = \frac{h_{fe}}{40I_c} = \beta_o r_e \quad (6.66)$$

where

$$r_e = \frac{1}{40I_c} \quad (6.67)$$

giving

$$f_T = \frac{1}{2\pi r_e C_{b'e}} \quad (6.68)$$

$f_T$ varies with collector current $I_C$ as shown in Fig. 6.23.
Example 6.4 A silicon npn transistor has $f_T = 400 \text{ MHz}$. Calculate $C_{b'e}$ for $I_C = 1 \text{ mA}$.

Solution

\[ r_e = \frac{1}{40I_c} = \frac{10^3}{40} = 25 \text{ } \Omega \]

Hence, \[ f_T = \frac{1}{2\pi 25 C_{b'e}} \]

\[ C_{b'e} = \frac{1}{2\pi \times 25 \times 400 \times 10^6} = 15.9 \text{ } \text{pF} \]

6.4 Miller Effect

In order to analyze the common emitter amplifier using the hybrid-pi equivalent circuit, a new theorem is introduced that helps to further simplify the equivalent circuit. Consider the basic amplifier shown in Fig. 6.24 in which feedback admittance $Y_f$ is connected from output to input.
The amplifier is driven by a voltage source $V_S$ in series with a source $R_S$ and has a voltage gain $A_V = V_o/V_i$. The input admittance of the basic amplifier given by

$$Y_a = I_a/V_i$$ (6.69)

while the output admittance is

$$Y_b = -I_b/V_o$$ (6.70)

With $Y_f$ connected, the resulting input admittance $Y_{in}$ becomes

$$Y_{in} = I_i/V_i$$ (6.71)

and the resulting output admittance $Y_{out}$ is given by

$$Y_{out} = -I_o/V_o$$ (6.72)

From (6.71),

$$Y_{in} = \frac{I_i}{V_i} = \frac{I_f + I_a}{V_i}$$ (6.73)

But

$$I_f = (V_i - V_o) Y_f$$ (6.74)

Therefore,

$$Y_{in} = \frac{(V_i - V_o) Y_f + I_a}{V_i} = Y_a + (1 - A_V) Y_f$$ (6.75)
Based on \((6.75)\), the input admittance \(Y_{in}\) seen at the amplifier input is the input admittance \(Y_a\) of the basic amplifier in parallel with an admittance whose value is that of the feedback admittance multiplied by the factor \((1 - A_V)\). If the amplifier is inverting, then \(A_V \rightarrow -A_V\) and the multiplying factor \((1 - A_V)\) becomes \((1 + A_V)\).

At the output of the amplifier, we have

\[
Y_{out} = -\frac{I_o}{V_o} = -\frac{I_f + I_b}{V_o}
\]  

(6.76)

Substituting for \(I_f\) using \((6.74)\) gives

\[
Y_{out} = -\left[\frac{(V_i - V_o) Y_f + I_b}{V_o}\right] = Y_b + Y_f \left(1 - \frac{1}{A_V}\right) \approx Y_b + Y_f, |A_V| \gg 1
\]  

(6.77)

Thus, the output admittance \(Y_{out}\) of the amplifier with feedback \(Y_f\) is the sum of the basic admittance \(Y_b\) and the admittance \(Y_f\) of the feedback admittance providing the magnitude of the gain of the amplifier is significantly greater than unity. Results \((6.75)\) and \((6.77)\) constitute Miller’s theorem. Based on this theorem, the amplifier circuit of Fig. 6.24 can be redrawn in the equivalent form of Fig. 6.25 in which the feedback admittance \(Y_f\) is replaced by an admittance \(Y_f(1 - A_V)\) at the input and an admittance \(Y_f(1 - A_V)\) at the output. This result enables a more simplified analysis of the original amplifier.

![Fig. 6.25 Equivalent amplifier circuit](image)
6.5 Common Emitter Amplifier

The results that have been derived will now be used to analyze the circuit of the common emitter amplifier shown in Fig. 6.26.

The hybrid-pi equivalent circuit is shown in Fig. 6.27 in which the collector-emitter resistor \( r_{ce} = 1/h_{oe} \) is assumed to be very large compared with \( R_L \) and therefore has been omitted. Since \( C_{b'c} \) is connected between \( b \) and \( c \) in order to apply Miller’s Theorem, we determine the voltage gain \( A_V \) between \( b \) and \( c \) given by

\[
A_V = \frac{V_o}{V_{b'c}}
\]

(6.78)
Now

\[ V_o = -g_m V_{b'e} R'_L \]  \hspace{1cm} (6.79)

where \( R'_L \) is \( R_L \) including the effect of \( C_{cb'} \). Therefore

\[ A_V = \frac{-g_m V_{b'e} R'_L}{V_{b'e}} = -g_m R'_L \]  \hspace{1cm} (6.80)

Since the feedback admittance \( Y_f \) is

\[ V_i(s) = I_b h_{ie} \]  \hspace{1cm} (6.81)

using Miller’s Theorem, \( Y_f \) across the collector-base junction can be replaced by \( Y_f (1 - A_V) \) at the input and \( Y_f (1 - 1/A_V) \) at the output. At the input,

\[ Y_f (1 - A_V) = j \omega C_{cb'} (1 + g_m R'_L) \]  \hspace{1cm} (6.82)

which is equivalent to a capacitance \( C_{M'} \) given by

\[ C_{M'} = C_{cb'} (1 + g_m R'_L) \]  \hspace{1cm} (6.83)

At the output,

\[ Y_f (1 - 1/A_V) = j \omega C_{cb'} (1 + 1/g_m R'_L) \approx j \omega C_{cb'}, \text{ } g_m R'_L \gg 1 \]  \hspace{1cm} (6.84)
which is equivalent to a capacitance $C_{b'e}$ at the output. The capacitance $C_{M'}$ at the input is called the Miller capacitance and the resulting equivalent circuit is shown in Fig. 6.28.

![Equivalent circuit after application of Miller's theorem](image)

**Fig. 6.28** Equivalent circuit after application of Miller's theorem

Because of the multiplying effect of the $(1 + g_m R'_L)$ factor, its value is comparable to $C_{b'e}$ between the base-emitter junction.

Evaluating the transfer function $V_o/V_b$ for the amplifier,

$$V_o = -g_m V_{b'e} R'_L$$ \hfill (6.85)

where

$$R'_L = R_L / (1/sC_{b'e})$$ \hfill (6.86)

$$V_{b'e} = \frac{r_{b'e}/(1/sC_{M})}{r_{b'b} + r_{b'e}/(1/sC_{M})} V_b$$ \hfill (6.87)

where

$$C_{M} = C_{M'} + C_{b'e}$$ \hfill (6.88)

Hence

$$\text{(6.89)}$$
The circuit to the left of \( b \) involving the source voltage \( V_S \), as well as \( R_S, R_A, \) and \( R_B \), can be replaced by the Thevenin equivalent \( V_G \) in series with \( R_G \) as shown in Fig. 6.29 where

\[
R_G = \frac{R_1}{R_2} R_S
\]  
(6.90)

and

\[
V_G = \frac{R_1}{R_S + \frac{R_1}{R_2}} V_S
\]  
(6.91)

---

**Fig. 6.29** Equivalent circuit with simplified source

Thus, \( R_G \) can be treated as part of \( r_{bb'} \) giving

\[
\frac{V_o}{V_G} = -g_m R_L' \frac{r_{bb'} e}{1 + sC_M (r_{bb'} + R_G + r_{bb'})}
\]  
(6.92)

Substituting for \( V_G \) in (6.92) gives

\[
\frac{V_o}{V_G} = -g_m R_L' \frac{r_{bb'} e}{1 + sC_M r_{bb'} e}
\]  
(6.93)
where

\[
\rho = \frac{R_A/\parallel R_B}{R_S + R_A/\parallel R_B}
\]  \hspace{1cm} (6.94)

From (6.42),

\[
R_L' = \frac{R_L}{1/sC_{cb'}} = \frac{R_L}{1 + sR_LC_{cb'}}
\]  \hspace{1cm} (6.95)

If \(C_{cb'}\) is small, then the pole created by \(R_LC_{cb'}\) is at a high frequency and can be ignored, in which case \(R_L' \rightarrow R_L\) in (6.95).

Thus from (6.93), transfer function \(V_o/V_S\) for the common emitter amplifier can be written as

\[
\frac{V_o}{V_S} = \frac{k}{1 + jf/f_o}
\]

where the low-frequency gain \(k\) of the amplifier is given by

\[
k = g_mR_L\rho\frac{r_{b'e}}{r_{bb'} + R_G + r_{b'e}}
\]  \hspace{1cm} (6.96)

and the cut-off frequency \(f_o\) is given by

\[
f_o = \frac{1}{2\pi C_M(r_{bb'} + R_G)//r_{b'e}}
\]  \hspace{1cm} (6.97)

A frequency response plot for the amplifier is shown in Fig. 6.30. \(f_o\) is the upper cut-off frequency of the amplifier. It is the frequency at which the gain of the amplifier falls by 3 dB below its low-frequency value. If the attenuation factor \(\rho\) is ignored and \(R_G\) set to zero, the low-frequency gain \(k\) in (6.96) becomes
the value obtained in Chap. 2.

From (6.97), the frequency response of the amplifier can be increased by reducing the source resistance $R_S$. Thus if $R_S = 0$ corresponding to a voltage source, then $f_o$ becomes

$$f_o' = \frac{1}{2\pi C_M r_{bb'} / r_{b'e}} \approx \frac{1}{2\pi C_M r_{bb'}} > f_o, r_{bb'} \ll r_{b'e}$$ (6.99)

If however $R_S$ is very large corresponding to a current source, then for $R_S > R_1 / R_2, f_o$ becomes

$$f_o'' = \frac{1}{2\pi C_M (r_{bb'} + R_1 / R_2) / r_{b'e}} \approx \frac{1}{2\pi C_M R_1 / R_2} < f_o, r_{bb'} \ll R_1 / R_2$$ (6.100)

The cut-off frequency is also influenced by the gain $g_m R_L$ of the amplifier since $C_M' \approx C_{cb'} g_m R_L$. If the gain is reduced by reducing $R_L$, the cut-off frequency is increased. A large transition frequency $f_T$ reduces $C_{b'e}$ in (6.68) and therefore also improves the frequency response of the amplifier. Finally, a small $C_{cb'}$ also improves the frequency response by decreasing the Miller capacitance $C_M$. 

![Frequency response plot of the common emitter amplifier](image)
Thus, in order to realize a high cut-off frequency \( f_o \) in the amplifier design, the following steps can be taken:

- Use a low source impedance, i.e., voltage-drive the amplifier.
- Use a low load resistance \( R_L \).
- Use a transistor with a large \( f_T \).
- Use a transistor with a low \( C_{cb'} \).

**Example 6.5** Determine the upper cut-off frequency for the common emitter amplifier shown in Fig. 6.31 where a 2N3904 transistor is used.

![Common emitter amplifier](image)

**Solution** The 2N3904 has \( f_T = 270 \) MHz, \( C_{cb'} = 4 \) pF, and \( \beta_o = 100 \).

The quiescent current for this circuit is easily determined to be 1 mA. Then \( r_{cb'} \) is given by \( r_{cb'} = \beta_o r_e = \frac{100}{40 \times 1 \text{ mA}} = 2.5 \text{ k} \). The capacitance \( C_{b'e} \) can be found from \( V_{oc} = -h_f e I_b R_L \), giving
\[ C_{b'e} = \frac{1}{2\pi f_T r_e} = \frac{1}{2\pi \times 270 \times 10^6 \times 25} = 23.6 \text{ pF}. \text{ } r_{bb'} \text{ is assumed to be about 20 } \Omega. \text{ From (6.88),} \]
\[ C_M = C_{b'e} + C_{cb'} (1 + g_m R_L) = 23.6 \text{ pF} + (1 + 40 \times 1 \text{ mA} \times 9 \text{ k}) 4 \text{ pF} = 1468 \text{ pF}. \]
From (6.90), \[ R_G = R_A \parallel R_B \parallel R_S = 27 \text{ k} \parallel 173 \text{ k} \parallel 600 \approx 600 \Omega. \text{ Hence from (6.97),} \]
\[ f_o = \frac{1}{2\pi C_M (r_{bb'} + R_G) \parallel r_{b'e}} = \frac{1}{2\pi \times 1468 \text{ pF} \times (20 + 600) \parallel 2500} = 218, 140 \text{ Hz}. \]

### 6.6 Common Emitter Amplifier with Local Series Feedback

The circuit of Fig. 6.32 shows a common emitter amplifier with only a partially decoupled emitter resistor. The resistor \( R_e \) appears in series with the emitter terminal. In order to evaluate the effect of the resistor on the frequency response of the stage, the transistor is again replaced by the simplified hybrid-pi equivalent circuit shown in Fig. 6.33. The circuit can be further simplified by replacing the dependent current source \( g_m V_{b'e} \) by two such sources as shown in Fig. 6.34. The voltage \( V_{b'} \) at base terminal \( b' \) with respect to ground is given by

\[ V_{b'} = V_{b'e} + (I_{b'} + g_m V_{b'e}) R_e \]  

\[ \text{(6.101)} \]
Fig. 6.32 Common emitter amplifier with partially bypassed emitter resistor
**Fig. 6.33** Equivalent circuit of amplifier in Fig. 6.32

**Fig. 6.34** Simplified equivalent circuit

Now

\[ I_{b'} = \frac{V_{b'e}}{Z_{b'e}} \]  \hspace{1cm} (6.102)

where

\[ Z_{b'e} = \frac{r_{b'e}}{1/sC_{b'e}} \]  \hspace{1cm} (6.103)

Therefore

\[ V_{b'} = V_{b'e} + (V_{b'e}/Z_{b'e} + g_m V_{b'e}) R_e = V_{b'e} \{1 + R_e (g_m + y_{b'e})\} \]  \hspace{1cm} (6.104)

where

\[ y_{b'e} = \frac{1}{Z_{b'e}} = \frac{1}{r_{b'e}} + sC_{b'e} \]  \hspace{1cm} (6.105)

Using (6.104) and (6.102), we get

\[ \frac{V_{b'}}{I_{b'}} = \{1 + R_e (g_m + y_{b'e})\} Z_{b'e} = \frac{1 + R_e (g_m + y_{b'e})}{y_{b'e}} \]  \hspace{1cm} (6.106)

Equation (6.106) represents the effective impedance between \( b' \) and ground. Hence, the components \( r_{cb'}, C_{b'e}, R_e, \) and \( g_m V_{b'e} \) can all be
replaced by an admittance $y_{b'}$ of value

$$y_{b'} = \frac{y_{b'e}}{1 + R_e (g_m + y_{b'e})}$$  \hspace{1cm} (6.107)

The voltage gain $A_V$ between $b'$ and $c$ is given by

$$A_V = \frac{V_o}{V_{b'}} = \frac{-g_m V_{b'e} R_L}{V_{b'e} [1 + R_e (g_m + y_{b'e})]} = \frac{-g_m R_L}{1 + R_e (g_m + y_{b'e})}$$  \hspace{1cm} (6.108)

Therefore, using Miller’s theorem, the capacitor $C_{b'c}$ between $b'$ and $c$ can be replaced by $C_M$ across $b'$ and ground where

$$C_M = \frac{g_m R_L}{1 + R_e (g_m + y_{b'e})} C_{b'c}$$  \hspace{1cm} (6.109)

and a capacitor $C_{b'c}$ across $c$ and ground. Also, from (6.104)

$$V_{b'e} = \frac{V_{b'}}{1 + R_e (g_m + y_{b'e})}$$  \hspace{1cm} (6.110)

The resulting equivalent circuit is shown in Fig. 6.35.

![Equivalent circuit of amplifier](image)

**Fig. 6.35** Equivalent circuit of amplifier in Fig. 6.32

The transfer function $V_o/V_S$ is given by

$$\frac{V_o}{V_S}$$  \hspace{1cm} (6.111)
\[
\frac{V_o}{V_S} = \frac{-g_mR_L}{1 + R_e (g_m + y_{b'e}) + (R_S + r_{bb'}) (y_{b'e} + sC_{b'e}g_mR_L)}
\]

Substituting for \( y_{b'e} \) using (6.105), (6.111) becomes

\[
\frac{V_o}{V_S} = \frac{k}{1 + jf/f_o}
\]

(6.112)

where

\[
k = \frac{g_mR_Lr_{b'e}}{R_S + r_{bb'} + r_{b'e} + R_e (1 + g_m r_{b'e})}
\]

(6.113)

and

\[
f_o = \frac{1}{2\pi C_{b'e}r_{b'e} (R_e + \alpha) / [R_S + r_{bb'} + r_{b'e} (1 + g_mR_e)]}
\]

(6.114)

with

\[
\alpha = (R_S + r_{bb'}) (1 + g_mR_LC_{b'e} / C_{b'e})
\]

(6.115)

From (6.114), for \( R_e \ll \alpha \), as \( R_e \) increases, \( f_o \) increases as shown in Fig. 6.36. Also, the gain-bandwidth product \( kf_o \) is

\[
kf_o = \frac{g_mR_Lr_{b'e}}{2\pi C_{b'e}r_{b'e} (R_e + \alpha)} = \frac{g_mR_L}{2\pi [R_eC_{b'e} + (R_S + r_{bb'}) (C_{b'e} + C_{b'e}g_mR_L)]}
\]

(6.116)
This product is maximum for $R_S = 0$, and therefore this stage is best driven from a voltage source.

### 6.7 Common Emitter Amplifier with Local Shunt Feedback

The circuit of Fig. 6.37 shows a common emitter amplifier with a resistor connecting collector and base and driven by a current source $I_S$ of internal resistance $R_S$. The equivalent circuit is shown in Fig. 6.38, and in this case, it is the trans-resistance $V_o/I_S$ that is investigated. Under several reasonable conditions including $I_C = \beta_D I_B$ and $C_{b'e} \gg C_{b'c}$, this transfer function is found to be

$$\frac{V_o}{I_S} = \frac{R_m}{1 + jf/f_o} \quad (6.117)$$

where

$$R_m = \frac{g_m r_{b'e} R_S R_F R_L}{(R_S + r_{bb'} + r_{b'e})(R_F + R_L) + g_m r_{b'e} R_S R_L} \quad (6.118)$$
and

\[ f_o = \frac{1}{2\pi r_{be} \left( r_{be} + r_{be}' \right) \left( R_F + R_L + g_m R_L r_{be}' R_S \right) \left[ C_{be} (R_F + R_L) + C_{be}' g_m R_L R_F \right]} \]  \quad (6.119)

**Fig. 6.37** Common emitter amplifier with local shunt feedback
This reduces to

\[
f_o = \frac{1}{2\pi r_{bb'}e(r_{bb'}+r_S) + g_m R_L R_F} \left[ C_{b'e} + C_{b'c} g_m R_L / R_F \right]
\]

Reducing \( R_F \) corresponds to increasing feedback. Eventually \( R_F \ll R_L \) and \( f_o \) becomes

\[
f_o = \frac{1}{2\pi r_{bb'}e(r_{bb'}+r_S) + g_m R_F} \left[ C_{b'e} + C_{b'c} g_m R_F \right]
\]

From (6.121), \( f_o \) increases as \( R_F \) is reduced, i.e. the bandwidth increases with increased feedback as shown in Fig. 6.39. It is convenient to identify the current gain \( A_I = I_L/I_S \) for the circuit which is easily obtained by dividing \( V_o/I_S \) by the load resistor \( R_L \). Thus, the current gain-bandwidth product \( A_I f_o \) for this circuit is given by

\[
A_I f_o = \frac{g_m R_S R_F}{(r_{bb'} + R_S) \left[ C_{b'e} (R_F + R_L) + C_{b'c} g_m R_F R_L \right]}
\]
which is a maximum when $R_S \to \infty$. That is, the common emitter amplifier with local shunt feedback is best driven from a current source in order to improve the frequency response characteristics.

![Graph]

**Fig. 6.39** Effect of local shunt feedback on bandwidth

### 6.8 High-Frequency Response of the Cascode Amplifier

Another method of improving the frequency response of the common emitter amplifier is to operate the configuration as a Cascode amplifier shown in a simplified form in Fig. 6.40 with equivalent circuits in Figs. 6.41 and 6.42. The configuration consists essentially of a common emitter amplifier $Tr_1$ operating in a common base amplifier $Tr_2$. The input of $Tr_2$ is the load of $Tr_1$. The Miller capacitance $C'_M$ arising from $C_{cb'1}$ is given by

$$C'_M = (1 + g_mR_L)C_{cb'1}$$  \hspace{1cm} (6.123)
Fig. 6.40 Cascode amplifier

Fig. 6.41 Equivalent circuit of Cascode amplifier
Since $R_{L1}$ is the input impedance $r_{e2}$ of $Tr_2$, its value is given by $R_{L1} = r_{e2}$. Because of the high frequency response of the common base amplifier compared with the common emitter amplifier, the frequency effect associated with $r_{e2}$ can be ignored. The DC collector current of $Tr_1$ is approximately that of $Tr_2$. Therefore

$$g_{m1} \approx 1/r_{e2}$$  \hspace{1cm} (6.124)$$

and hence the gain of the common emitter stage is unity. Hence

$$C'_M = (1 + 1)C_{cb1} = 2C_{cb'1}$$  \hspace{1cm} (6.125)$$

and the total effective capacitance $C'_M$ between $b_1$ and $e_1$ is

$$C'_M = C_{b'e1} + C_{cb'1}$$  \hspace{1cm} (6.126)$$

The upper cut-off frequency therefore becomes

$$\bar{f}_o = \frac{1}{2\pi C'_M (R_S + r_{b'b})/r_{b'e}} > f_o = \frac{1}{2\pi C_M (R_S + r_{b'b})/r_{b'e}}$$  \hspace{1cm} (6.127)$$

since $C'_M < C_M$. That is, the cut-off frequency of the common emitter stage of the Cascode amplifier is higher than that of the normal common emitter amplifier because the voltage gain of the common emitter stage in the Cascode circuit is unity, and therefore, there is no multiplication of the collector-base junction capacitor; the value of $C'_M$ is significantly reduced.
Now
\[ V_o = -g_{m2} V_{b'e2} R_L' \]  
(6.128)

Therefore
\[
\frac{V_o}{V_S} = \frac{V_o}{V_{e2b2}} \frac{V_{c1e1}}{V_S} = \frac{-r_{b'e}}{r_{bb'} + R_S + r_{b'e}} \frac{g_m R_L}{1 + sC_M (r_{bb'} + R_S) / / r_{b'e} (1 + sC_{cb2} R_L)}
\]  
(6.129)

which has the same low-frequency voltage gain expression as the common emitter amplifier but a higher cut-off frequency.

6.9 High-Frequency Response of the Common Base Amplifier

In the common emitter amplifier, the base-emitter input capacitance along with the Miller capacitance serve to limit the high frequency response of the amplifier. In the common base amplifier of Fig. 6.43 now under consideration, the absence of any significant capacitance between the collector and the emitter of the transistor means that the Miller effect in this configuration is negligible. A higher frequency response is therefore expected.
The hybrid-pi equivalent circuit for this configuration is shown in Fig. 6.44. Since $r_{bb'}$ is small compared with the adjacent circuit components, a further simplification of the equivalent circuit is its removal such that $b'$ is connected directly to ground. Thus the capacitance $C_{b'e}$ only appears across the output load $R_L$, and there is no Miller effect. To simplify the analysis, the voltage sources $V_S$ is converted to a current source $V_S/R_S$. This simplified equivalent circuit is shown in Fig. 6.45.
Thus,

\[ V_o = -g_m R_L / (1/sC_{b'e} V_{b'e}) = \frac{-g_m R_L}{1 + sC_{b'e} R_L} V_{b'e} \]  \hspace{1cm} (6.130)

\[ (6.131) \]
From this,
\[
V_{b'e} = -\left( g_m V_{b'e} + V_S/R_S \right) \frac{1}{\left( \frac{1}{R_S} + \frac{1}{r_{b'e}} + sC_{b'e} \right)} \left( \frac{r_{b'e}}{R_S r_{b'e} C_{b'e}} \right)
\]
\[
= -\left( g_m V_{b'e} + V_S/R_S \right) \frac{r_{b'e}}{r_{b'e} + R_S + sR_S r_{b'e} C_{b'e}} \tag{6.132}
\]

where
\[
I_{b'h_{ie}} = I_x R_B \tag{6.134}
\]
and
\[
Z_L = R_L/\sqrt{1/sC_{b'e}} \tag{6.135}
\]

Dividing the numerator and denominator in (6.133) by \((1 + h_{fe})\) yields
\[
\frac{V_o}{V_S} = \frac{Z_L}{r_{e+R_S}} = \frac{R_L}{r_{e+R_S}} \frac{R_S r_{e} \left( R_S r_{e} \right)}{R_S + r_{e}} \left[ 1 + sC_{b'e} \left( R_S r_{e} \right) \right] \left( 1 + sC_{b'e} R_L \right) \tag{6.136}
\]

For a transistor with small \(C_{b'e}\) and \(R_L\), the upper cut-off frequency of the common base amplifier is
\[
f_H = \frac{1}{2\pi C_{b'e} R_S/\parallel r_{e}} \tag{6.137}
\]

The transition frequency \(f_T\) of a transistor is given by
\[
f_T = \frac{1}{2\pi r_e C_{b'e}} \tag{6.138}
\]
and therefore \(f_H > f_T\). However, in practice, the second pole of (6.136) corresponding to the cut-off frequency
sets the upper cut-off frequency with $f'_H < f_H, f_T$. Thus, the frequency response of the common base amplifier can be of the order of $f_T$ and therefore much higher than the frequency response of the common emitter amplifier. However, the low input impedance of the common base amplifier limits its applicability.

**Example 6.6** Determine the upper cut-off frequency for the common base amplifier shown in Fig. 6.46 where a 2N3904 transistor is used.

![Common base amplifier diagram]

**Solution** The transistor is again the 2N3904, and it is biased at 1 mA. Therefore the characteristics are the same as in Example 6.5, i.e., $I_{cq} = 1$ mA, $f_T = 270$ MHz, $C_{cb'} = 4$ pF, $C_{b'e} = 23.6$ pF, $r_{b'e} = 2.5$ kΩ, and $r_e = 1/40I_c = 25$ Ω. Hence, using (6.139), the upper cut-off frequency is given by

$$f'_H = \frac{1}{2\pi C_{b'e} R_L} = \frac{1}{2\pi \times 4 \times 10^{-12} \times 9000} = 4.4 \text{ MHz}.$$  

Note that the pole frequency given by (6.138) is
The common collector amplifer or emitter follower also has a better frequency response than the common emitter amplifer. In this section we analyze the performance of this configuration. The basic circuit is shown in Fig. 6.47 where biasing components are omitted for simplicity. Using the hybrid-pi equivalent circuit, the emitter follower can be represented as shown in Fig. 6.48. From this,

\[ V_o = \left( g_m V_{be} + \frac{V_{be}}{r_{be}/1/sC_{be}} \right) R_E = V_{be} \left( g_m + \frac{1 + s r_{be} C_{be}}{r_{be}} \right) R_E = V_{be} \left( \frac{r_{be} + 1 + s r_{be} C_{be}}{r_{be}} \right) R_E \] (6.140)
Therefore,

\[ V_{b'e} = \frac{r_{b'e}}{R_E} \left( \frac{1}{1 + g_m r_{b'e} + s r_{b'e} C_{b'e}} \right) V_o \]  \hspace{1cm} (6.141)

Now,

\[ V_{b'c} = V_o + V_{b'e} = V_o + V_o \frac{r_{b'e}}{R_E} \left( \frac{1}{1 + g_m r_{b'e} + s r_{b'e} C_{b'e}} \right) \]  \hspace{1cm} (6.142)

Hence

\[ \frac{V_o}{V_{b'c}} = \frac{1}{1 + \frac{r_{b'e}}{R_E} \left( \frac{1}{1 + g_m r_{b'e} + s r_{b'e} C_{b'e}} \right)} \cdot \frac{1}{R_E \left( 1 + g_m r_{b'e} + s r_{b'e} C_{b'e} \right)} \]  \hspace{1cm} (6.143)

This reduces to

\[ \frac{V_o}{V_{b'c}} = \frac{1}{(R_E + r_{b'e}) \left( 1 + g_m r_{b'e} + s r_{b'e} C_{b'e} \right)} \cdot \frac{R_E}{(1 + g_m r_{b'e} + s r_{b'e} C_{b'e})} \]  \hspace{1cm} (6.144)
But

\[ \frac{R_E}{R_E + r_{b'e}} \frac{1 + g_m r_{b'e}}{1 + \frac{r_{b'e}}{R_E}} = \frac{R_E (1 + g_m r_{b'e})}{R_E + r_{b'e} + g_m r_{b'e}} = \frac{R_E (1 + g_m r_{b'e})}{R_E (1 + \frac{r_{b'e}}{R_E} + g_m r_{b'e})} \approx 1, R_E \gg \frac{1}{g_m} \]

(6.145)

Hence

\[ \frac{V_o}{V_{b'c}} \approx \frac{1 + sC_{b'e} \frac{r_{b'e}}{1 + g_m r_{b'e}}}{1 + s \frac{C_{b'e} r_{b'e}}{1 + g_m r_{b'e} + \frac{r_{b'e}}{R_E}}} \]

(6.146)

Finally, since the input impedance seen at the transistor base is high, the ratio

\[ V_{b'c} / V_i \approx \frac{1/sC_{b'}}{R_S + r_{bb'} + 1/sC_{b'}} = \frac{1}{1 + sC_{b'}(R_S + r_{bb'})} \]

Then the voltage gain is given by

\[ \frac{V_o}{V_i} = \frac{1}{1 + sC_{b'}(R_S + r_{bb'})} \cdot \frac{1 + sC_{b'e} \frac{r_{b'e}}{1 + g_m r_{b'e}}}{1 + s \frac{C_{b'e} r_{b'e}}{1 + g_m r_{b'e} + \frac{r_{b'e}}{R_E}}} \]

(6.147)

Thus if \( R_E \gg r_{b'e} \) then \( C_{b'e} \gg C_{b'c} \). This suggests a very high frequency response for the common collector amplifier if driven from a low source impedance and has a high value emitter resistor in which case the time constant \( C_{b'c} r_{bb'} \) is small compared with \( C_{b'e} r_{b'e} \). Then

\[ V_{b'c} \approx V_i. \] Under such circumstances, the effect of \( r_{bb'} \) and \( C_{b'e} \) come into play and limit the overall frequency response. Then the circuit bandwidth is primarily set by \( r_{bb'} \) and \( C_{b'c} \) at a frequency

\[ f_U = \frac{1}{2\pi (R_S + r_{bb'}) C_{b'}} \]

(6.148)

**Example 6.7** Determine the upper cut-off frequency for the common collector amplifier shown in Fig. 6.49 where a 2N3904 transistor is used.
Solution For the emitter follower Fig. 6.49 driven from a low source impedance of 50 Ω, the upper cut-off frequency $f_U$ is given by

$$f_U = \frac{1}{2\pi (R_S + r_{br'}) C_{cb'}} = \frac{1}{2\pi \times (50 + 20) \times 4 \times 10^{-12}} = 568 \text{ MHz}$$

### 6.11 High-Frequency Response of a Common Source FET Amplifier

The equivalent circuit for the JFET at high frequency is shown in Fig. 6.50. There are two main junction capacitances, namely the gate-source capacitance $C_{gs}$ and the gate-drain capacitance $C_{gd}$. Consider the common source configuration shown in Fig. 6.51. In this configuration, the equivalent circuit becomes that shown in Fig. 6.52. Based on Miller’s theorem, the capacitor $C_{gd}$ may be replaced by a capacitor $C_{gd}(1 + g_m R_L)$
across $C_{gs}$ where $R'_L = R_L / r_{ds}$. In such a case the source resistance $R_S$ and the capacitance

$$C = C_{gs} + C_{gd} \left(1 + g_m R'_L \right)$$

form a low-pass filter with cut-off frequency

$$f_{H1} = \frac{1}{2\pi R_S \left[C_{gs} + \left(1 + g_m R'_L \right) C_{gd}\right]}$$

(6.149)

**Fig. 6.50** High-frequency equivalent circuit of JFET
This frequency can be increased by reducing $R_S$ which corresponds to driving the circuit from a low-impedance source. Note also that by Miller’s theorem a capacitor of approximate value $C_{gd}$ appears across the
output between the drain and ground. This capacitor introduces another pole at a frequency given by

$$f_{H2} = \frac{1}{2\pi R_L//r_{ds}C_{gs}}$$  \hspace{1cm} (6.150)

This frequency would typically be higher than that associated with $R_S$ in (6.149).

**Example 6.8** Find the cut-off frequency of the common source amplifier shown in Fig. 6.53. The JFET has the following characteristics:

- $C_{gs} = 50$ pF, $C_{gd} = 6$ pF, $r_d = 100$ kΩ, $g_m = 5$ mA/V, $R_S = 5$ kΩ

![Common source JFET amplifier](image)

**Solution** Using (6.149),

$$f_{H1} \approx \frac{1}{2\pi R_S |C_{gs} + (1 + g_m R_L') C_{gd}|}$$

the upper cut-off frequency is given by

$$f_{H1} \approx \frac{1}{2\pi 5000 [50 + (1 + 5 \times 7.4) 6] \times 10^{-12}} = 114 \text{ kHz}.$$
other pole frequency is given by
\[ f_{H2} = \frac{1}{2\pi R_L'//\tau_{ds}C_{gs}} = \frac{1}{2\pi \times 8 \times 100 \times 50 \, \text{pF}} = 430 \, \text{kHz}. \]

### 6.12 High-Frequency Response of a Common Gate FET Amplifier

In the common source amplifier, the gate-source capacitance and the Miller capacitance both limited the high frequency response of the circuit. In the common gate amplifier of Fig. 6.54 the capacitance between the drain and the source is small and therefore the Miller effect is insignificant. As in the case of the common base configuration, a good high-frequency response is expected. The equivalent circuit is shown in Fig. 6.55. To simplify the analysis, the voltage source \( V_i \) is converted to a current source \( V_i/R_i \) and the bias-setting resistor \( R_S \) is omitted since in generally, \( R_S \gg 1/g_m \) where \( 1/g_m \) is the input impedance of the configuration. Thus,

\[ R_m = \frac{g_m r_{b'e} R_S R_F R_L}{(R_S + r_{bb'} + r_{b'e})(R_F + R_L) + g_m r_{b'e} R_S R_L} \tag{6.151} \]

\[ V_{gs} = -\left( g_m V_{gs} + \frac{V_i}{R_i} \right) \frac{1}{1/R_i + sC_{gs}} \tag{6.152} \]
Fig. 6.54 Common gate FET amplifier

Fig. 6.55 Equivalent circuit of common gate amplifier
This becomes
\[ V_{gs} \left( 1 + \frac{g_m R_i}{1 + sR_i C_{gs}} \right) = V_{gs} \left( \frac{1 + g_m R_i + sR_i C_{gs}}{1 + sR_i C_{gs}} \right) = -V_i \frac{1}{1 + sR_i C_{gs}} \] (6.153)

Hence
\[ \frac{V_o}{V_i} \cdot \frac{V_{gs}}{V_i} = -\frac{g_m R_L}{1 + sC_{gd} R_L} \cdot \frac{1}{1 + g_m R_i + sR_i C_{gs}} \] (6.154)

This reduces to
\[ \frac{V_o}{V_i} = -\frac{g_m R_L}{1 + g_m R_i} \cdot \frac{1}{(1 + sC_{gd} R_L)(1 + sC_{gs} R_i//1/g_m)} \] (6.155)

From (6.155), the upper cut-off frequency is given by
\[ f_L = \frac{1}{2\pi R_L C_{gd}} \] (6.156)

since the pole introduced by \( C_{gs} \) and \( R_i//1/g_m \) is in general at a higher frequency.

**Example 6.9** For a common gate JFET amplifier with \( R_S = 1 \) k and \( R_L = 9 \) k, using the JFET of Example 6.8, find the upper cut-off frequency of the circuit.

**Solution** For the JFET of Example 6.8, \( C_{gd} = 6 \) pF. From (6.156), the upper cut-off frequency is given by
\[ f_L = \frac{1}{2\pi R_L C_{gd}} = \frac{1}{2\pi \times 9 \times 6 \text{ pF}} = 2.9 \text{ MHz}. \]

### 6.13 High-Frequency Response of a Common Drain FET Amplifier

We now consider the common drain or source follower configuration shown in Fig. 6.56. The associated equivalent circuit is presented in Fig. 6.57. Here, \( R_G \) and \( r_{ds} \) have been omitted since both are generally quite large.
From Fig. 6.57,

\[ V_o = V_{gs} \left( g_m + sC_{gs} \right) R_S \]  \hspace{1cm} (6.157)

From which

\[ V_o = \frac{V_{gs} g_m}{R_S} \]  \hspace{1cm} (6.158)
Now

\[ V_{gs} = \frac{V_o}{R_S \left(g_m + sC_{gs}\right)} \]

Therefore

\[ V_{gd} = V_o + V_{gs} = V_o \frac{1 + \left(g_m + sC_{gs}\right)R_S}{\left(g_m + sC_{gs}\right)R_S} \]

If \( g_mR_S \gg 1 \), then \( \frac{g_mR_S}{1 + g_mR_S} \approx 1 \) and in (6.160) \( V_o/V_{gd} \rightarrow 1 \). This suggests a very high-frequency response for the common drain amplifier when driven by a low source impedance \( R_i \) (in which case \( V_{gd} \approx V_i \)) and has a high value of FET source resistor \( R_S \). Note however that a non-zero \( R_i \) in conjunction with \( C_{gs} \) and the small Miller capacitance resulting from \( C_{gd} \) form a low-pass filter which limits the eventual frequency response of this circuit.

### 6.14 High-Frequency Response of Multistage Amplifiers

For amplifier systems in which there are cascaded stages such as discussed in Chap. 5, each stage introduces at least one pole in the frequency response of the overall system. When two or more stages are cascaded, the effect on the frequency response is the introduction of additional poles at the same or different frequencies. Thus, an amplifier comprising two common emitter stages will have at least two poles given by

\[ A_V(j\omega) = \frac{k}{(1 + j\omega/f_{o1})(1 + j\omega/f_{o2})} \]
where $k$ is the low-frequency gain of the cascaded amplifier and $f_{01}$ and $f_{02}$ are the two poles of the system. A frequency response plot illustrating the position of the poles is shown in Fig. 6.58. It can be shown that for $f \gg f_{01}, f_{02}$, the slope of the curve approaches $-40$ dB/decade which is twice the value of a single pole system. Similarly, if a third stage is added, the resulting system will have at least three poles resulting in a high-frequency roll-off rate of $-60$ dB/decade as shown in Fig. 6.58. These poles may be close or separated in frequency depending on the configuration of the particular cascaded amplifier. Each pole introduces phase shift (lag) between the output signal and the input signal and this must be considered when designing feedback amplifiers if instability is to be avoided in such systems. This is fully discussed in Chap. 7 on feedback amplifiers.

![Frequency plots of two- and three-pole system](image)

**Fig. 6.58** Frequency plots of two- and three-pole system

**Example 6.10** The transfer function of a three-pole amplifier system is given in (6.162).

$$A_V(j\omega) = \frac{10^4}{(1 + jf/10)(1 + jf/10^3)(1 + jf/10^4)}$$  \hspace{1cm} (6.162)
Plot the asymptotic curve for this system, indicating the low-frequency gain and the position of each pole.

**Solution**  From the transfer function (6.162), there are three poles. The break frequency resulting from each pole is given by $f = f_0$ where $f_0$ is the defined by the pole function $(1 + jf/f_0)$. Examination of each of these poles in (6.162) reveals the pole frequencies as $f_{o1} = 10$ Hz, $f_{o2} = 1$ kHz and $f_{o3} = 10$ kHz. The low-frequency gain $A_V(\text{DC})$ is found when $f \to 0$ which corresponds to $A_V(\text{DC}) = 10^4$. Hence the asymptotic curve is easily found by drawing a horizontal line starting at $10^4$ at some frequency below $f_{o1} = 10$ Hz and after passing through the frequency $f_{o1} = 10$ Hz changes slope from zero to $-20$ dB/decade. As the frequency increases, it continues at this slope and changes to $-40$ dB/decade after passing through the frequency $f_{o2} = 1$ kHz. With further increase in frequency the slope changes to $-60$ dB/decade as the line passes through $f_{o3} = 10$ kHz. This is the final slope change. This is shown in Fig. 6.59.
6.15 Applications

In this section, several circuits discussed in previous chapters are simulated in order to illustrate high-frequency response characteristics.

6.15.1 Direct Coupled Ring-of-Three

The circuit in Fig. 6.60 is a three-stage direct coupled amplifier that has a very high gain. It comprises three common emitter gain stages that are directly coupled and operating from a 9 V supply. The output of $Tr_1$ drives $Tr_2$, and the output of $Tr_2$ drives $Tr_3$. The resistor chain $R_6 - R_5 - R_1$ provides bias current to the base of $Tr_1$. It represents a DC feedback loop that ensures that there is bias stability at the output. Any change in the quiescent voltage at the collector of $Tr_3$ is corrected by changes in $Tr_1$ and $Tr_2$. Capacitor $C_3$ short-circuits the feedback signal to ground for AC. Selecting a current of 0.5 mA for $Tr_1$, it follows that $R_2 = 0.7 \text{ V}/0.5 \text{ mA} = 1.4 \text{ k}$. Similarly, with a current of 0.5 mA for $Tr_2$, then $R_3 = 0.7 \text{ V}/0.5 \text{ mA} = 1.4 \text{ k}$. In the final stage, since this is the output that drives an external load, a current of 1 mA is selected. For maximum symmetrical swing, the voltage across $R_4$ must be $9/2 = 4.5 \text{ V}$. 
Hence $R_4 = 4.5/1 \text{ mA} = 4.5 \text{ k}$. The base current of $Tr_1$ is 0.5 mA/100 = 5 μA. Let the current through the bias resistor string $R_6 - R_5 - R_1$ be 10 times this value in order to ensure bias stability. Then $R_1 = 0.7/50 \text{ μA} = 14 \text{ k}$. Since the voltage at the collector of $Tr_3$ is 4.5 V, then $R_5 + R_6 = (4.5 - 0.7)/50 \text{ μA} = 76 \text{ k}$. This resistance may have to be adjusted for higher gain transistors. Setting $R_5 = R_6$ gives $R_5 = R_6 = 76 \text{ k}/2 = 38 \text{ k}$. For adequate low-frequency response, coupling capacitors $C_1 = C_2 = 10 \text{ μF}$. Capacitor $C_3$ is chosen to ensure grounding of the feedback signal at a low frequency relative to the signals being amplified. A value of 47 μF is used. This circuit has a gain of about 100 dB and a bandwidth of 300 kHz.

*Ideas for Exploration:* (i) Simulate the system and determine the gain by injecting a low-amplitude sine wave at 1 kHz. It will be observed that the high gain means that the amplifier output will be driven into clipping for all but the lowest signal amplitudes. (ii) Measure the gain for one or two lower-gain amplifiers discussed previously for comparison.
6.15.2 Common Emitter Amplifier with Local Series Feedback

The circuit in Fig. 6.61 is a voltage divider-biased common emitter amplifier designed using the principles of Chap. 2. Its frequency response for varying values of \( R_e \) was simulated using multisim while keeping the sum \( R_e + R_E = 2 \) k constant so that the bias conditions remain unchanged. The results are shown in Table 6.1. As \( R_e \) increased from 100 to 500 \( \Omega \), the bandwidth of the circuit increased from 1.9 to 4.9 MHz, while the gain decreased from 36.2 to 24.3 dB as illustrated in Fig. 6.36. This confirms the theory discussed in Sect. 6.6 and verifies the use of local series feedback to extend the bandwidth while stabilizing the gain of a common emitter amplifier.
**Fig. 6.61** Common emitter amplifier with partially bypassed emitter resistor

**Table 6.1** Results of frequency response tests of CE amplifier with local series feedback

<table>
<thead>
<tr>
<th>Resistor $R_e$</th>
<th>100 Ω</th>
<th>200 Ω</th>
<th>300 Ω</th>
<th>400 Ω</th>
<th>500 Ω</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandwidth</td>
<td>1.9 MHz</td>
<td>2.9 MHz</td>
<td>3.7 MHz</td>
<td>4.4 MHz</td>
<td>4.9 MHz</td>
</tr>
<tr>
<td>Voltage gain</td>
<td>36.2 dB</td>
<td>31.4 dB</td>
<td>28.3 dB</td>
<td>26 dB</td>
<td>24.3 dB</td>
</tr>
</tbody>
</table>

**Ideas for Exploration:** (i) Simulate the system and measure frequency response of the circuit for various values of $R_e$. (ii) Measure the gain for the system and observe that the gain becomes more stable as $R_e$ increases.
6.15.3 Common Emitter Amplifier with Local Shunt Feedback

The circuit in Fig. 6.62 is a collector-base feedback biased common emitter amplifier designed using the principles of Chap. 2. The feedback component $R_f$ in series with the capacitor $C_f$ allows the changing of the effective feedback resistor $R_F$ for signals while maintaining bias conditions thereby applying local shunt feedback. Its frequency response for varying values of $R_f$ was tested with a source resistance of 10 k. The results are shown in Table 6.2. As $R_f$ decreased from 100 to 1 k, the bandwidth of the circuit increased from 1 to 87.2 MHz while the gain decreased from 18.6 to −20 dB as illustrated in Fig. 6.39. This confirms the theory discussed in Sect. 6.7 and verifies the use of local shunt feedback to extend the bandwidth while stabilizing the gain of a common emitter amplifier.

![Common emitter amplifier with local shunt feedback](image_url)
Table 6.2 Results of frequency response tests of CE amplifier with local shunt feedback

<table>
<thead>
<tr>
<th>Resistor $R_f$</th>
<th>100 k</th>
<th>50 k</th>
<th>20 k</th>
<th>10 k</th>
<th>1 k</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandwidth</td>
<td>1 MHz</td>
<td>2 MHz</td>
<td>5 MHz</td>
<td>9.6 MHz</td>
<td>87.2 MHz</td>
</tr>
<tr>
<td>Voltage gain</td>
<td>18.6 dB</td>
<td>13.2 dB</td>
<td>5.6 dB</td>
<td>0 dB</td>
<td>-20 dB</td>
</tr>
</tbody>
</table>

**Ideas for Exploration:** (i) Simulate the system and measure frequency response of the circuit for various values of $R_f$. (ii) Measure the gain for the system and observe that the gain becomes more stable as $R_f$ decreases.

### 6.15.4 Cascode Amplifier Using BJTs

The circuit in Fig. 6.63 is a Cascode amplifier comprising a BJT in a common emitter configuration driving another transistor in a common base mode. The first transistor is biased with a collector current of 1 mA using $R_B$, while the base of the second transistor is held at a fixed voltage using two 1N4148 silicon diodes. A source resistance of $R_S = 1$ k was used. The frequency response of the circuit was tested using a 10 mV sinusoidal input. The bandwidth of the system was measured at 5.6 MHz. A common emitter amplifier with 1 mA current and the same load resistor and source resistor has a bandwidth of 343 kHz which is significantly lower. Thus, the Cascode arrangement prevents the multiplication of the collector-base capacitance of the first transistor and subsequent formation of a low-pass filter with the 1 k resistor at the input. This confirms the theory discussed in Sect. 6.8 and verifies the use of the Cascode for wideband amplification.
Ideas for Exploration: (i) Simulate the system and measure frequency response of the circuit for various values of $R_S$. (ii) Replace the diode bias arrangement with a potential divider with filter capacitor and examine the system performance.

6.15.5 Cascode Amplifier Using BJT and JFET

The circuit in Fig. 6.64 is a Cascode amplifier comprising a 2N3904 BJT in a common emitter configuration driving a JFET in a common gate mode. The first transistor is biased with a collector current of 1 mA using $R_B = 2.7 \, \text{M} \Omega$, while the gate of the JFET is connected to the emitter of the BJT as shown in Fig. 6.64. The 2N3458 JFET with a 1 mA drain current has a gate-source voltage of $-1.91 \, \text{V}$ which is sufficient for the proper operation of the BJT. A source resistance $R_S = 1 \, \text{k} \Omega$ is used. The frequency response of the circuit was tested using a 10 mV sinusoidal input. The bandwidth of the system was measured at 2.2 MHz. This again is better than a common emitter amplifier with 1 mA current and
the same load resistor and source resistor which has a bandwidth of 343 kHz. Because the common emitter BJT is operating into the low input impedance source of the JFET, the significant multiplication of the collector-base capacitance of the BJT is prevented. The advantage of this form of the Cascode amplifier is that no additional biasing arrangements for the JFET are necessary.

![BJT-JFET Cascode amplifier diagram](image)

**Fig. 6.64** BJT-JFET Cascode amplifier

*Ideas for Exploration:* (i) Simulate the system and measure frequency response of the circuit for various values of $R_S$. (ii) Try different JFETs while ensuring that the gate-source voltage at the particular quiescent current is sufficient to properly operate the BJT.

**Problems**

1. Determine the input coupling capacitor for the circuit shown in Fig. 6.65 in order that the amplifier have a low cutoff frequency of 150 Hz. Assume transistor $\beta = 125$. 

*Fig. 6.65* BJT-JFET Cascode amplifier
2. For the amplifier circuit shown in Fig. 6.66 which is biased for maximum symmetrical swing, determine a suitable value of coupling capacitor to realize a maximum lower cut-off frequency of 70 Hz.

3. Determine the output coupling capacitor $C_o$ for the circuit shown in Fig. 6.67 in order that the amplifier has a low-frequency cut-off frequency of 50 Hz. Assume transistor $\beta = 100$.

4. Determine $C_E$ for the common emitter amplifier in Fig. 6.68 in order to produce a lower cut-off frequency of less than 25 Hz. Assume all coupling capacitors are large.

5. Determine the capacitors $C_i$, $C_E$, and $C_o$ in the circuit of Fig. 6.69 to give $f_L = 80$ Hz. Assume $h_{fe} = 200$.

6. Evaluate the lower cut-off frequency resulting from each of the capacitors shown in Fig. 6.70.

7. A silicon NPN transistor has $f_T = 200$ MHz. Determine $C_{v'c}$ for a collector current of 2 mA.

8. State and verify Miller’s theorem.

9. For the common emitter amplifier shown in Fig. 6.71, determine the upper cut-off frequency. The transistor used has $f_T = 250$ MHz, $C_{cb'} = 4$ pF, and $\beta = 125$.

10. Determine the upper cut-off frequency for the common base amplifier shown in Fig. 6.72 where a 2N3904 transistor is used.

11. Determine the upper cut-off frequency for the common collector amplifier shown in Fig. 6.73 where a 2N3904 transistor is used.

12. Find the cut-off frequency of the common source amplifier shown in Fig. 6.74. The JFET has the following characteristics: $C_{gs} = 70$ pF, $C_{gd} = 8$ pF, $r_d = 150$ kΩ, $g_m = 10$ mA/V.
13. Draw the equivalent circuit of the circuit in Fig. 6.74.

14. For a common gate JFET amplifier with $R_S = 5 \, \text{k}$ and $R_L = 6 \, \text{k}$, using a JFET having $C_{gd} = 4 \, \text{pF}$, find the upper cut-off frequency of the circuit.

15. Explain the excellent wideband characteristics of the Cascode amplifier.

16. Sketch a common emitter amplifier in which local series feedback is used to improve the amplifier bandwidth. For the maximum bandwidth, what should be the nature of the source resistance?

17. Sketch a common emitter amplifier in which local shunt feedback is used to improve the amplifier bandwidth. For the maximum bandwidth, what should be the nature of the source resistance? For the realization of a Cascode amplifier using a JFET as the second stage, what is the necessary characteristic of the JFET for this arrangement.
**Fig. 6.65** Circuit for Question 1
Fig. 6.66  Circuit for Question 2
Fig. 6.67 Circuit for Question 3
Fig. 6.68 Circuit for Question 4

Fig. 6.69 Circuit for Question 5
**Fig. 6.70** Circuit for Question 6

**Fig. 6.71** Circuit for Question 9
Fig. 6.72  Circuit for Question 10

Fig. 6.73  Circuit for Question 11
Fig. 6.74  Circuit for Question 12

Bibliography


A feedback amplifier is one in which a portion of the output is fed back to the system input where it is combined with the input signal. The basic concept is shown in Fig. 7.1. At the amplifier input, the feedback signal which may be a voltage or current is combined with the input signal which is also a voltage or current through a summing or mixing network, and the resulting signal is passed into the amplifier system. The summing network is either a series circuit which mixes feedback voltage with source voltage or a shunt circuit which mixes feedback current with source current while the feedback network is most often a passive network, usually resistive.
The basic feedback principle in feedback systems is the sampling of a portion of the output signal such that when mixed with the input improves the overall characteristics of the amplifier. When any increase in the output signal results in a feedback signal into the input in such a way as to cause a decrease in the output signal, the amplifier is said to have negative feedback. Negative feedback is generally useful because it can improve the characteristics of the various amplifier topologies presented earlier. For example, feedback can produce a significant improvement in the linearity and frequency response of the amplifier and lower distortion and noise. Another advantage of negative feedback is that it stabilizes the gain of the amplifier against variations in the characteristics of the transistors or other active devices used in the amplifier. The price paid for these improvements is the lowered gain of the amplifier with feedback (closed-loop gain) compared with the gain of the amplifier without feedback (open-loop gain). Feedback can, however, result in amplifier instability, and therefore appropriate steps need to be taken to prevent this.

In this chapter, we introduce the concept of feedback and apply it to amplifier systems. The resulting circuits display a range of improved characteristics, which are discussed. At the end of the chapter, the student will be able to:

- Explain the feedback concept
- Discuss the different types of amplifiers and feedback
- Design feedback amplifiers
7.1 Classification of Amplifiers

Amplifier systems may be conveniently classified into four types: voltage amplifiers, current amplifiers, transconductance amplifiers, and trans-resistance amplifiers. This classification is based on the magnitudes of the input and output impedances of an amplifier relative to the source and load impedances, respectively.

7.1.1 Voltage Amplifier

The voltage amplifier accepts a voltage at its input and delivers a voltage at its output. It is convenient to represent the amplifier as a Thevenin equivalent circuit as shown in Fig. 7.2.

![Thevenin equivalent circuit of a voltage amplifier](image)

In order to amplify effectively, the input resistance $R_i$ of the voltage amplifier must be high so that most of the input voltage is dropped across the input of the amplifier and little is lost across the source resistance $R_s$, i.e., $R_i \gg R_s$. In such a case, $V_i \approx V_s$. Ideally, the input resistance must be infinite. In order to effectively deliver the voltage to a load, the output impedance $R_o$ of the system must be low so that most of the output voltage is delivered to the load $R_L$ and little is dropped across the output impedance, i.e., $R_o \ll R_L$. Under these conditions, the output voltage is $V_o \approx A_v V_i$. Then, the voltage at the amplifier output is proportional to the voltage at the input, the proportionality factor being independent of the magnitudes of the source and load resistances. Ideally, the output impedance of a voltage amplifier is zero.
7.1.2 Current Amplifier
The current amplifier accepts a current at its input and delivers a current at its output. It is convenient to represent this amplifier as a Norton equivalent circuit as shown in Fig. 7.3. In order to effectively amplify the current signal, the input impedance $R_i$ of the current amplifier must be low so that most of the input current flows into the input of the amplifier and little is lost through the source resistance $R_s$, i.e., $R_i \ll R_s$. In such circumstances, $I_i \approx I_s$. In order to effectively deliver the amplified current to a load, the output impedance $R_o$ of the system must be high so that most of the output current flows into the load $R_L$ and little is lost through the output impedance. Under these conditions, the output current $I_o \approx A_i I_i$, and the current at the output is proportional to the current input, the proportionality factor being independent of the magnitudes of the source and load resistances. Ideally, the input resistance of a current amplifier is zero, and the output resistance is infinite.

![Fig. 7.3 Norton equivalent circuit of a current amplifier](image)

7.1.3 Transconductance Amplifier
We turn now to the transconductance amplifier which accepts a voltage at its input and delivers a current at its output. For this system, it is convenient to represent the amplifier as a Thevenin equivalent input and a Norton equivalent output as shown in Fig. 7.4. In order to operate effectively, the input resistance $R_i$ must be high so that most of the input voltage is dropped across the input of the amplifier and little is lost
across the source resistance $R_s$, i.e., $R_i \gg R_s$. For these conditions, the input voltage $V_i \approx V_s$. In order to effectively deliver the output current to a load, the output resistance $R_o$ of the system must be high so that most of the current flows into the load $R_L$ and little flows into the shunt output $R_o$ resulting in an output current $I_o \approx G_m V_i$. Under these conditions, the output current is proportional to the input voltage, and the proportional factor is independent of the magnitudes of the source and load resistances. Ideally, the input and output resistances of a transconductance amplifier are both infinite.

![Fig. 7.4 Thevenin equivalent input and Norton equivalent output of a transconductance amplifier](image)

**7.1.4 Trans-resistance Amplifier**

Finally, the trans-resistance amplifier accepts a current at its input and delivers a voltage at its output. It is convenient to represent this system as a Norton equivalent input and Thevenin equivalent output as shown in Fig. 7.5. In order to amplify effectively, the input resistance $R_i$ of the trans-resistance amplifier must be low so that most of the input current flows into the input of the amplifier and little is lost through the source resistance $R_s$. In order to effectively deliver the output voltage to a load, the output resistance $R_o$ of the system must be low so that most of this voltage is delivered to the load $R_L$ and little is dropped across the output impedance. Then, the input current $I_i \approx I_s$ and the output voltage $V_o \approx R_m I_i$. As a result, the voltage at the output is proportional to the input current, and the factor of proportionality is independent of
the magnitudes of the source and load resistances. Ideally, the input and output resistances of a trans-resistance amplifier are both zero. Table 7.1 summarizes the characteristics of the four amplifier types.

![Norton equivalent input and Thevenin equivalent output of a trans-resistance amplifier](image)

**Fig. 7.5** Norton equivalent input and Thevenin equivalent output of a trans-resistance amplifier

**Table 7.1** Amplifier characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Voltage</th>
<th>Current</th>
<th>Transconductance</th>
<th>Trans-resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transfer function</td>
<td>$V_o = A_v V_i$</td>
<td>$I_o = A_i I_i$</td>
<td>$I_o = G_m V_i$</td>
<td>$V_o = R_m I_i$</td>
</tr>
<tr>
<td>Input resistance</td>
<td>$\infty$</td>
<td>0</td>
<td>$\infty$</td>
<td>0</td>
</tr>
<tr>
<td>Output resistance</td>
<td>0</td>
<td>$\infty$</td>
<td>$\infty$</td>
<td>0</td>
</tr>
</tbody>
</table>

### 7.2 Feedback Amplifier Topologies

Feedback may be applied to anyone of the amplifier topologies presented in the previous section in order to improve their performance. Thus, feedback around a voltage amplifier will increase its normally high input resistance and lower its normally low output resistance. The method of application depends on the topology, and in this section we explore such methods. In each of the four configurations considered, the output signal may be sampled using an appropriate sampling network and this signal applied at the input by way of a suitable feedback network. At the amplifier input, the feedback signal is mixed with the external signal being amplified via a summing network and the resulting signal passed into the amplifier. The summing network is either a series mixer in which feedback voltage is compared
with source voltage or a shunt mixer in which feedback current is compared with source current.

Feedback around the four basic amplifier topologies is shown in Figs. 7.6, 7.8, 7.10, and 7.12. The voltage amplifier, trans-resistance amplifier, transconductance amplifier, and current amplifier have, respectively, voltage-series feedback, voltage-shunt feedback, current-series feedback, and current-shunt feedback.

**Fig. 7.6** Feedback voltage amplifier

### 7.2.1 Voltage-Series Feedback

For the voltage amplifier in Fig. 7.6, the output signal being sampled is a voltage, and this sampling is done by connecting across the output. The resulting feedback voltage $V_f$ must be subtracted from the input voltage $V_s$ by placing the signal in series with the input voltage. Note that the input and output signal voltages must be in phase for voltage subtraction to take place. The result is voltage-series feedback. From Fig. 7.6,

$$P_D \geq V_Z I_{Z_{mx}}$$

(7.1)

where $V_f = \beta V_o$. The output voltage is given by

$$V_o = \beta V_f$$

(7.2)
This gives

\[ V_i = I_b (h_{ie} + 1/sC_i) \]  \hspace{1cm} (7.3)

Therefore, system voltage gain with feedback \( A_{vf} = \frac{V_o}{V_s} \) is given by

\[ R = \frac{V_{inn} - V_Z}{I_{Zmn} + I_L} \]  \hspace{1cm} (7.4)

The result (7.4) shows that voltage-series feedback around a voltage amplifier results in the amplifier gain reduced by the factor \((1 + \beta A_v)\).

An example of the application of voltage-series feedback is shown in the simplified two-transistor circuit of Fig. 7.7 consisting of a common emitter amplifier \( Tr_1 \) driving another common emitter amplifier \( Tr_2 \). A portion of the output voltage at the collector of \( Tr_2 \) is returned through the feedback network \( R_F R_E \) to the emitter of \( Tr_1 \), where it is subtracted from the input voltage.
7.2.2 Voltage-Shunt Feedback

In the case of the trans-resistance amplifier of Fig. 7.8, the output signal being sampled is a voltage and again the sampling is accomplished by connecting across the output. However, the sampled voltage must first be converted to a current since it must be subtracted from the input signal current. The subtraction is effected by connecting the feedback current in shunt with the input current. Note that the output voltage must be inverted relative to the voltage associated with the input current for current subtraction to take place. The result is voltage-shunt feedback. From Fig. 7.8

\[ I_R \geq 10 \ I_B \]  

(7.5)

where \( I_f = \beta V_o \). The output voltage is given by

\[ V'' = \frac{-\alpha}{\beta} V_o \]  

(7.6)
This gives

$$V_o (1 + \beta R_m) = R_m I_s \tag{7.7}$$

Therefore, system trans-resistance with feedback $R_{mf} = \frac{V_o}{I_s}$ is given by

$$R_{mf} = \frac{R_m}{1 + \beta R_m} \tag{7.8}$$

The result (7.8) shows that voltage-shunt feedback around a trans-resistance amplifier results in the amplifier trans-resistance reduced by the factor $(1 + \beta R_m)$. An example of the application of voltage-shunt feedback is the single transistor common emitter amplifier shown in Fig. 7.9, where the output voltage at the collector of the transistor develops a feedback current in resistor $R_F$ which is connected between the collector and base of the transistor.
7.2.3 Current-Series Feedback

For the transconductance amplifier in Fig. 7.10, the output signal is a current rather than a voltage, and sampling this signal requires connecting directly in the current output path, i.e., in series. The sampled current must then be converted to a voltage in order to subtract it from the input signal voltage by connecting in series. The input voltage must be in phase with the associated feedback voltage for the voltage subtraction process to take place. The result is current-series feedback. From Fig. 7.10,

\[ P_D = V_Z I_{Z_{MAX}} \]  \hspace{1cm} (7.9)

where \( V_f = \beta I_o \). The output current is given by

\[ I_o = G_m V_i = G_m (V_s - V_f) = G_m V_s - G_m \beta I_o \]  \hspace{1cm} (7.10)

Fig. 7.9 Voltage-shunt feedback
This gives

\[ I_o (1 + \beta G_m) = G_m V_s \]  \hspace{1cm} (7.11)

Therefore, system transconductance with feedback \( G_{mf} = \frac{I_o}{V_s} \) is given by

\[ G_{mf} = \frac{G_m}{1 + \beta G_m} \]  \hspace{1cm} (7.12)

The result (7.12) shows that voltage-shunt feedback around a transconductance amplifier results in the amplifier transconductance reduced by the factor \( 1 + \beta G_m \). An example of the application of this type of feedback is the single transistor common emitter circuit of Fig. 7.11. Here, the output current \( I_o \) is sampled by the emitter resistor \( R_E \), where a feedback voltage \( V_f \) is developed. This voltage appears in series with the input voltage \( V_s \) from which it is subtracted. It should be noted that the output current develops a voltage across the collector resistor \( R_L \) which is available at the collector of the transistor.
Finally, for the current amplifier in Fig. 7.12, the output signal is again a current, and therefore the sampling must be effected by connecting in the signal path, i.e., in series. The sampled current is then subtracted from the input current by connecting the feedback current in shunt with the input current. For the current subtraction to take place, the associated input and output voltages must be out of phase. The resulting connection is referred to as current-shunt feedback. From Fig. 7.12

\[ I_R \geq 10 \quad I_B \]  \hspace{1cm} (7.13)

where \( I_f = \beta I_o \). The output current is given by

(7.14)
This gives

\[ I_o (1 + \beta A_i) = A_i I_s \]  \hspace{1cm} (7.15)

Therefore, system current gain with feedback \( A_{if} = \frac{I_o}{I_s} \) is given by

\[ A_{if} = \frac{A_i}{1 + \beta A_i} \]  \hspace{1cm} (7.16)

The result (7.16) shows that current-shunt feedback around a current amplifier results in the amplifier current gain reduced by the factor \((1 + \beta A_i)\). An example of current-shunt feedback is demonstrated in the simplified two-transistor circuit of Fig. 7.13. The output current \( I_o \) is sampled by the feedback network \( R_F R_E \) and a feedback current \( I_f \) flows through \( R_F \). This current is subtracted from the input current.
In this section, we discuss the transfer function of the various amplifiers with negative feedback. We do so using a generalized amplifier system as shown in Fig. 7.14 which represents the four amplifier types considered, namely, voltage, current, transconductance, and trans-resistance. In the diagram, the (open-loop) transfer gain $A$ is for the four amplifier types $A_V, A_I, G_M, R_M$, while the feedback network has a reverse transmission factor $\beta$. For the amplifier, we have

$$R_{F_1} \gg h_{ie}$$  \hspace{1cm} (7.17)

$$X_f = \beta X_o$$ \hspace{1cm} (7.18)

and

$$X_d = X_S - X_f$$ \hspace{1cm} (7.19)
where \( X_s \) is the input signal, \( X_o \) is the output signal, \( X_f \) is the feedback signal, and \( X_d \) is the error signal. Using (7.19) and (7.18) in (7.17) gives the closed-loop transfer gain \( A_f \) as

\[
A_f = \frac{A}{1 + \beta A}
\]  

(7.20)

**Fig. 7.14** Basic feedback amplifier system

Note that for negative feedback, \(|1 + \beta A| > 1\) and therefore \(|A_f| < |A|\), i.e., the closed-loop gain of the amplifier, is less than the open-loop gain. The opposite is true for positive feedback as it occurs in oscillators. For the feedback system, the quantity \( A\beta \) is called the loop gain and represents the gain experienced by a signal that travels through the amplifier \( A \) and back to the input via the feedback network \( \beta \). Thus, from (7.20),

\[
20 \log A_f = 20 \log A - 20 \log (1 + A\beta)
\]

\[
\approx 20 \log A - 20 \log A\beta
\]

(7.21)

\[
20 \log A\beta = 20 \log A - 20 \log A_f
\]

(7.22)

i.e., the loop gain in decibels is equal to the difference between the open-loop gain in decibels and the closed-loop in decibels. The loop
gain is, therefore, an indication of the amount of feedback around the amplifier.

A simple application of this involves operational amplifiers. In the 741, for example, the open-loop response is shown in Fig. 7.15 with a low-frequency gain of $10^5$ or 100 dB. For a closed-loop gain of 10 corresponding to 20 dB, it follows that the amount of feedback applied to the op-amp is $100 \text{ dB} - 20 \text{ dB} = 80 \text{ dB}$. If the closed-loop gain is reduced to 1 or 0 dB, then the feedback level increases to 100 dB.

![Open-loop response of 741 op amp](image)

**Fig. 7.15** Open-loop response of 741 op amp

Three conditions must be satisfied for the above feedback analysis to hold true:

1. The input signal is transmitted to the output through the amplifier A and not through the network $\beta$.
2. The feedback signal is transmitted from the output to the input through the $\beta$ block and not through the amplifier A.
3. The reverse transmission factor $\beta$ of the feedback network is independent of the load and the source resistances.
7.4 Gain Stabilization Using Negative Feedback

The components in an amplifier system are likely to experience changes in values arising from environmental changes in temperature, ageing, component replacement, and other factors. These changes in component values will generally result in changes in the gain of the amplifier. In many applications, amplifier gain changes are unacceptable. Feedback stabilizes amplifier gain against component value change. To see this, consider the basics amplifier with feedback shown in Fig. 7.14. The closed-loop gain from (7.20) is

\[ A_f = \frac{A}{1 + \beta A} \]  

(7.23)

In the presence of a large amount of negative feedback, the loop gain \( A\beta \) is much greater than one and, therefore, (7.23) reduces to

\[ A_f \approx \frac{A}{\beta A} = \frac{1}{\beta} \]  

(7.24)

i.e., for \( A\beta \gg 1 \), the closed-loop gain is \( 1/\beta \) and is independent of the open-loop gain \( A \). Since \( \beta \) can be made independent of \( A \), it follows from (7.24) that for \( A\beta \gg 1 \), changes in \( A \) do not affect the closed-loop gain \( A_f \). The feedback renders the closed-loop amplifier virtually immune to changes in open-loop gain.

In order to quantify this gain-stabilizing effect, consider again Eq. (7.23). For a constant feedback factor \( \beta \), differentiating \( A_f \) with respect to \( A \) gives

\[ \frac{dA_f}{dA} = \frac{(1 + \beta A) - \beta A}{(1 + \beta A)^2} = \frac{1}{(1 + \beta A)^2} \]  

(7.25)

Equation (7.25) leads to

\[ dA_f = \frac{dA}{(1 + \beta A)^2} \]  

(7.26)
Using Eq. (7.23), we have

\[
\frac{dA_f}{A_f} = \frac{dA/(1 + \beta A)^2}{A/(1 + \beta A)} = \frac{1}{(1 + \beta A)} \frac{dA}{A}
\]  
(7.27)

The absolute value of Eq. (7.27) is

\[
\left| \frac{dA_f}{A_f} \right| = \frac{1}{|1 + \beta A|} \left| \frac{dA}{A} \right|
\]  
(7.28)

Equation (7.28) shows that the magnitude of the fractional change in gain with feedback \(|dA_f/A_f|\) is reduced by the factor \(1 + A\beta \approx A\beta\) or the loop gain, compared to the fractional change without feedback \(|dA/A|\).

**Example 7.1** An amplifier with gain 1000 has a gain change of 20% due to temperature. Calculate the change in gain of the feedback amplifier if the feedback factor \(\beta = 0.1\).

**Solution** Using Eq. (7.28),

\[
\left| \frac{dA_f}{A_f} \right| = \frac{1}{(1 + 0.1 \times 1000)} \times 20 = 0.198 \approx 0.2\%.
\]

Thus, while the amplifier open-loop gain changes from 1000 by 20%, the closed-loop amplifier changes by only 0.2%. This represents a 100-fold improvement. The factor \(D = 1 + A\beta\) is sometimes called the desensitivity.

### 7.5 Increase in Bandwidth Using Negative Feedback

Consider an amplifier with low-frequency gain \(k\) and bandwidth \(f_o\) given by

\[
A = \frac{k}{1 + jf/f_o}
\]  
(7.29)

Then substituting (7.29) in (7.23) gives

\[
\frac{dA_f}{A_f} = \frac{dA/(1 + \beta A)^2}{A/(1 + \beta A)} = \frac{1}{(1 + \beta A)} \frac{dA}{A}
\]  
(7.30)
\[ A_f = \frac{A}{1 + \beta A} = \frac{k}{1 + jf/f_o} \frac{1}{1 + \beta \frac{k}{1 + jf/f_o}} \]

This becomes
\[ A_f = \frac{k}{1 + k\beta + jf/f_o} = \frac{k/ (1 + \beta k)}{1 + jf/f_o (1 + k\beta)} \]  

(7.31)

This finally reduces to
\[ A_f = \frac{k'}{1 + jf/f_o'} \]  

(7.32)

where
\[ k' = k/ (1 + \beta k) \]  

(7.33)

and
\[ f_o' = f_o (1 + \beta k) \]  

(7.34)

From (7.33), the closed-loop low-frequency gain is \( k' = \frac{k}{1 + \beta k} \approx \frac{1}{\beta} \) for \( k\beta \gg 1 \), and the closed-loop bandwidth is \( f_o' = f_o (1 + \beta k) \approx f_o k\beta \) again for \( k\beta \gg 1 \). This means that the bandwidth of the amplifier is increased by the factor \( k\beta \) as a result of the negative feedback. This occurs at the expense of low-frequency gain which is reduced by the same factor shown in Fig. 7.16.
Example 7.2  An amplifier with a transfer function (7.29) has a low-frequency open-loop gain of 100,000 and an open-loop bandwidth of 10 Hz. For a closed-loop gain of 10, calculate the closed-loop bandwidth of the amplifier.

Solution  For this amplifier $f_o = 10$ Hz and $k = 100,000$. Since $k \gg 1$, to a very good approximation the closed-loop gain is $1/\beta$ giving $\beta = 0.1$. Therefore, the closed-loop bandwidth $f_o' = f_o(1 + \beta k) \approx f_o k \beta = 10 \times 100,000 \times 0.1 = 100,000$ Hz.

7.6 Feedback and Harmonic Distortion
Distortion in an amplifier results from nonlinearity associated with the active elements in the system. This nonlinearity increases as the amplitude of the signal increases and is, therefore, greatest at the output of the amplifier. The effect is the generation of harmonics of the input signal that were not present originally. This is called harmonic distortion which can also be reduced by the use of negative feedback. Consider the open-loop amplifier shown in Fig. 7.17.
The distortion produced in this amplifier is represented as the signal $D$ added at the output. This assumes that the amplifier is approximately linear such that the principle of superposition applies. Thus,

$$V_o = Av_i + D \quad (7.35)$$

If feedback is now applied as shown in Fig. 7.18, then

$$Z_i = h_{ie} || R_B \ . \quad (7.36)$$

and

$$\varepsilon = V_i - \beta V_o \quad (7.37)$$
Substituting (7.37) in (7.36) yields

\[ V_o = \frac{AV_i}{1 + A\beta} + \frac{D}{1 + A\beta} \]  \hspace{1cm} (7.38)

From (7.38) and (7.35), it can be seen that for the same output \( V_o \), the distortion \( D \) produced at the output has been reduced by a factor of the loop gain. Negative feedback reduces output-generated noise by the same factor as it does output stage distortion.

### 7.7 Input Resistance

Negative feedback directly influences the input resistance of an amplifier. The nature of that influence depends on the method of application of the feedback. Specifically, if the feedback is series applied (voltage), then since the feedback voltage opposes the input signal voltage, it follows that the input current is reduced from what it would be without the feedback, and therefore the overall effect is an increase in input resistance. This result, which we will quantify shortly, is not affected by whether the feedback signal is derived by voltage or current sampling. If the feedback is shunt applied (current), then since the feedback current increases the signal current, the effect is a decrease in the input resistance to this type of amplifier. Again, the effect is independent of the method of sampling of the feedback signal. In the sections to follow, the effect of negative feedback on amplifier input resistance is examined and quantified.

#### 7.7.1 Voltage-Series Feedback

The Thevenin equivalent of the voltage-series feedback amplifier is shown in Fig. 7.19. Since the amplifier input resistance is being considered, the source resistance is set to zero. The amplifier input resistance \( R_{if} \) is then given by \( R_{if} = V_s/I_i \). In order to determine this, we have

\[ V_s = V_f + V_i = \beta V_o + I_i R_i \]  \hspace{1cm} (7.39)

and

\[ \text{(7.40)} \]
\[ V_o = \frac{A_v V_i R_L}{R_o + R_L} = A_V I_i R_i \]

where

\[ A_V = \frac{V_o}{V_i} = \frac{A_v R_L}{R_o + R_L} \]  \hspace{1cm} (7.41)

is the open-loop gain of the amplifier, taking the effect of the external load into account, and \( A_v \) is the open-loop gain with no load. Hence, \( A_V \to A_v \) as \( R_L \to \infty \). Substituting (7.40) in (7.39) and rearranging we get

\[ R_{if} = \frac{V_s}{I_i} = \frac{V_i (1 + \beta A_V)}{I_i} = R_i (1 + \beta A_V) \]  \hspace{1cm} (7.42)

*Fig. 7.19* Thevenin Equivalent of voltage-series feedback amplifier

From (7.42) it can be seen that the input resistance of the amplifier is increased by the loop gain value as a result of the negative feedback.

### 7.7.2 Voltage-Shunt Feedback

The Norton equivalent input-Thevenin equivalent output representation of the voltage-shunt feedback amplifier is shown in Fig. 7.20. Since the amplifier input resistance is being considered, the source resistance is set to infinity (removed). In order to determine the amplifier input resistance \( R_{if} \) from Fig. 7.20, we have

\[ (7.43) \]
\[ I_s = I_f + I_i = \beta V_o + I_i \]

and

\[ V_o = \frac{R_m I_i R_L}{R_o + R_L} = R_M I_i \quad (7.44) \]

where

\[ R_M = \frac{V_o}{I_i} = \frac{R_m R_L}{R_o + R_L} \quad (7.45) \]

is the open-loop trans-resistance of the amplifier, taking the effect of the external load into account and \( R_m \) is the open-loop gain with no load. Therefore, \( R_M \to R_m \) as \( R_L \to \infty \). Substituting (7.44) in (7.43) and rearranging, we get

\[ R_{if} = \frac{V_i}{I_s} = \frac{V_i}{I_i (1 + \beta R_M)} = \frac{R_i}{1 + \beta R_M} \quad (7.46) \]

![Voltage-shunt feedback amplifier](image)

**Fig. 7.20** Voltage-shunt feedback amplifier

From (7.46) it can be seen that the input resistance of the amplifier is lowered by the factor of the loop gain as a result of the negative feedback.

### 7.7.3 Current-Series Feedback
The Thevenin equivalent input-Norton equivalent output representation of the current-series feedback amplifier is shown in Fig. 7.21. Since the amplifier input resistance is being considered, the source resistance is again set to zero. In order to determine the amplifier input resistance \( R_{if} \) from Fig. 7.21, we have

\[
V_o = -I_o R_L = -h_f e I_b R_L
\]  

(7.47)

and

\[
I_o = \frac{G_m V_i R_o}{R_o + R_L} = G_M V_i
\]  

(7.48)

where

\[
G_M = \frac{I_o}{V_i} = \frac{G_m R_o}{R_o + R_L}
\]  

(7.49)

is the open-loop transconductance of the amplifier, taking the effect of the external load into account, and \( G_m \) is the open-loop gain with no load. Therefore, \( G_M \to G_m \) as \( R_L \to 0 \). Substituting (7.48) in (7.47) and rearranging, we get

\[
R_{if} = \frac{V_s}{I_i} = \frac{V_i (1 + \beta G_M)}{I_i} = R_i (1 + \beta G_M)
\]  

(7.50)

Fig. 7.21 Current-series feedback amplifier
From (7.50) it can be seen that the input resistance of the amplifier is increased by the factor of the loop gain as a result of the negative feedback.

### 7.7.4 Current-Shunt Feedback

The Norton equivalent of the current-shunt feedback amplifier is shown in Fig. 7.22. Since the amplifier input resistance is being considered, the source resistance is once again set to infinity (removed). In order to determine the amplifier input resistance $R_{if}$ from Fig. 7.22, we have

\[
I_s = I_f + I_i = \beta I_o + I_i \tag{7.51}
\]

and

\[
A_V = \frac{V_o}{V_i} = \frac{A_o R_L}{R_o + R_L} \tag{7.52}
\]

where

\[
A_I = \frac{I_o}{I_i} = \frac{A_o R_o}{R_o + R_L} \tag{7.53}
\]

is the open-loop current gain of the amplifier, taking the effect of the external load into account, and $I_i$ is the open-loop gain with no load.

Therefore, $A_I \rightarrow A_o$ as $R_L \rightarrow 0$. Substituting (7.52) in (7.51) and rearranging, we get

\[
R_{if} = \frac{V_i}{I_s} = \frac{V_i}{I_i (1 + \beta A_I)} = \frac{R_i}{1 + \beta A_I} \tag{7.54}
\]
From (7.54) it can be seen that the input resistance of the amplifier is decreased by the factor of the loop gain as a result of the negative feedback.

## 7.8 Output Resistance

Negative feedback also directly influences the output resistance of an amplifier. The nature of that influence depends on the method of deriving the feedback. In particular, if the feedback is acquired by sampling an output voltage, then regardless of the method of application of the feedback, the output resistance is reduced in an attempt to stabilize that output voltage. If on the other hand the feedback is acquired by sampling an output current, then the effect is an increase in output resistance in an attempt to maintain the output current. Again, the effect is independent of the method of application of the feedback signal. In the following sections, the effect of negative feedback on amplifier output resistance is examined and quantified.

### 7.8.1 Voltage-Series Feedback

Using the Thevenin equivalent of the voltage-series feedback amplifier Fig. 7.19, we determine the output resistance $R_{of}$ of this topology. In order to do so, the load $R_L$ must be disconnected and the input signal removed by setting $V_s = 0$. A voltage $V$ is then applied to the output terminals as in Fig. 7.23 and the resulting current $I$ flowing into the
output terminal determined. Then the ratio $V/I$ gives the output resistance $R_{of}$. From Fig. 7.19, we have

$$I = \frac{V - A_vV_i}{R_o} = \frac{V + A_v\beta V}{R_o} \tag{7.55}$$

![Diagram of amplifier circuit](image)

**Fig. 7.23** Determining output resistance

Since with $V_s = 0$, $V_i = -\beta V$. It follows from (7.55) that $R_{of}$ is given by

$$R_{of} \equiv \frac{V}{I} = \frac{R_o}{1 + \beta A_v} \tag{7.56}$$

This result confirms that the output resistance $R_{of}$ of the amplifier with feedback is reduced. It is reduced by the factor $1 + \beta A_v$. $R_{of}$ is the output resistance seen by the load $R_L$. If $R_L$ is treated as part of the amplifier, then the output resistance with feedback becomes $R_{of}^\prime$ in parallel with $R_L$, that is

$$R_{of}^\prime = \frac{R_{of}R_L}{R_{of} + R_L} \tag{7.57}$$

Substituting for $R_{of}$ from (7.56) yields

$$R_{of}^\prime = \frac{R_o}{1 + \beta A_v} \frac{R_L}{R_o + \frac{R_L}{1 + \beta A_v} + R_L} \tag{7.58}$$
This reduces to

\[
R'_{o_f} = \frac{R_o R_L / (R_o + R_L)}{1 + \beta A_v R_L / (R_o + R_L)} = \frac{R'_o}{1 + \beta A_V}
\]  

(7.59)

Here, \(R'_o = \frac{R_o R_L}{R_o + R_L}\) is the parallel resistance of \(R_o\) and \(R_L\) representing the amplifier output resistance with feedback with \(R_L\) treated as part of the amplifier, and \(A_V = A_v R_L / (R_o + R_L)\) is the amplifier gain with feedback, taking the effect of \(R_L\) into account. Note that (7.59) takes the same form as (7.56).

### 7.8.2 Voltage-Shunt Feedback

Using the Norton equivalent input-Thevenin equivalent output representation of the voltage-shunt feedback amplifier in Fig. 7.20, we determine the output resistance \(R_{o_f}\) of this topology using a similar approach. We again disconnect the load \(R_L\) from the amplifier output and set the input signal \(I_s = 0\). With a voltage \(V\) applied to the output the resulting current \(I\) flowing into the output terminal determined is given by

\[
I = \frac{V - R_m I_i}{R_o} = \frac{V + R_m \beta V}{R_o}
\]

(7.60)

since with \(I_s = 0\), \(I_i = -\beta V\). It follows from (7.60) that \(R_{o_f}\) is given by

\[
R_{o_f} \equiv \frac{V}{I} = \frac{R_o}{1 + \beta R_m}
\]

(7.61)

This result shows that the output resistance \(R_{o_f}\) of the amplifier without feedback is reduced by the factor \(1 + \beta R_m\). If \(R_L\) is treated as part of the amplifier, then the output resistance with feedback becomes \(R_{o_f}\) in parallel with \(R_L\), which reduces to

\[
R'_{o_f} = \frac{R'_o}{1 + \beta R_M}
\]

(7.62)
Here, $R'_o$ is again the parallel resistance of $R_o$ and $R_L$ representing the amplifier output resistance without feedback with $R_L$ treated as part of the amplifier, and $R_M = R_mR_L/(R_o + R_L)$ is the amplifier transresistance without feedback, taking the effect of $R_L$ into account.

### 7.8.3 Current-Series Feedback

We here use the Thevenin equivalent input-Norton equivalent output representation of the current-series feedback amplifier as shown in Fig. 7.21 in order to determine the output resistance. We disconnect the load $R_L$ from the amplifier output and set the input signal $V_s = 0$. A voltage $V$ applied to the output produces a current $I$ flowing into the output terminal. With $V_s = 0$, $V_f = -\beta I$ and, therefore, $V_i = -V_f = \beta I$. Hence, the current $I$ is given by

$$I = \frac{V}{R_o} - G_mV_i = \frac{V}{R_o} - G_m\beta I$$  \hspace{1cm} (7.63)

It follows from (7.63) that $R_{of}$ is given by

$$R_{of} \equiv \frac{V}{I} = R_o (1 + \beta R_m)$$  \hspace{1cm} (7.64)

Result (7.64) indicates that the output resistance of the amplifier is increased by a factor of the loop gain of the amplifier.

### 7.8.4 Current-Shunt Feedback

In analyzing the current-shunt feedback configuration, we use the Norton equivalent representation of the feedback amplifier shown in Fig. 7.22. We disconnect the load $R_L$ from the amplifier output and set the input signal $I_s = 0$. A voltage $V$ applied to the output produces a current $I$ flowing into the output terminal. Since for $I_s = 0$, $I_f = -\beta I$ and, therefore, $I_i = -I_f = \beta I$, then the current $I$ is given by

$$I = \frac{V}{R_o} - A_iI_i = \frac{V}{R_o} - A_i\beta I_i$$  \hspace{1cm} (7.65)

It follows from (7.65) that $R_{of}$ is given by
Again, the current sampling in this amplifier configuration results in an increased amplifier output resistance.

7.9 Analysis of Feedback Amplifiers

In this section, we apply negative feedback to actual transistor amplifier circuits and discuss methods of analyzing the various configurations. Specifically, we consider the voltage-series, voltage-shunt, current-shunt, and current-series modes of feedback systems.

In analyzing a feedback amplifier, the open-loop gain $A$ and the feedback factor $\beta$ need to be determined. These two parameters allow the determination of the closed-loop gain and other characteristics of the closed-loop system. The open-loop transfer function $A$ represents the gain of the amplifier with no feedback but considering the loading of the $\beta$ network. In order to determine $A$, the following rules must be applied:

**Input Circuit**
1. For voltage sampling, set the output voltage to zero. This corresponds to short-circuiting the output terminal to ground.
2. For current sampling, set the output current to zero. This corresponds to open-circuiting the output terminal.

**Output Circuit**
1. For series mixing, set the input current to zero. This corresponds to opening the input terminal.
2. For shunt mixing, set the input voltage to zero. This corresponds to short-circuiting the input terminal.

These steps ensure that the negative feedback is reduced to zero while still taking into account the loading of the feedback circuitry on the basic amplifier.

\[
R_{of} \equiv \frac{V}{I} = R_o (1 + \beta A_i)
\]
7.9.1 Voltage-Series Feedback

Consider the voltage amplifier comprising two common emitter amplifiers that are cascaded to produce a higher overall voltage gain as shown in Fig. 7.24. The biasing circuitry is omitted for simplicity. We first note that because of the signal inversion produced by each stage, the output voltage at the collector of the second stage is in phase with the input voltage at the base of the first stage. We note also that a signal injected at the emitter of the first stage will produce an inverted output signal and, therefore, the feedback signal must be applied at the emitter of $Tr_1$. Voltage sampling is thus effected by sampling the output voltage at the collector of the second stage and applying series feedback mixing with the input voltage at the emitter of the first stage. The $\beta$ network, therefore, comprises resistors $R_F$ and $R_E$. One of the assumptions necessary for the feedback analysis to hold is that there must be no signal feed-forward through the feedback network. The emitter current of $Tr_1$ is approximately equal to the input current and flows forward through the feedback network $R_E//R_F$. However, this current is generally small as compared with the current $I_F$ from the output. In order to determine the basic amplifier without feedback, we first determine the input circuit of the amplifier by setting the output voltage to zero. The effect of this is that $R_F$ appears in parallel with $R_E$. Following this, the output circuit is determined by setting the input current to zero. This corresponds to opening the connection of the junction of $R_E$ and $R_F$ to the emitter of $Tr_1$ with the result that $R_F$ appears in series with $R_E$. The resulting open-loop voltage amplifier is shown in Fig. 7.25. The feedback factor $\beta$ is given by

$$\beta = \frac{V_f}{V_o} = \frac{R_E}{R_F + R_E}$$ (7.67)
Fig. 7.24 Voltage-series feedback amplifier
The amplifier open-loop gain can now be found in the usual way following which feedback analysis can proceed. It should be noted that there is (local) current-series feedback in the first stage of the amplifier because of the presence of the un-bypassed emitter resistance. This kind of feedback is analyzed shortly. An example follows.

**Example 7.3** Evaluate the voltage gain, input resistance, and output resistance for the feedback voltage amplifier in Fig. 7.26. For the transistors $h_{fe} = 100$, $h_{ie} = 2.5 \text{ k}$, $h_{re} = h_{oe} = 0$. 
**Solution**

1. The first step is the evaluation of the open-loop gain of the amplifier, taking into account the loading effect of the feedback network. The effective load $R_{L1}$ of $Tr_1$ is $R_{L1} = 12 \, k\Omega / 153 \, k\Omega / 47 \, k\Omega / 2.5 \, k = 1.96 \, k\Omega$. The effective emitter resistance $R_e$ of $Tr_1$ is $R_{e1} = 470 \, k\Omega / 5.6 \, k = 434 \, \Omega$. Hence, the voltage gain $A_{V1}$ of the first stage is

$$A_{V1} = -\frac{h_{fe}R_{L1}}{h_{ie} + (1+h_{fe})R_{e1}} = -\frac{100 \times 1.96 \, k\Omega}{2.5 \, k + 101 \times 0.434 \, k\Omega} = -4.27.$$  

The effective load $R_{L2}$ of $Tr_2$ is $R_{L2} = 5.6 \, k\Omega / (5.6 + 0.47) \, k = 2.91 \, k\Omega$. Hence, the voltage gain $A_{V2}$ of the second stage is

$$A_{V2} = -\frac{h_{fe}R_{L2}}{h_{ie}} = -\frac{100 \times 2.91 \, k\Omega}{2.5 \, k\Omega} = -116.4.$$  

Therefore, the overall open-loop voltage gain $A_V$ is

$$A_V = A_{V1} \times A_{V2} = 4.27 \times 116.4 = 497.$$  

Now,
\[ \beta = \frac{R_E}{R_F + R_E} = \frac{470}{5600 + 470} = 0.077. \]

Also

\[ 1 + \beta A_V = 1 + 0.077 \times 497 = 39.3. \]

Therefore, the closed-loop voltage gain \( A_{Vf} \) is found to be

\[ A_{Vf} = \frac{A_V}{1 + \beta A_V} = \frac{497}{39.3} = 12.6. \]

This is quite close to the value for very large open-loop gain given by

\[ A_{Vf}(A_V \to \infty) = 1/\beta = 12.9. \]

2. Looking in at the base of the first transistor (i.e., omitting for the moment the two base biasing resistors), the open-loop input resistance \( R_i \) is

\[ R_i = h_{ie} + (1 + h_{fe}) R_{e1} = 2.5 \, k + 101 \times 0.47 \, k = 49.97 \, k. \]

There the input resistance \( R_{if} \) of the closed-loop amplifier is

\[ R_{if} = (1 + \beta A_V) R_i = 39.3 \times 49.97 \, k = 1.96 \, M. \]

The effective input resistance to the closed-loop amplifier would now be \( R_{if}/163 \) k/37 k, i.e., \( R_{if} \) in parallel with the two base biasing resistors which are outside the feedback loop of the amplifier.

3. The open-loop input resistance \( R_o \) is \( R_o = R_{L2} = 2.91 \, k \). Therefore, the closed-loop output resistance \( R_{of} \) is

\[ R_{of} = \frac{R_o}{1 + \beta A_V} = \frac{2.91 \, k}{39.3} = 74 \, \Omega. \]

Another voltage amplifier in which voltage-series feedback is employed is the emitter follower. In this circuit, the full output voltage constitutes the feedback voltage and is subtracted from the input voltage. The error voltage is that dropped across the base emitter junction of the transistor. It is possible to apply the feedback analysis to this circuit to arrive at the gain expression and other characteristics. This analysis shows that the emitter follower can be viewed as a common emitter amplifier with collector resistor \( R_E \) and open-loop gain

\[ A_V = \frac{h_{fe} R_E}{h_{ie}} = g_m R_E \]

around which 100\% voltage-series feedback corresponding to \( \beta = 1 \) is applied. The resulting closed-loop voltage gain is given by

\[ A_{Vf} = \frac{A_V}{1 + \beta A_V}. \]

This, therefore, gives
which of course is the voltage gain of the emitter follower found previously. The circuit’s increased input impedance, decreased output impedance, improved frequency response, and reduced distortion as compared with the common emitter amplifier also result from this voltage-series feedback. The common source amplifier is an analogous case using FET technology. A third example of a voltage-series feedback amplifier is the operational amplifier which will be discussed in Chap. 8.

7.9.2 Current-Shunt Feedback

An example of current-shunt feedback is the current amplifier comprising two common emitter amplifiers as shown in Fig. 7.27. The biasing circuitry is again omitted for simplicity. We note that because of the signal inversion produced by the first stage, the signal output at the emitter of the second stage is out of phase with the input signal at the base of the first stage. Current sampling of the output current in \( V_{o} \) is achieved by inclusion of the resistor \( R_{E} \) in the emitter of \( T_{r2} \) through which the output current \( I_{o} \) flows. In conjunction with resistor \( R_{F} \), the two resistors form a current divider (corresponding to the voltage divider in the voltage-series feedback case) which results in a feedback current \( I_{f} \) flowing away from the base of \( T_{r1} \) and subtracting from the input current \( I_{s} \). Because the output current is sampled and a feedback current is mixed at the input, this arrangement is current-shunt feedback. The \( \beta \) network, therefore, comprises resistors \( R_{F} \) and \( R_{E} \).

Note, however, that in this particular configuration, the output current is converted to a voltage in \( R_{2} \) giving \( V_{o} = I_{o}R_{2} \). Resistor \( R_{2} \) is, however, outside the feedback loop.
To determine the basic current amplifier without feedback, we determine the input circuit of the amplifier by reducing the output current to zero. This is done by opening the output current loop at the emitter of $Tr_2$. The effect of this is that $R_E$ appears in series with $R_F$ from the base of $Tr_1$ to ground. The output circuit is determined by setting the input voltage to zero. This corresponds to short-circuiting the input terminal of $Tr_1$ to ground. The result is that $R_F$ appears in parallel with $R_E$ at the emitter of $Tr_2$. The resulting open-loop amplifier is shown in Fig. 7.28. The signal source is represented as a Norton equivalent circuit since the feedback signal is a current. The open-loop current gain can now be found. Noting that the collector current is much larger than the base current of $Tr_2$, it follows that
From this the feedback factor beta is given by

$$\beta = \frac{I_f}{I_o} = \frac{R_E}{R_F + R_E}$$  \hspace{1cm} (7.70)

Because the input resistance of this feedback amplifier is low, the circuit is easily converted into a voltage amplifier by driving the input with a voltage signal $V_S$ operating into a resistor $R_S \gg R_{if}$ which gives $I_S = V_S/R_S$. 

![Open-loop amplifier circuit with feedback network loading](image)
Example 7.4  For the current amplifier as shown in Fig. 7.29, determine the closed-loop current gain, input resistance, and output resistance. For the transistors $h_{fe} = 100$, $h_{ie} = 2.5 \, \text{k}$, $h_{re} = h_{oe} = 0$. Determine $R_S$ to give a voltage gain of 15.

![Current-shunt feedback amplifier example](image)

**Fig. 7.29** Current-shunt feedback amplifier example

**Solution**

1. The open-loop current gain must first be determined. This is given by $A_I = \frac{I_o}{I_S} = \frac{I_o}{I_{b2}} \frac{I_{c1}}{I_{b1}} \frac{I_{b1}}{I_S}$. From the circuit $\frac{I_o}{I_{b2}} = -h_{fe} = -100$;

   \[ \frac{I_{b2}}{I_{c1}} = -\frac{R_1}{R_1 + R_2}, \]

   where (noting that $R_F \ll R_B$) we have $R_{i2} = h_{ie} + (1 + h_{fe}) \frac{R_E}{R_F} = 2.5 + 101 \times 0.1/1.2 = 11.8 \, \text{k}$. Hence,

   \[ \frac{I_{b2}}{I_{c1}} = -\frac{17.3}{17.3+11.8} = -0.59; \quad \frac{I_{c1}}{I_{b1}} = h_{fe} = 100 \text{ and} \]
The result is \[
\frac{I_{b1}}{I_s} = \frac{R_F + R_E}{R_F + R_E + h_{ie}} = \frac{1.2 + 0.1}{1.2 + 0.1 + 2.5} = 0.34.
\] The feedback factor is \[
\beta = \frac{R_E}{R_F + R_E} = \frac{0.1}{1.2 + 0.2} = 0.08
\]
and \[1 + \beta A_I = 1 + 0.08 \times 2006 = 161.5.\]
This gives the closed-loop current gain \[
A_{if} = \frac{A_I}{1 + \beta A_I} = \frac{2006}{161.5} = 12.4.
\]
This can be compared with the value \[A_{if}(A_I \to \infty) = 1/\beta = 12.5.\]

3. The open-loop input resistance to the current amplifier is given by \[R_i = h_{ie} / (R_F + R_E) = 2.5 / 1.3 = 0.855 \, \text{k}.\] Therefore, the closed-loop feedback is given by \[R_{if} = \frac{R_i}{1 + \beta A_I} = \frac{0.855}{161.5} = 5.3 \, \Omega.\] As a current amplifier with feedback, the input resistance is small as expected. To enable the circuit to accept a voltage signal input, a resistor \[R_S \gg R_{if}\] can be added in series with the input. For a voltage gain of 15, \[
\frac{V_o}{V_s} = \frac{I_o R_2}{I_s R_S} = A_{IF} \times \frac{R_i}{R_S} = 12.4 \times \frac{9 \, \text{k}}{R_S} = 15
\]
This gives \[R_S = 7.4 \, \text{k}.\]

3. The open-loop output resistance \[R_o\] looking in at the collector of the second transistor is \[R_o = \infty\] since \[h_{oe} = 0.\] Hence, the closed-loop output resistance \[R_{of}\] looking at the collector is \[R_{of} = R_o (1 + \beta A_I) = \infty.\] It follows, therefore, that the output resistance of the amplifier is \[R_{of} / R_2 = R_2 = 9 \, \text{k}.\]

Another example of current-shunt feedback is the common base amplifier configuration. Here, the full output current constitutes the feedback current that is subtracted from the input current. The error current flows in/out of the base of the transistor. By viewing the configuration this way, it is possible to apply the feedback analysis to this circuit to arrive at the current gain expression and other characteristics. This analysis shows that the common base amplifier can be viewed as a common emitter amplifier with open-loop current
gain $A_I = h_{fe}$ around which 100% current-shunt feedback corresponding to $\beta = 1$ is applied. The resulting closed-loop current gain is given by $A_{If} = \frac{A_I}{1 + \beta A_I}$. This, therefore, gives

$$A_{If} = \frac{h_{fe}}{1 + \beta h_{fe}} = \frac{h_{fe}}{1 + h_{fe}}$$  \hspace{1cm} (7.71)

which of course is the current gain of the common base amplifier. The circuit's reduced input impedance, increased output impedance, improved frequency response, and reduced distortion as compared with the common emitter amplifier also result from the current-shunt feedback. The common gate amplifier is an analogous case using FET technology.

7.9.3 Current-Series Feedback

The example of current-series feedback that we wish to consider is the single transistor circuit shown in Fig. 7.30. The sampled current signal is the output current $I_o$ flowing in resistor $R_E$, where it develops a feedback signal voltage $V_f$ across resistor $R_E$. Because of the arrangement in which feedback voltage $V_f$ is in series with the input voltage, then $V_f$ is subtracted from the input signal voltage, the error voltage driving the base-emitter junction of the transistor. Applying the rules of analysis, the input circuit of the open-loop amplifier is derived by opening the output loop. The result of this is that resistor $R_E$ appears in the input circuit, and this affects the open-loop transconductance of the amplifier. The output circuit is obtained by opening the input loop. The result is that $R_E$ also appears in the output circuit, but this has practically no effect on the output current. The open-loop circuit is shown in Fig. 7.31.
Fig. 7.30  Current-series feedback amplifier
The feedback factor is given by
\[
\beta = \frac{V_f}{I_o} = \frac{-I_oR_E}{I_o} = -R_E
\] (7.72)

The open-loop transconductance \( G_M \) is given by
\[
G_M = \frac{I_o}{V_s} = \frac{-h_fe I_b}{I_b(h_{ie} + R_E)} = -\frac{h_fe}{h_{ie} + R_E}
\] (7.73)

Hence, the closed-loop transconductance becomes
\[
G_{Mf} = \frac{I_o}{V_s} = \frac{G_M}{1 + \beta G_M} = \frac{-h_fe}{h_{ie} + (1 + h_{fe})R_E} = -\frac{1}{r_e + R_E}
\] (7.74)

It is possible to derive (7.74) using the \( h \)-parameter equivalent circuit for the closed-loop amplifier without using the equivalent circuit.
in Fig. 7.31. It is interesting to note that since $h_{fe} \gg 1$ then for sufficiently large $R_E$, $(1 + h_{fe})R_E \gg h_{ie}$ and (7.74) becomes $G_{Mf} \approx -1/R_E$ which is $1/\beta$. This represents stabilization of the transconductance consistent with the effects of negative feedback. The output current develops a voltage given by $V_o = I_o R_L$. Hence, the voltage gain of this circuit is

$$A_{Vf} = \frac{V_o}{V_s} = \frac{I_o R_L}{V_s} = G_{Mf} R_L = -\frac{h_{fe}R_L}{h_{ie} + (1 + h_{fe})R_E} = -\frac{R_L}{r_e + R_E}$$

(7.75)

obtained in Chap. 4. The open-loop input impedance of the amplifier is $R_i = h_{ie} + R_E$, and therefore the closed-loop input impedance is given by

$$R_{if} = (1 + \beta G_M)(h_{ie} + R_E) = h_{ie} + (1 + h_{fe})R_E$$

(7.76)

This is exactly the expression obtained using $h$-parameter analysis. Looking into the collector of the transistor the output impedance without feedback (in the absence of the output admittance $1/h_{oe}$) is infinite, and therefore the addition of feedback cannot increase it further. However, the output impedance involving the collector resistor $R_L$ is simply the infinite output impedance in parallel with $R_L$ which is $R_L$.

**Example 7.5** For the transconductance amplifier of Fig. 7.32, determine the closed-loop transconductance $G_{Mf}$, the closed-loop input impedance, and the closed-loop output impedance.
Solution We proceed in the manner developed in the case of the other two amplifiers. Thus, the open-loop transconductance is

\[ G_M = \frac{I_o}{V_s} = -\frac{h_{fe}}{h_{ie} + R_E} = -\frac{100}{2.5 + 2} = -22.22 \, \text{mA/V}. \]

\[ \beta = R_E = -2k. \] And hence

\[ 1 + \beta G_M = 1 - 2 \times (-22.22) = 45.44. \] Therefore,

\[ G_{Mf} = \frac{G_M}{1 + \beta G_M} = \frac{-22.22}{45.44} = -0.49 \, \text{mA/V}. \] Looking in at the base of the transistor the open-loop input impedance is

\[ R_i = h_{ie} + R_E = 2.5 + 2 = 4.5 \, \text{k}. \] Therefore, the closed-loop input impedance is

\[ R_{if} = (1 + \beta G_M)R_i = 45.44 \times 4.5 \, \text{k} = 204 \, \text{k}. \] The effective input impedance is

\[ R_{ef} = \frac{R_{if}}{173/27} = 21 \, \text{k}. \] Thus, the high input impedance of this circuit is reduced by the biasing resistors which are outside the feedback loop. Looking into the collector of the amplifier, the open- and closed-loop
output impedance is $\infty$ since $h_{oe} = 0$. Therefore, the output impedance of the amplifier is $R_{of} = \infty//R_L = 9\, \text{k}$. Once again, the output current of this amplifier is converted to a voltage in $R_L$ yielding $V_o = I_o R_L$. Therefore, the voltage gain of the circuit is $V_o/V_S = I_o R_L/V_S = G_{Mf} R_L = -0.49 \times 9 = -4.4$, which is precisely the value obtained using Eq. (7.75).

7.9.4 Voltage-Shunt Feedback

The single transistor amplifier circuit of Fig. 7.33 is an example of voltage-shunt feedback. The sampled output voltage at the collector of the transistor develops a feedback current in the feedback resistor $R_F$. Because of the inverting action of the configuration, this current is subtracted from the input signal at the base of the transistor. The rules of feedback analysis give the input circuit of the open-loop amplifier by shorting the output node corresponding to setting $V_o = 0$. This results in $R_F$ being placed between the base and emitter of the transistor. The output circuit of the open-loop amplifier is determined by shorting the input node corresponding to setting $V_i = 0$. This places $R_F$ across the collector and emitter of the transistor. The signal source is represented as a Norton equivalent circuit since the feedback signal is a current. The resulting circuit is shown in Fig. 7.34.
Fig. 7.33 Voltage-shunt feedback amplifier

Fig. 7.34 Open-loop amplifier circuit with feedback network loading
From Fig. 7.33, since the output voltage \( V_o \) is much greater than the input voltage \( V_i \) at the transistor base and out of phase with it, for a positive going input voltage the feedback current \( I_f \) flows such that

\[
I_f = \frac{V_i - V_o}{R_F} \approx -\frac{V_o}{R_F}
\]  
(7.77)

Therefore,

\[
\beta = \frac{I_f}{V_o} = -\frac{1}{R_F}
\]  
(7.78)

Assuming \( R_F \gg R_L \), the open-loop trans-resistance \( R_M \) is given by

\[
R_M = \frac{V_o}{I_s} = \frac{-h_{fe}I_bR_LR_F}{I_b(h_{ie} + R_F)} = -\frac{h_{fe}R_LR_F}{h_{ie} + R_F}
\]  
(7.79)

Hence, the closed-loop trans-resistance becomes

\[
R_{Mf} = \frac{V_o}{I_s} = \frac{R_M}{1 + \beta R_M} = \frac{-h_{fe}R_LR_F}{h_{ie} + R_F + h_{fe}R_L}
\]  
(7.80)

If \( R_F \gg h_{ie} \) then (7.80) becomes

\[
R_{Mf} = \frac{V_o}{I_s} = -\frac{h_{fe}R_L}{R_F}
\]  
(7.81)

The open-loop input impedance \( R_i \) seen by the current source from Fig. 7.34 is \( R_i = R_F/h_{ie} \) and if \( R_F \gg h_{ie} \), then \( R_i = h_{ie} \). The closed-loop input impedance \( R_{if} \) is then

\[
R_{if} = \frac{R_i}{1 + \beta R_M} = \frac{h_{ie}}{1 + h_{fe}R_L/R_F}
\]  
(7.82)

Because the input resistance of this feedback amplifier is low, the circuit is easily converted into a voltage amplifier by driving the input with a voltage signal \( V_S \) operating into a resistor \( R_S \gg R_{if} \) which yields \( I_S = V_S/R_S \). The output impedance for the closed-loop amplifier is given by
The current feedback amplifier is another example of a trans-resistance amplifier with voltage-shunt feedback. This circuit will be discussed in Chap. 8.

Example 7.6 For the trans-resistance amplifier of Fig. 7.35, determine \( R_{Mf} \), \( R_{if} \), \( R_{of} \) and the value of \( R_S \) to give the system a voltage gain of 15. Use \( h_{fe} = 100 \) and \( h_{ie} = 250 \).

\[
R_{of} = \frac{R_o}{1 + \beta R_M} = \frac{R_L//R_F}{1 + \beta R_M} \tag{7.83}
\]

\[
\beta = -\frac{1}{R_F} = -\frac{1}{93}. \text{ Hence, } 1 + \beta R_M = 1 + \frac{99.73}{93} = 2.07. \text{ Therefore,}
\]
\[ R_{Mf} = \frac{R_M}{1 + \beta R_M} = -\frac{99.73}{2.07} = -48.2 \text{ k} \]. The open-loop input resistance

\[ R_i = R_f/h_{ie} = 93/0.25 \approx 250 \text{ } \Omega \], and hence the closed-loop input resistance is

\[ R_{if} = \frac{R_i}{1 + \beta R_i} = \frac{250}{2.07} = 121 \text{ } \Omega \]. Since \( R_{if} \) is low, if \( R_S \gg R_{if} \) then

\[ I_S = V_S/R_S \], where \( V_S \) is a voltage signal. Then the system voltage gain is

\[ V_o/V_S = V_o/I_S R_S = \frac{R_{Mf}}{R_S} \]. For a voltage gain of \(-10\), \( R_{Mf}/R_S = -10 \) and therefore \( R_S = \frac{48.2}{-10} = 4.8 \text{ k} \). Note that 4.8 k \( \gg \) 121 \( \Omega \). Finally, the output resistance is given by

\[ R_{of} = \frac{R_o}{1 + \beta R_M} = \frac{R_L/R_f}{1 + \beta R_M} = \frac{1/93}{2.07} = 483 \text{ } \Omega \].

The configuration shown in Fig. 7.36a involves voltage-shunt feedback as in Fig. 7.35 except that the use of an emitter follower prevents loading of \( R_L \) by \( R_F \). Hence, the assumption \( R_F \gg R_L \) is no longer necessary. Therefore, the transfer function \( V_o/I_S \) is given by

\[ R_{Mf} = \frac{V_o}{I_s} = \frac{R_M}{1 + \beta R_M} = \frac{-h_{fe}R_L R_F}{h_{ie} + R_F + h_{fe}R_L} \]

(7.84)

*Fig. 7.36 Two-transistor configuration with voltage-shunt feedback*
Since $R_S \gg R_{if}$ which yields $I_s = V_s/R_S$, then

$$V_o/V_S = V_o/I_sR_S = \frac{-h_{fe}R_LR_F}{h_{ie} + R_F + h_{fe}R_L}/R_S,$$

(7.85)

Hence

$$\frac{V_o}{V_S} = \frac{-h_{fe}R_LR_F/R_S}{h_{ie} + R_F + h_{fe}R_L} = \frac{-R_F/R_S}{1 + (h_{ie} + R_F)/h_{fe}R_L} = \frac{-R_F/R_S}{1 + R_F/h_{fe}R_L}, R_F \gg h_{ie}$$

(7.86)

For the bootstrapped version shown in Fig. 7.36b, $h_{fe}R_L \rightarrow h_{fe}R_L'$, where $R_L' \gg R_L$ and therefore

$$\frac{V_o}{V_S} = \frac{-R_F/R_S}{1 + (h_{ie} + R_F)/h_{fe}R_L'} = \frac{-R_F}{R_S}$$

(7.87)

**Example 7.7** Design a two-transistor voltage-shunt feedback amplifier with a gain of 50 using the topology in Fig. 7.36.

**Solution** Let $V_{CC} = 20$ V. Since the gain is in the first stage, maximum symmetrical swing is applied to this stage. Using a collector current of 1 mA in $Tr_1$, for maximum symmetrical swing, $R_L = 10$ V/1 mA = 10 k. If bootstrapping is to be applied, this resistor must be split into two resistors giving $R_{La} = R_{Lb} = 5$ k. The emitter voltage of $Tr_2$ is $10 - 0.7 = 9.3$ V. Using a current of 2 mA in $Tr_2$, then $R_E = 9.3/2 = 4.7$ k. Noting that the base current of $Tr_1$ (1 mA/100) is provided by $R_F$, then $(9.3 - 0.7)/R_F = 1$ mA/100 giving $R_F = 860$ k. From Example 5.8 in Chap. 5, the effective load resistor $R_L$ of $Tr_1$ is increased to $R_L' = 66$ k.

Therefore, using (7.87) for the voltage gain of the circuit, $R_F/R_S = 20$ giving $R_S = R_F/50 = 17.2$ k.

**7.10 Voltage Amplifiers**

Following the general consideration of the four types of amplifiers and the application of negative feedback around them, we wish now to
consider in greater detail the amplifier type of the set that is most widely used: the voltage amplifier. The voltage amplifier can be found in an amazing array of products and applications. The operational amplifier (see Chap. 8) is one example of a voltage amplifier that is manufactured in vast numbers for a wide range of applications including audio systems, industrial systems and domestic applications. These devices are available for almost any conceivable requirement including low noise, low distortion, high voltage output, high current output, or high-frequency applications.

As pointed out previously, a voltage amplifier has a high input impedance and low output impedance. The input signal is a voltage and the output signal is also a voltage. The feedback type is voltage-series as shown in Fig. 7.37b. This is often referred to as the non-inverting configuration since the output signal is in phase with the input signal. The sample $V_f$ of the output signal $V_o$ given by $V_f = \beta V_o$, where $\beta = R_1/(R_2 + R_1)$ is subtracted from the input signal $V_i$. The resulting error signal $\varepsilon = V_i - V_f$ is amplified by the voltage amplifier. This type of feedback makes a good voltage amplifier better by increasing the bandwidth and the (already high) input impedance and decreasing the distortion and the (already low) output impedance.

![Fig. 7.37](image)

The transfer function $A_{vf} = V_o/V_i$ of the open-loop amplifier (i.e., amplifier without feedback) in Fig. 7.37a is represented here by a single
pole system given by

\[ A_v = \frac{A_o}{1 + jf/f_o} \]  \hspace{1cm} (7.88)

where \( A_o \) is the low-frequency gain and \( f_o \) is the open-loop break frequency or bandwidth. The transfer function \( A_{vf} = V_o/V_i \) of the closed-loop amplifier in Fig. 7.37b is given by

\[ R = \frac{V_{in} - V_Z}{I_{Zmn} + I_L} \]  \hspace{1cm} (7.89)

After substituting for \( A_v \) using (7.88) and manipulating, we get

\[ A_{vf} = \frac{(1 + \frac{R_2}{R_1}) \cdot \frac{A_o\beta}{1 + A_o\beta}}{1 + jf/f_o (1 + A_o\beta)} \]  \hspace{1cm} (7.90)

where

\[ V_{GS} = V_G - I_D R_S \]  \hspace{1cm} (7.91)

is the feedback factor. At low frequencies, Eq. (7.90) reduces to

\[ A_{vf}(DC) = \left(1 + \frac{R_2}{R_1}\right) \cdot \frac{A_o\beta}{1 + A_o\beta} \]  \hspace{1cm} (7.92)

In operational amplifiers and many voltage amplifiers, \( A_o \) is usually very large and hence the loop gain \( A_L = A_o\beta \) is usually such that \( A_o\beta \gg 1 \). Equation (7.90) therefore reduces to

\[ A_{vf} = \frac{1 + R_2/R_1}{1 + jf/f_o}, A_o\beta \gg 1 \]  \hspace{1cm} (7.93)

where

\[ \bar{f}_o = f_o A_o\beta \]  \hspace{1cm} (7.94)

is the closed-loop bandwidth. From (7.93), the low-frequency closed-loop gain \( A_{vf}(DC) \) for \( A_o\beta \gg 1 \) is given by
\[ A_{vf}(DC) = 1 + R_2/R_1 = 1/\beta \]  

Note that as expected, Eq. (7.92) also reduces to
\[ A_{vf}(DC) = 1 + R_2/R_1, A_o\beta \gg 1 \]  

**Example 7.8**  A voltage amplifier has a low-frequency open-loop gain of \(10^4\). If \(\beta = 0.1\), determine the low-frequency closed-loop gain using (7.92) and compare with (7.95).

**Solution**  From (7.92),
\[ A_{vf}(DC) = \left(1 + \frac{R_2}{R_1}\right) \frac{A_o\beta}{1+A_o\beta} = \frac{A_o}{1+10^4} = 9.99 \]

Using (7.95), the low-frequency closed-loop gain is given by
\[ A_{vf}(DC) = 1 + \frac{R_2}{R_1} = 1/\beta = 1/0.1 = 10. \]
These two values are within 0.1%.

As can be seen from (7.94), the closed-loop bandwidth \(\bar{f}_o\) varies with the loop gain \(A_o\beta\). Alternatively, since \(A_o\) is fixed, by expressing (7.94) in terms of \(A_{vf}(DC)\) as
\[ \bar{f}_o = f_o/A_o/A_{vf}(DC) \]

it is clear that the closed-loop bandwidth \(\bar{f}_o\) is inversely proportional to the closed-loop low-frequency gain \(A_{vf}(DC)\). The loop gain \(A_L = A_o\beta\) expressed in dB is given by
\[ A_L (dB) = 20 \log (A_o\beta) = 20 \log A_o + 20 \log \beta = 20 \log A_o - 20 \log (1/\beta) = 20 \log A_o - 20 \log A_{vf}(DC) = \text{low-freq open-loop gain (dB)} - \text{low-freq closed-loop gain (dB)} \]
As can be seen from Fig. 7.38, the loop gain $A_L$ is an indication of the amount of feedback around the amplifier. Since from (7.95), the minimum value of $A_{vf}(DC)$ is $A_{vf}(DC) = 1$ corresponding to $\beta = 1$, this represents the maximum amount of feedback applied in the system. The maximum feedback occurs when $\beta = 1$ and is given by $A_{L\text{max}} = 20\log A_o$. This is the unity gain configuration and is obtained by setting $R_1 \to \infty$ and/or $R_2 = 0$ in Fig. 7.37. The corresponding bandwidth is given by

$$\bar{f}_{o(\text{max})} = f_o A_o$$  \hspace{1cm} (7.99)

which is referred to as the gain bandwidth product (GBP) of the voltage amplifier.

![Frequency response plot showing loop gain](image)

$\textbf{Fig. 7.38}$ Frequency response plot showing loop gain

The loop gain and closed-loop bandwidth are shown in Fig. 7.38. Finally, from (7.97),

$$A_{vf}(DC)f_o = f_o A_o = \text{GBP} = \text{const}$$  \hspace{1cm} (7.100)

This equation relates the closed gain with the closed-loop bandwidth, based on the GBP of the particular device.
Example 7.9  For example, for an amplifier with a GBP of 100 kHz, determine the closed-loop bandwidth if the closed-loop gain is 10.

Solution  Using Eq. (7.98), the closed-loop bandwidth would be 100 kHz/10 = 10 kHz.

Example 7.10  A voltage amplifier has an open-loop characteristic as shown in Fig. 7.39. For a closed-loop gain of 10 (20 dB), determine the following:

1. The open-loop bandwidth
2. The open-loop low-frequency gain
3. The GBP for the amplifier
4. The closed-loop bandwidth
5. The amount of applied feedback in the system

Fig. 7.39  Diagram for Example 7.9
Solution  From the characteristic shown in Fig. 7.39, (1) the open-loop bandwidth is 1 kHz; (2) the open-loop low-frequency gain is 80 dB; (3) the GBP is given by $GBP = f_o A_o = 10^3 \times 10^4 = 10^7$ Hz; (4) for a closed-loop gain of 10, the closed-loop bandwidth $\overline{f_o}$ is found using (7.100) which yields $\overline{f_o} = \frac{GBP}{A_{v_f}(DC)} = \frac{10^7}{10} = 1 \text{ MHz}$; (5) the amount of feedback is open-loop gain (dB)−closed-loop gain (dB) = 80 dB − 20 dB = 60 dB.

The open-loop characteristic shown in Fig. 7.39 corresponding to a voltage amplifier with a single pole characteristic will have a maximum phase shift between output and input of 90°. It can be shown that such a system will not become unstable with feedback and can accommodate 100% feedback. As a result, it is sometimes referred to as being unity gain stable. However, steps have to be taken with (multistage) amplifiers in order to realize conditions that ensure system stability when feedback is applied. These methods are discussed in Sect. 7.12. Also, the analysis developed is directly applicable to practical operational amplifiers since the assumed high input impedance and low output impedance that characterize a good voltage amplifier are easily met by modern operational amplifiers. These will be more extensively discussed in the next chapter.

### 7.11 Transistor Feedback Amplifier

The feedback concept can be applied in the design of a voltage amplifier system using discrete devices. One basic topology is shown in Fig. 7.40. It comprises three amplifying stages: the input stage made up of the differential amplifier $Tr_1$ and $Tr_2$, the intermediate common emitter stage $Tr_3$ and the emitter follower output stage $Tr_4$. Signals applied at the input of the differential amplifier $Tr_1 Tr_2$ are amplified and passed via $R_3$ to the second stage $Tr_3$. This common emitter amplifier provides the bulk of the voltage gain. The output stage $Tr_4$ is an emitter follower that provides a low-impedance output drive. In this configuration, the loading effects of the feedback network are negligible.
7.11.1 Differential Amplifier

In the differential amplifier stage, two transistors $Tr_1$ and $Tr_2$ are connected at their emitters where an approximately constant current $I$ through resistor $R_2$ is connected to supply bias current to each. Each transistor is basically in a common emitter mode with an input supplied to its base and an output taken from its collector. At the two base terminals of the differential amplifier are the input signal $V_i = v_{i1}$ at the base of $Tr_1$ and the feedback signal $V_f = v_{i2}$ at the base of $Tr_2$. The output $v_{o1}$ is taken at the collector of $Tr_1$ where resistor $R_3$ is connected.
It is possible to obtain an output $v_{o2}$ at the collector of $Tr_2$ by the inclusion of another resistor $R_3$. Thus, $v_{i1} - v_{i2}$ is the differential input voltage and $v_{o1}$ is the single-ended output voltage. Since there are two inputs and one output, the amplifier is said to have a double-ended input and a single-ended output.

In examining the small-signal behaviour of this circuit, the output voltage $v_{o1}$ at the collector of $Tr_1$ due to each input acting alone, that is, with the opposite input grounded, will be determined and then the superposition principle will be applied to determine the output due to both acting simultaneously. Consider the case where input 2 is grounded ($v_{i2} = 0$) and a small signal applied to input 1. We assume perfectly matched transistors $Tr_1$ and $Tr_2$ and, therefore, that $I_{C1} = I_{C2}$. Since $Tr_1$ is essentially a common emitter amplifier, $v_{i1}$ is amplified and inverted. For amplification of $v_{i1}$, $Tr_2$ functions as a common base amplifier. Hence, the input impedance $r_e$ of $Tr_2$ is the emitter resistance of $Tr_1$. Therefore, the voltage gain of $Tr_1$ is

$$A_{v1} = \frac{v_{o1}}{v_{i1}} = -\frac{h_{fe}R_L}{h_{ie} + (1 + h_{fe})r_e} \tag{7.101}$$

where

$$r_e = \frac{h_{ie}}{1 + h_{fe}} = \frac{0.025}{I_{C2}} \tag{7.102}$$

is the input impedance to the common base amplifier $Tr_2$ and $R_L$ is the load at the collector of $Tr_1$. Therefore,

$$A_{v1} = \frac{v_{o1}}{v_{i1}} = -\frac{h_{fe}R_L}{2h_{ie}} \approx -\frac{R_L}{2r_e} \tag{7.103}$$

Since the current $I = I_{E1} + I_{E2}$ in resistor $R_2$ is approximately constant, it follows that the change in $I_{E1}$ in response to $v_{i1}$ results in a corresponding change (of opposite sign) in $I_{E2}$. This can be used to produce an amplified voltage $v_{o2}$ at the collector of $Tr_2$ by the inclusion of a resistor, that is, in phase with $v_{i1}$. If $v_{i1}$ is now set to zero and an
input signal $v_{i2}$ applied at the base of $Tr_2$, then $Tr_2$ acts like a common emitter amplifier with an un-bypassed emitter resistor $r_e$ of $Tr_1$ with $Tr_1$ as a common base amplifier. Since there is no resistor in the collector of $Tr_2$, the change in collector current $I_{E2}$ does not produce an output voltage in $Tr_2$. Since the current $I$ is constant, it follows that the change in $I_{E2}$ in response to $v_{i2}$ results in a corresponding change (of opposite sign) in $I_{E1}$. This, therefore, produces an amplified voltage $v_{o1}$ at the collector of $Tr_1$ given by

$$A_{v2} = \frac{v_{o1}}{v_{i2}} = \frac{R_L}{2r_e} \quad (7.104)$$

Thus for the output $v_{o1}$ of $Tr_1$, from (7.103) the component due to $v_{i1}$ is $-\frac{R_L}{2r_e}v_{i1}$ and from (7.104) that due to $v_{i2}$ is $\frac{R_L}{2r_e}v_{i2}$. Using the superposition principle,

$$v_{o1} = -\frac{R_L}{2r_e} (v_{i1} - v_{i2}) \quad (7.105)$$

Hence, the gain [single-ended out/differential in] is given by

$$A_{V1} = \frac{v_{o1}}{v_{i1} - v_{i2}} = -\frac{R_L}{2r_e} \quad (7.106)$$

If a resistor $R_3$ is included in the collector of $Tr_2$, then by similar arguments the output $v_{o2}$ from the collector of $Tr_2$ is given by $v_{o2} = -v_{o1}$. Therefore, from (7.105)

$$v_{o2} = \frac{R_L}{2r_e} (v_{i1} - v_{i2}) \quad (7.107)$$

Hence, the differential output ($v_{o1} - v_{o2}$) is given by

$$v_{o1} - v_{o2} = -\frac{R_L}{r_e} (v_{i1} - v_{i2}) \quad (7.108)$$

i.e., the differential gain is given by

$$\quad (7.109)$$
\[
\frac{v_{o1} - v_{o2}}{v_{i1} - v_{i2}} = -\frac{R_L}{r_e}
\]

In the circuit of Fig. 7.40, the load \( R_L \) is resistor \( R_3 \) in parallel with the input impedance \( h_{ie} \) to transistor \( Tr_3 \) giving \( R_L = R_3//h_{ie3} \). Thus, the voltage gain of the input stage of Fig. 7.40 is given by

\[
A_{V1} = -\frac{R_3//h_{ie3}}{2r_e}
\]  
(7.110)

and

\[
h_{ie3} = \frac{h_{fe}}{40I_{C3}}
\]  
(7.111)

### 7.11.2 Common Emitter Amplifier

The second stage of the amplifier consists of transistor \( Tr_3 \) in a common emitter amplifier configuration with load \( R_4 \). This stage amplifies the output from the differential amplifier stage and provides most of the voltage gain of the overall amplifier. The gain of the stage is given by

\[
A_{V2} = -40I_{C3}R_L
\]  
(7.112)

where \( I_{C3} \) is the current in transistor \( Tr_3 \) and \( R_L \) is the load made up of \( R_4 \) in parallel with the input impedance of \( Tr_4 \). Since \( Tr_4 \) is in the emitter follower configuration, its input impedance is high and, therefore, does not significantly affect \( R_4 \). Hence, \( R_L \approx R_4 \).

### 7.11.3 Emitter Follower

The output stage of the amplifier consists of an emitter follower whose voltage gain \( A_{V3} \) is approximately one. It presents low output impedance and provides the amplifier with the ability to deliver current without loading down the amplifier and reducing the open-loop gain.

The overall gain \( A_V \) of the open-loop amplifier is given by the product of the open-loop gain of the three stages, i.e.,

\[
A_V = A_{V1} \times A_{V2} \times A_{V3}
\]

The closed-loop amplifier is shown in Fig. 7.40. The negative feedback being applied is voltage-series feedback as in the
non-inverting operational amplifier. For a sufficiently large open-loop gain, the closed-loop gain is given by

\[ A_V = 1 + \frac{R_6}{R_7} \]  

(7.113)

In order that the circuit be stable, a small capacitor must be placed from the collector of transistor \( Tr_3 \) to its base. This is called compensation and is discussed in Sect. 7.12.

**Example 7.11** Design a feedback amplifier with a closed-loop gain of 10 using the configuration shown in Fig. 7.40. Use small signal transistors having \( h_{fe} = 100 \) and a ±25-V supply. Justify all steps in your design. Calculate the open-loop voltage gain of your amplifier.

**Solution** Let the current in \( Tr_1 \) and \( Tr_2 \) be 0.5 mA. This is a reasonable current that results in good transistor frequency response and current gain. This results in 1 mA flowing through resistor \( R_2 \). The voltage at the base of \( Tr_1 \) is approximately 0 V and hence

\[ R_2 = \frac{25 - 0.7}{1\text{mA}} = 24.3 \text{ k} \]  

The base current of \( Tr_1 \) flowing through \( R_1 \) is 0.5 mA/100 = 5 μA. Allowing a maximum 50 mV drop across \( R_1 \) gives

\[ R_1 = 50 \times 10^{-3}/5 \times 10^{-6} = 10 \text{ k} \]  

Since the base-emitter voltage of \( Tr_3 \) is across \( R_3 \), \( R_3 = 0.7/0.5 \text{ mA} = 1.4 \text{ k} \). The voltage at the output of the amplifier must be zero under quiescent conditions. The voltage at the base of \( Tr_4 \) is, therefore, 0.7 V. This gives the voltage drop across \( R_4 \) as

\[ 25 - 0.7 = 24.3 \text{ V} \]  

We choose a current 2 mA in \( Tr_3 \) which is somewhat higher than the currents in the differential stage. Then \( R_4 = 24.3/2 \text{ mA} = 12 \text{ k} \). In order to drive external loads, we choose an even larger current of 5 mA in \( Tr_4 \). Then \( R_5 = 25/5 \text{ mA} = 5 \text{ k} \). For a closed-loop gain of 10, we assume that the open-loop gain is sufficiently large such that the closed-loop gain is given by

\[ A_{VF} = 10 = 1 + R_7/R_6 \]  

For \( R_6 = 1 \text{ k} \) then \( R_7 = 9 \text{ k} \). In this design, a compensation capacitor between the collector and base of \( Tr_3 \) is generally needed for stability. Its value, which is likely
to be in the range 1–100 pF, is adjusted for a flat frequency response (Example 7.12).

The open-loop voltage gain is determined as follows: The voltage gain $A_{V1}$ of the differential stage is

$$A_{V1} = \frac{R_3/h_{ie3}}{2r_e},$$

where $r_e$ is associated with $Tr_1$ and $Tr_2$ and $h_{ie3}$ is associated with $Tr_3$. $r_e = 1/40I_C = 1/40 \times 0.5 = 50 \Omega$ and $h_{ie3} = 100/40 \times 2 \text{ mA} = 1.25 \text{ k}$. Therefore, $A_{V1} = \frac{1.4 \text{ k}/1.25 \text{ k}}{2 \times 50} = 10$.

The voltage gain $A_{V2}$ of the second and main voltage gain stage is given by $A_{V2} = 40I_C R_L$, where $I_C = 2 \text{ mA}$ and $R_L$ is the load resistance of $Tr_3$. This load is $R_4 = 12 \text{ k}$ in parallel with the input impedance of the emitter follower $Tr_4$. The input impedance of $Tr_4$ is higher than $h_{fe} R_5 = 100 \times 5 \text{ k} = 500 \text{ k}$. Therefore, $R_L = 12 \text{ k}/500 \text{ k} \approx 12 \text{ k}$ and $A_{V2} = 40 \times 2 \times 12 = 960$. Therefore, the open-loop gain of the amplifier is $A_V = A_{V1} A_{V2} = 10 \times 960 = 9600$. Using the complete formula,

$$A_{Vf} = \frac{A_V}{1+B_A} = \frac{9600}{1+0.1 \times 9600} = 9.99.$$ This is very close to 10 and, therefore, justifies our use of $A_{Vf} = 1 + R_7/R_6$.

The design of this amplifier is not complete. The circuit has at least three poles, each of which can introduce significant phase shift such that instability can occur upon application of feedback. Steps must, therefore, be taken to ensure that the system with feedback is stable. This is the subject of the next section.

### 7.12 Stability and Compensation

In a negative feedback amplifier with open-loop gain $A$ and feedback factor $\beta$, the closed-loop gain is given by $A_f = \frac{A}{1+B_A}$. If the magnitude of the loop gain $A\beta$ is very large, i.e., $|A\beta| \gg 1$, then $A_f \rightarrow 1/\beta$ which is the closed-loop low-frequency gain of an amplifier. This analysis is, however, generally inadequate since $A$ and sometimes $\beta$ are frequency dependent. This means that at certain frequencies $|A\beta|$ may not be very
much greater than unity. Under such circumstances, the situation needs to be further examined. Thus, the closed-loop gain becomes

\[ A_f(s) = \frac{A(s)}{1 + \beta(s)A(s)} \]  

(7.114)

For physical frequencies \( s = j\omega \) and the closed-loop gain takes the form

\[ A_f(j\omega) = \frac{A(j\omega)}{1 + \beta(j\omega)A(j\omega)} \]  

(7.115)

The loop gain now becomes \( A(j\omega)\beta(j\omega) \) which is a complex function that can be represented by its magnitude and phase

\[ A(j\omega)\beta(j\omega) = |A(j\omega)\beta(j\omega)|e^{j\phi(\omega)} \]  

(7.116)

where \( \phi(\omega) \) is the phase shift of a signal exiting the feedback network relative to a signal entering the amplifier. The stability of the closed-loop system depends on the loop-gain. If the magnitude of the loop-gain is unity and the phase shift is \( 180^\circ \), then

\[ |A(j\omega)\beta(j\omega)|e^{j\phi(\omega)} = 1 \cdot e^{-j180^\circ} = -1 \]  

(7.117)

Hence, the closed-loop gain becomes \( \frac{A(j\omega)}{1-1} \rightarrow \infty \). This suggests that the system will produce an output without an input and is, therefore, unstable. If the magnitude of the loop gain is less than one when \( \phi = -180^\circ \), the system will not sustain the output without an input and is stable. The difference in dB between unity loop gain corresponding to 0 dB and the loop gain value at \( \phi = -180^\circ \) is the Gain Margin which is the amount by which the gain can be increased before instability ensues. The difference between the phase at the frequency at which the loop gain magnitude is unity and \( \phi = -180^\circ \) is the Phase Margin. It is the amount by which the phase lag can be increased before exciting instability. Both of these parameters give an indication of the level of stability of the feedback system, the larger the values the greater the level of stability. They are illustrated in Fig. 7.41. Multistage feedback
amplifiers with several poles are all subject to instability because of the phase shift contribution of the various stages.

\[ |A\beta| \]

\[ \text{dB} \]

\[ f(180^\circ) \text{ Gain} \]

\[ f(180^\circ) \text{ Margin} \]

\[ \text{Phase Margin} \]

\[ \text{Fig. 7.41} \text{ Bode plot of amplifier loop gain} \]

A simple approach to investigating stability involves the separate construction of Bode plots for the amplifier transfer function \( A(j\omega) \) and the factor \( 1/\beta(j\omega) \) which represents the closed-loop gain for high-gain systems. Noting that

\[ 20 \log |A\beta| = 20 \log |A(j\omega)| - 20 \log \left| \frac{1}{\beta(j\omega)} \right| \]

(7.118)
we can see that the difference between the two graphs is actually the loop gain expressed in dB. Therefore, the stability of the feedback system can be assessed by determining the difference between the $|A|$ plot and the $|1/\beta|$ plot. For $|A\beta| = 1$, then $20 \log |A\beta| = 0$ and hence the point of intersection of the two curves corresponds to the point at which $|A\beta| = 1$. An example will illustrate the method:

Consider a three-pole amplifier whose open-loop transfer function is given by

$$A(j\omega) = \frac{10^5}{(1 + j\omega 10^3)(1 + j\omega 10^4)(1 + j\omega 10^5)}$$  \hspace{1cm} (7.119)

The magnitude $|A(j\omega)|$ at a frequency $f$ (Hz) is found from

$$|A(f)| = \frac{10^5}{|1 + j\frac{f}{10^3}| \cdot |1 + j\frac{f}{10^4}| \cdot |1 + j\frac{f}{10^5}|}$$  \hspace{1cm} (7.120)

while the phase $\phi$ is given

$$\phi = -\left[\tan^{-1}\left(f/10^3\right) + \tan^{-1}\left(f/10^4\right) + \tan^{-1}\left(f/10^5\right)\right]$$  \hspace{1cm} (7.121)

Consider a frequency-independent feedback factor $\beta$ that yields a closed-loop gain of $20 \log (1/\beta) = 85$ dB. Plots of $|A(j\omega)|$ and $|1/\beta|$ are shown in Fig. 7.42. At the point of intersection of the curves, the frequency is $1.6 \text{ kHz}$ and the phase angle is $-108^\circ$. Therefore, at a gain of $85$ dB, the phase margin is $180^\circ - 108^\circ = 72^\circ$ and the amplifier is stable. The gain margin can be found by finding the difference between the $|1/\beta|$ plot (at the intersection point) and the value of the $|A|$ plot at $\phi = -180^\circ$. Since the open-loop gain at which the phase is $-180^\circ$ is approximately $60$ dB, it follows that the gain margin is $85$ dB $- 60$ dB $= 25$ dB. For a closed-loop gain of $50$ dB, $\phi < -180^\circ$ at the point of intersection and, therefore, the amplifier is unstable.
It is possible to determine the minimum closed-loop gain for a stable amplifier. It is given by the intersection point at which $\phi = -180^\circ$. This represents a theoretical stability limit and not a practical limit since phase angles of less than this limit for decreasing gains result in decreasing levels of stability manifested as humps in the closed-loop response as shown in Fig. 7.43.
It can be shown that a phase shift approaching \(-180^\circ\) will only occur on the \(-40\, \text{dB/dec}\) segment of the \(|A|\) plot, and hence, instability can be avoided by the following simple rule: The feedback amplifier will be stable if the \(20 \log |1/\beta|\) curve intersects the \(20 \log |A|\) curve at a \(-20\, \text{dB/dec}\) segment. This results in a phase margin of approximately \(45^\circ\), a value considered acceptable for a stable amplifier. In the case, where \(\beta\) is also frequency dependent, the rule becomes the feedback amplifier will be stable providing the relative slopes of the \(20 \log |1/\beta|\) and the \(20 \log |A|\) curves at the point of intersection does not exceed \(-20\, \text{dB/dec}\).

### 7.12.1 Compensating Feedback Amplifiers

As we discussed, a multipole amplifier is increasingly likely to be unstable as the closed-loop gain is reduced. In order to ensure stability of the closed-loop system with acceptable levels of frequency response peaking, the magnitude and phase responses of the open-loop amplifier and the feedback network can be adjusted such that \(\phi < -180^\circ\) when \(|A\beta| = 1\) or alternatively that \(|A\beta| < 1\) when \(\phi = -180^\circ\). This process is referred to as *Compensation*. The three methods to be discussed are

\[ \text{(1)} \]
dominant pole compensation, (2) miller compensation, and (3) lead compensation.

### 7.12.2 Dominant Pole Compensation

This is perhaps the simplest method and involves the introduction of a pole at a frequency that is lower than all the system poles such that the effects of these poles on the open-loop magnitude response is minimal and, therefore, the changed open-loop gain response intersects the closed-loop plot at a relative slope of −20 dB/dec. In order to illustrate the method, consider the open-loop 20 log |A| response of Fig. 7.44 having three poles at $f_{p1}, f_{p2},$ and $f_{p3}$ and a closed 20 log |1/β| plot as shown. The |1/β| plot intersects the |A| plot at a slope greater than −20 dB/dec, and our rule-of-thumb for a stable feedback amplifier is not satisfied. In order to correct this, a new pole is introduced at the maximum frequency $f_1$ that causes the intersection of the changed |A| and the |1/β| plot at a relative slope of −20 dB/dec and at a frequency before the effect of the lowest pole at $f_{p1}$ (curve a). The closed-loop amplifier is now stable. For general purpose, operational amplifiers that must be stable for all values of feedback (unity-gain stable), the pole at $f_1$ would have to be moved to $f_D$ so that the modified plot intersects the 0 dB line at −20 dB/dec (curve d). The advantage of this method is its simplicity, but its disadvantage is that gain across the frequency spectrum is reduced and, therefore, less feedback is available at these frequencies.
A better approach to compensating a feedback amplifier is to create the dominant pole by shifting the pole at the lowest frequency $f_{p1}$ to a lower frequency rather than introducing a new one. Thus, we can move the first pole at $f_{p1}$ to a frequency $f_2$ such that the effect of the next lowest pole at $f_{p2}$ is avoided before intersection with the $|1/\beta|$ plot (curve b). As can be seen in Fig. 7.44, the new $|A|$ plot intersects the $|1/\beta|$ plot at $-20$ dB/dec, but the resulting dominant pole frequency $f_2$ is greater than the previous dominant pole frequency $f_1$ making more negative feedback available across the frequency range. For the circuit shown in Fig. 7.45, the lowest frequency pole is set at node A and is given by $f_{p1} = 1/2\pi R_A C_A$. Here, $R_A$ is the total resistance between node A and the emitter of $Tr_3$ which is approximately $R_3/h_{ie3}$ and $C_A$ is primarily made up of the base-emitter capacitance of $Tr_3$. The pole-shifting technique can be implemented by introducing a capacitor $C_C$ across the base-emitter junction of $Tr_3$ as shown. The adjusted pole is now at $f_2 = 1/2\pi R_A(C_A + C_C)$. 

*Fig. 7.44* Gain-frequency plot for three compensating methods
Fig. 7.45 Amplifier with dominant pole compensation

7.12.3 Miller Compensation

A second method of compensation that is superior to the first is Miller compensation. It is implemented by placing a capacitor $C_f$ between the collector and base of $Tr_3$ in Fig. 7.46. A simplified equivalent circuit of the input and output of transistor $Tr_3$ is shown in Fig. 7.46. Here, $R_A$ and $C_A$ are the total resistance and capacitance between node A and ground, and $R_B$ and $C_B$ are the total resistance and capacitance between node B and ground. Without the compensation capacitor $C_f$ the poles created by the transistor are
With the introduction of $C_f$, the transfer function from the input of $Tr_1$ to the output of $Tr_3$ becomes

\[
\frac{V_o}{V_i} = g_{m1} \frac{(g_{m2} - sC_f)R_A R_B}{1 + s \left[ C_A R_A + C_B R_B + C_f (g_{m2} R_A R_B + R_A + R_B) \right] + s^2 \left[ C_A C_B + C_f (C_A + C_B) \right] R_A R_B}
\]  

(7.123)

where $g_{m1}$ is the transconductance of the differential stage and $g_{m2}$ is the transconductance of the second stage. The zero in this transfer function is located at a frequency $f_z = g_{m2}/2\pi C_f$ which for typical transistor parameters is generally at a high frequency and away from the main system poles. Considering the denominator polynomial and noting that it is second-order, it can be approximated by

(7.124)
where $\omega'_{p1}$ and $\omega'_{p2}$ are the representative poles of the system. One pole is usually dominant, i.e., $\omega'_{p1} \ll \omega'_{p2}$. Therefore, $D(s)$ becomes

$$D(s) \approx 1 + \frac{s}{\omega'_{p1}} + \frac{s^2}{\omega'_{p1} \omega'_{p2}}$$  \hspace{1cm} (7.125)

Comparing the denominator of (7.123) and (7.125) and equating coefficients yields

$$f'_{p1} = \frac{1}{2\pi \left[ C_A R_A + C_B R_B + C_f (g_{m2} R_A R_B + R_A + R_B) \right]} \approx \frac{1}{2\pi g_{m2} R_B C_f R_A}$$
$$f'_{p2} \approx \frac{g_{m2} C_f}{C_A C_B + C_f (C_A + C_B)}$$ \hspace{1cm} (7.126)

An increase in $C_f$ reduces $f'_{p1}$ but increases $f'_{p2}$. This effect is called pole-splitting and allows movement of $f'_{p1}$ to a dominant frequency while also moving $f'_{p2}$ to a higher frequency away from the first pole as shown in Fig. 7.47 (curve c).

**Fig. 7.47** Gain-frequency plot showing miller compensating method (curve c)
The overall effect is that the available compensated open-loop gain is increased. It should also be noted in (7.126) that the capacitance \( C_f \) has effectively been multiplied by the Miller-effect factor \( g_{m2}R_B \) which is the low-frequency gain of the stage. The effect overall is the increase of the value of the capacitance in parallel with \( R_A \) to \( C_f' = g_{m2}R_B C_f \) such that \( f_{p1}' \) can be written as \( f_{p1}' = 1/2\pi C_f' R_A \). The capacitance \( C_f \) therefore, need not be very large and is usually much smaller than the value \( C_c \) used in the pole-shifting method of compensation applied at node A in Fig. 7.45.

In order to determine the value of \( C_f \) needed to compensate a particular amplifier, we note that (7.123) can be written as

\[
\frac{V_o(s)}{V_i} = \frac{g_{m1}R_A g_{m2}R_B \left(1 - \frac{s C_f}{g_{m2}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}
\]  
(7.127)

At frequencies close to the dominant pole, frequency (7.127) becomes

\[
A(s) = \frac{V_o(s)}{V_i} \approx \frac{g_{m1}R_A g_{m2}R_B}{\left(1 + \frac{s}{\omega_{p1}}\right)}
\]  
(7.128)

The magnitude of this transfer function using (7.126) is

\[
|A(j\omega)| = \frac{g_{m1}R_A g_{m2}R_B}{\omega_{p1}} = \frac{g_{m1}R_A R_B}{\omega g_{m2}R_B C_f R_A} = \frac{g_{m1}}{\omega C_f}
\]  
(7.129)

At the frequency \( \omega_T \) where the \( |1/\beta| \) curve intersects the \( |A| \) curve, we have \( |A(\omega_T)\beta| = 1 \) and therefore

\[
\frac{\beta g_{m1}}{\omega_T C_f} = 1
\]  
(7.130)

This gives

\[
(7.131)
Example 7.12  Consider the amplifier circuit in Fig. 7.45 with an open-loop transfer function corresponding to Eq. (7.123). The objective is to compensate the amplifier so that the closed-loop amplifier with resistive feedback is unity-gain stable, i.e., it is stable for all values of $\beta$ up to the maximum value of unity. The second stage $Tr_3$ has $C_A = 1000$ pF, $C_B = 10$ pF, and $g_m = 40$ mA/V. It is assumed that the pole at $f_{p1}$ is associated with the input of $Tr_3$ and the pole at $f_{p2}$ is introduced by the output of $Tr_3$.

Solution  Using $f_{p1} = 10^4 = \frac{1}{2\pi C_A R_A}$ gives

$$R_A = \frac{1}{10^4 \times 2\pi \times 1000 \times 10^{-12}} = 15.9 \text{ k}.$$ For $f_{p2} = 10^5$ then $10^5 = \frac{1}{2\pi C_B R_B}$ gives

$$R_B = \frac{1}{10^5 \times 2\pi \times 10 \times 10^{-12}} = 159 \text{ k}.$$ Using dominant pole compensation by introducing capacitor $C_C$ across the base-emitter junction of $Tr_3$ means that the pole at $f_{p1}$ is moved to a new frequency $f_D$ given by

$$f_D = \frac{1}{2\pi R_A (C_A + C_C)}.$$ In order to determine the actual frequency $f_{D'}$, a line of slope $-20 \text{ dB/dec}$ is drawn backwards from the 0 dB gain at frequency $f_{p2} = 10^5$ and the frequency at which it intersects the open-loop characteristic is noted. In this case the intersection occurs at 1 Hz. Thus, $f_D = 1 = \frac{1}{2\pi R_A (C_A + C_C)}$ yields $C_C = 0.009 \mu F$. Instead of dominant pole compensation, Miller compensation can be used by adding capacitor $C_f$ across the collector-base junction of $Tr_3$. This results in new poles at

$$f'_{p1} \approx \frac{1}{2\pi g_m R_B C_f R_A}$$

and

$$f'_{p2} \approx \frac{g_m C_f}{C_A C_B + C_f(C_A + C_B)}.$$ Let $f'_{p1}$ coincide with the third system pole at $f_{p3} = 10^6$ Hz. Then in order to determine the frequency $f'_{p1}$, a line of slope $-20 \text{ dB/dec}$ is drawn backwards from the 0 dB gain at frequency $f_{p3} = 10^6$ and the frequency
at which it intersects the open-loop characteristic is noted. This turns out to be \( f_p' = 10 \text{ Hz} \). Hence, \( f_p' \approx \frac{1}{2 \pi g_{m2} R_B C_f R_A} = 10 \) giving \( C_f = 157 \) pF. Then \( f_p' \approx \frac{g_{m2} C_f}{C_\text{A} C_\text{B} + C_f (C_\text{A} + C_\text{B})} = 37 \text{ MHz} \) which exceeds \( f_{p3} = 10^6 \text{ Hz} \).

Example 7.13 Calculate the compensation capacitor \( C_f \) for the design in Example 7.10.

Solution For the circuit of Example 7.10, \( r_e = 1/40 \times 0.5 \text{ mA} = 50 \Omega \) and \( A_V = 10 \). Therefore, for \( f_c = 20 \text{ MHz} \), the capacitor \( C_f \) is given by

\[
C_f = \frac{g_m}{2 \pi A_V f_c} = \frac{1}{2 r_e \times 2 \pi \times 20 \text{ MHz}} = 79.5 \text{ pF}.
\]

7.12.4 Lead Compensation
The two methods discussed thus far all involve modifying the shape of the forward transfer function \( A \) in order to achieve the desired \( A\beta \) response. The shape of \( A\beta \) can also be influenced by modifying the beta network response using appropriate reactive elements and thereby achieve compensation. One such method is called lead compensation. It operates by the introduction of leading phase in the feedback network \( \beta \) designed to reduce the amount of phase lag caused by the forward network \( A \). In the case of a voltage amplifier, lead compensation can be implemented by the placement of a capacitor \( C \) across the feedback resistor as shown in Fig. 7.48. Experimental adjustment of the value to maximize bandwidth while minimizing frequency response peaking is a simple approach to utilizing the technique.
7.13 Three-Transistor Feedback Amplifier

The three-transistor circuit shown in Fig. 7.49 is another useful voltage amplifier configuration. It is a single-ended design that requires capacitor coupling. The first stage is a common emitter amplifier that provides modest gain. Emitter resistor $R_1$ is included to allow the application of voltage-series feedback around the amplifier. The second stage is another common emitter amplifier which provides the main voltage gain. Resistor $R_6$ is a feedback loop that provides DC bias to $Tr_1$. The loop is disabled at medium and high frequencies by capacitor $C_2$. The final stage is an emitter follower that prevents loading of $R_4$ and gives the amplifier a low-impedance output. Resistor $R_7$ along with $R_1$ is the overall feedback loop. Capacitor $C_3$ is necessary for DC blocking in the feedback loop. $C_1$ and $C_4$ are coupling capacitors and $C_5$ is required for stability.
Example 7.14  Design a transistor amplifier with a gain of 10 using the configuration of Fig. 7.49. Use a 30 V supply and transistors with current gain of 100.

Solution  We choose currents of 1 mA for \( Tr_1 \), 2 mA for \( Tr_2 \), and 5 mA for \( Tr_3 \). We also select \( R_1 = 220 \) Ω. This resistor should not be too large otherwise the gain of this first stage would be unduly reduced and it should be large enough to accommodate the negative feedback implementation. The design starts at stage 2 where the voltage swing is greatest. For bias stability, let the voltage at the emitter or \( Tr_2 \) be about one tenth of the supply voltage giving 3 V. Hence, \( R_3 = 3/2 \) mA = 1.5 k. For maximum symmetrical swing in \( Tr_2 \), \( R_4 = \frac{(30-3)/2}{mA} = 6.75 \) k. Using Kirchhoff’s voltage law around the internal feedback loop,

\[ 3 = I_{B1}R_6 + 0.7 + I_{C1}R_1, \]

where \( I_{B1} \) and \( I_{C1} \) are the base and collector currents of \( Tr_1 \). Using \( I_{B1} = 1 \) mA/100 = 0.01 mA, \( I_{C1} = 1 \) mA and \( R_1 = 220 \) Ω we get \( R_6 = 208 \) k. Since the emitter of \( Tr_2 \) is at 3 V, the
collector of \( Tr_1 \) is 3.7 V. Hence, \( R_2 = (30 - 3.7)/1 \text{ mA} = 26.3 \text{ k} \). The voltage at the collector of \( Tr_2 \) is \( 3 + 13.5 = 16.5 \text{ V} \). At the output stage, the emitter of \( Tr_3 \) is \( 16.5 - 0.7 = 15.8 \text{ V} \). Hence, \( R_5 = 15.8/5 \text{ mA} = 3 \text{ k} \).

The open-loop gain of the amplifier is the product of the gain of the two common emitter stages. The voltage gain of the first stage is \( A_v(Tr_1) = -R_2/h_{ie2}/(R_1 + r_e) \), where

\[
h_{ie2} = h_{fe2}/40I_{C2} = 100/40 \times 2 \text{ mA} = 1.25 \text{ k}
\]

and

\[
r_e = 1/40I_{C1} = 25 \text{ } \Omega.
\]

Hence, \( A_v(Tr_1) = -4.8 \). For the second stage,

\[
A_v(Tr_2) = 40I_{C2}R_4 = -540
\]

from which the overall open-loop gain is

\[
(4.8 \times 540) = 2592.
\]

This reasonably high open-loop gain results in a closed-loop gain given by \( A_{vf} = 1 + R_7/R_1 \). Hence, designing for a gain of 10, \( 10 = 1 + R_7/220 \) giving \( R_7 = 2 \text{ k} \). Capacitor \( C_5 \) is given by

\[
C_5 = \frac{g_m}{2\pi f_c A_v}
\]

where \( g_m = 1/(r_e(Tr_1) + R_1) = 1/(25 + 220) = 1/245 \). Using \( f_c = 3 \text{ MHz} \) and \( A_v = 10 \),

\[
C_5 = \frac{1}{245 \times 2\pi \times 3 \times 10^6 \times 10} = 22 \text{ pF}.
\]

### 7.14 Applications

Several applications of circuits involving the negative feedback principle are presented and discussed.

#### 7.14.1 Three-Transistor Preamplifier

The circuit in Fig. 7.50 is another three-transistor preamplifier configuration. The first stage is a common emitter amplifier using an npn transistor. The output of this stage is directly coupled to the input of the second stage which is also a common emitter configuration. This, however, uses a pnp transistor. The output of this second stage is also directly coupled to the output stage which is a common collector amplifier using an npn transistor. Resistor \( R_7 \) provides DC feedback that establishes quiescent current stability throughout the system. This feedback is reduced for signals since resistor \( R_6 \) is connected from the emitter of \( Tr_1 \) to ground for signals via \( C_3 \). It is evident that this feedback arrangement is voltage-series feedback and hence, for
sufficiently high open-loop gain, the closed-loop gain of the system for signals is $1 + R_7/R_6$. $C_4$ is the Miller compensation capacitor. Because of the DC feedback loop from the output to the emitter of $Tr_1$, it is convenient to start the design process for this circuit at the output.

![Three-transistor preamplifier](image)

**Fig. 7.50** Three-transistor preamplifier

Let the currents be 0.5 mA in $Tr_1$, 1 mA in $Tr_2$, and 4 mA in $Tr_3$. For a 20-V supply, let the emitter of $Tr_3$ be 10 V for maximum symmetrical swing. Hence, noting that the collector current of $Tr_1$ and $Tr_3$ flow into $R_5$, then $R_5 = 10V/(4 + 0.5)\ mA = 2.2\ k$. The voltage at the base of $Tr_3$ which is connected to the collector of $Tr_2$ is 10.7 V. Hence, $R_4 = 10.7\ V/1\ mA = 10.7\ k$. Since the current in $Tr_1$ is 0.5 mA, $R_3 = 0.7\ V/0.5\ mA = 1.2\ k$. Resistor $R_6$ which forms part of the signal feedback loop must not be too large as it will unduly limit the gain of this stage. A value of 220 $\Omega$ is selected. If the circuit has to have a closed-loop gain of 11, then $R_7 = 2.2\ k$. Since the collector current of $Tr_1$ flows through $R_7$
into $R_5$, the voltage drop across $R_7$ is 2.2 V. The base voltage of $Tr_1$ is then $10 + 2.2 + 0.7 = 12.9$ V. For quiescent current stability, let the current through $R_1$ and $R_2$ be 0.1 mA. Then $R_2 = 12.9 \text{ V/0.1 mA} = 129 \text{ k}$ while $R_1 = (20 - 12.9)/0.1 \text{ mA} = 71 \text{ k}$. From Eq. (7.131), the value of the compensation capacitor is given by $C_5 = \frac{g_m}{2\pi f_c A_V}$, where

$$g_m = \frac{1}{(r_e(Tr_1) + R_6) = 1/(25 + 220) = 1/245.}$$

Using $f_c = 3 \text{ MHz}$ and $A_V = 11$, $C_5 = \frac{1}{245 \times 2 \pi \times 3 \times 10^6 \times 10} = 22 \text{ pF}$.

**Ideas for Exploration**: (i) Use the bootstrapping technique to increase the input impedance of the amplifier. (ii) Use the bootstrapping technique to increase the gain of the second stage.

### 7.14.2 DC Voltmeter Using Differential Amplifier

The circuit of a DC voltmeter is shown in Fig. 7.51. It uses a differential amplifier at the input followed by a pnp Darlington pair such as the MPSA65 in the common emitter mode. The differential amplifier provides modest gain while the Darlington pair produces higher gain. The meter is placed in a feedback loop around the amplifier such that the current through the meter is defined by the input voltage and a resistor value. Thus, the meter current $I_m$ develops a voltage $V_x = I_m R_{10}$, ($VR_C = 0$) at the inverting input which is subtracted from the input voltage $V_i$ at the non-inverting input giving an error signal ($V_i - V_x$).

This error signal is multiplied by the amplifier open-loop gain $A$ giving an output $V_o = A(V_i - V_x)$. Providing the open-loop gain $A$ of the system is large, the difference is minimized by the feedback loop such that $I_m = V_i/R_{10}$. 


Current through the Darlington pair is set at 0.5 mA giving $R_{11} = 1.5 \text{ V}/0.5 \text{ mA} = 3 \text{ k}$, while that through the differential pair is set at 100 μA giving $R_9 + VR_Z \approx 1 \text{ V}/0.1 \text{ mA} = 10 \text{ k}$. Use $R_9 = 8.2 \text{ k}$ and potentiometer $VR_Z = 5 \text{ k}$ which is varied to zero the meter. Each transistor in the pair passes 50 μA. These low currents ensure that the system can be operated from penlight batteries over a long period before battery replacement. The voltage across the base-emitter junction of the MPSA65 at 0.5 mA is about 1 V, and hence $R_8 = 1 \text{ V}/0.05 \text{ mA} = 20 \text{ k}$. Full-scale deflection of the meter must occur for an input voltage of 100 mV. Hence, $100 \text{ mV}/(R_{10} + VR_C) = 100 \text{ μA}$ giving $R_{10} + VR_C = 1 \text{ k}$. Set $R_{10} = 680 \text{ Ω}$ and potentiometer $VR_C = 1 \text{ k}$ which is used to calibrate the meter. The upper ranges of 0.3 V, 1 V, 3 V, 10 V, 30 V, and 100 V require input resistors $R_1 = 20 \text{ k}$, $R_2 = 90 \text{ k}$, $R_3 = 290 \text{ k}$, $R_4 = 1 \text{ M}$, $R_5 = 3 \text{ M}$, $R_6 = 10 \text{ M}$ as shown. These in conjunction with $R_7 = 10 \text{ k}$ will attenuate the input voltages such that 100 mV will appear at the input to the differential amplifier on each range.
Ideas for Exploration: (i) Explain the mechanism whereby $VR_Z$ can zero the meter and $VR_C$ can be used to calibrate the meter. (ii) Modify the circuit so that it can measure ac signals by placing the meter in a diode bridge.

7.14.3 RIAA Preamplifier

The signal from a phonograph disk (record) has a characteristic in which the high frequencies have a higher amplitude than the low frequencies. Because of this, the preamplifier for such a signal must possess a frequency response characteristic that is exactly the inverse of this. This means that the amplifier must have a higher gain for low frequencies and a lower gain for high frequencies. The Record Industry Association of America (RIAA) has developed a standard for magnetic phonograph cartridges that establishes the exact nature of this equalization characteristic. This is shown in Fig. 7.52 where two poles and one zero are indicated.

![RIAA equalization curve](image)

Fig. 7.52 RIAA equalization curve

The poles are at 50 and 2100 Hz and the zero is at 500 Hz. A practical implementation of this is shown in Fig. 7.53. It is based on the three-transistor preamplifier of Sect. 7.13 with a CR network in the
signal feedback loop which creates the RIAA equalization characteristic. The design of the network is algebraically quite tedious. The values given in the diagram achieve close adherence to the required curve. The standard input resistance for magnetic pickups is 47 k as achieved in the diagram.

![RIAA Preamplifier Circuit Diagram](image)

**Fig. 7.53** RIAA preamplifier


**7.14.4 JFET-BJT Preamplifier**
A circuit for a preamplifier using a JFET at the input is shown in Fig. 7.54. This configuration is similar to the three BJT circuit except that the input BJT is replaced by a JFET. This gives the circuit a very high input impedance. The JFET is connected in the common source mode. The output drives $Tr_2$ which is a pnp BJT in the common emitter mode while the final stage is an emitter follower to buffer the second stage and also provide a low-impedance output. The circuit uses a bipolar supply which of course enhances the available output voltage swing. Resistor $R_1 = 10 \text{ M}$ connects the gate to ground and enables $Tr_1$ to be self-biased. Resistor $R_7$ provides DC feedback that establishes quiescent current stability throughout the system. This feedback is reduced for signals since resistor $R_6$ is connected from the source of $Tr_1$ to ground for signals via $C_3$. This feedback arrangement is voltage-series feedback and hence, for sufficiently high open-loop gain, the closed-loop gain of the system for signals is $1 + R_7/R_6$. $C_4$ is the Miller compensation capacitor. Because of the DC feedback loop from the output to the source of $Tr_1$, the design process for this circuit starts at the output.
Let the currents be 0.5 mA in $Tr_1$, 1 mA in $Tr_2$, and 3 mA in $Tr_3$. For a ±9 V supply, let the emitter of $Tr_3$ be 0 V for maximum symmetrical swing. Then, noting that the bias currents of the JFET and the emitter follower flow into $R_5$, the value of this resistor is given by $R_5 = 9 \, \text{V}/3.5 \, \text{mA} = 2.6 \, \text{k}$. The voltage at the base of $Tr_3$ which is connected to the collector of $Tr_2$ is 0.7 V. Hence, $R_3 + R_4 = 9.7/1 \, \text{mA} = 9.7 \, \text{k}$. Since the current in $Tr_1$ is 0.5 mA, $R_2 = 0.7 \, \text{V}/0.5 \, \text{mA} = 1.2 \, \text{k}$. From Shockley’s equation, for a drain current of 0.5 mA in $Tr_1$, $V_{GS} = -3 \, \text{V}$. Hence, $R_7 = 3/0.5 \, \text{mA} = 6 \, \text{k}$. If the circuit has to have a closed-loop gain of 11, then $R_6 = 600 \, \Omega$. This value of resistor $R_6$ which forms part of the signal feedback loop limits the gain of this stage. This is overcome by
bootstrapping resistor $R_3$ with capacitor $C_5$ which increases the value of $R_3$ for signals thereby increasing the gain of $Tr_2$. From Eq. (7.131), the value of the compensation capacitor is given by

$$C_5 = \frac{g_m}{2\pi f_c A_V},$$

where

$$g_m = 1/(1/g_m(Tr_1) + R_6) = 1/(100 + 600) = 1.4 \times 10^{-3}$$

and

$$g_m(Tr_1) = 10 \text{ mA/V is used. Using } f_c = 2 \text{ MHz and } A_V = 11,$$

$$C_5 = \frac{1}{245 \times 2 \pi \times 3 \times 10^6 \times 10} = 22 \text{ pF}.$$

_Ideas for Exploration:_ (i) Replace the bootstrapping arrangement in the collector of $Tr_2$ by a constant current source.

### 7.14.5 AC Millivoltmeter

The circuit shown in Fig. 7.55 is that of a wide-band AC millivoltmeter for the measurement of signals in the millivolt range. It uses two common emitter amplifiers so that the sensitivity of the system exceeds that of the single transistor configuration discussed in Chap. 4. The input transistor $Tr_1$ is bootstrapped and, therefore, provides a high-input impedance to the circuit. This stage drives a common emitter amplifier $Tr_2$, the collector of which is directly coupled to a second common emitter amplifier around $Tr_3$. The microammeter along with a bridge rectifier is included in a feedback loop connected to the emitter of $Tr_2$. The first stage design follows the bootstrapped emitter follower Example 4.10. Using a 9V supply, let the bias voltage at the emitter of $Tr_2$ be 1 V. For a collector current of 0.5 mA, $R_6 = 1/0.5 \text{ mA} = 2 \text{ k}$. Since this stage precedes the output stage where there is further amplification, maximum symmetrical swing is not required. Allowing 2 V across $Tr_2$ for proper operation, the remaining voltage dropped across $R_5$ is 6 V. Hence, $R_5 = 6 \text{ V}/0.5 \text{ mA} = 12 \text{ k}$. The voltage at the collector of $Tr_2$ is 3 V and, therefore, the voltage across $R_8$ is 2.3. Selecting 1 mA quiescent current in $Tr_3$, then $R_8 = 2.3/1 \text{ mA} = 2.3 \text{ k}$. For maximum symmetrical swing in $Tr_3$, the voltage across $R_7$ is $(9 - 2.3)/2 = 3.4 \text{ V}$. Hence, $R_7 = 3.4 \text{ V}/1 \text{ mA} = 3.4 \text{ k}$. The voltage at the emitter of $Tr_3$ is 2.3 V and the voltage at the base of $Tr_2$ is 1.7 V. The base current of $Tr_2$ is 0.5 mA/100 = 0.005 mA. Therefore, the DC
feedback resistor \( R_9 = (2.3 - 1.7)/0.005 \text{ mA} = 120 \text{ k.} \) Because of the AC feedback through the meter to the emitter of \( Tr_2 \), resistor \( R_{10} = 10 \text{ mV/100} \mu\text{A} = 100 \Omega \). Resistor \( R_{10} \) should be a potentiometer that is adjusted to give full-scale deflection for an input of 10 mV.

![AC millivoltmeter circuit diagram](image)

**Fig. 7.55** AC millivoltmeter

*Ideas for Exploration:* (i) Introduce an attenuator similar to that used in other meter projects to extend the range of this instrument to 100 V.

### 7.14.6 Video Amplifier

This circuit utilizes wideband stages to achieve video frequency amplification (Fig. 7.56). Thus, the input stage is a differential amplifier in which the first stage functions in the emitter follower mode while the second is in the common base mode. The output stage is another emitter follower. In addition to these wideband stages, the system has feedback from output to the inverting input. The result is very
wideband operation. With a 15 V supply, using $R_1 = 12 \, k$ and $R_2 = 4.7 \, k$ sets the voltage at the base of $Tr_1$ at 4.2 V. Let the current in each transistor in the differential pair be 1.5 mA for good high-frequency response. Then $R_3 = (4.2 \, - \, 0.7)/3 \, mA = 1.2 \, k$. Since the base voltage of $Tr_2$ is about 4.2 V, the maximum peak-to-peak swing available at $Tr_3$ is approximately $(15 \, - \, 4.2)/2 = 5.4 \, V$. Hence, for maximum symmetrical swing in $Tr_2$, $R_4 = 5.4/1.5 \, mA = 3.6 \, k$. In order to drive transmission lines which typically have characteristic impedances of between 50 and 300 $\Omega$, let the current in the emitter follower output stage be 10 mA. The voltage at the base of $Tr_3$ is $(15 \, - \, 5.4) = 9.6 \, V$, and, therefore, the resistance in the emitter of this transistor is $8.9/10 \, mA = 890 \, \Omega$. In order to get 4.2 V at the base of $Tr_2$, for $R_6 = 470 \, \Omega$ then $R_5 = 520 \, \Omega$. The closed-loop gain of the system is set by $1 + R_5/R$, where $R$ is the value of $VR_1 = 1 \, k$ added to the value of $R_7 = 47 \, \Omega$, in parallel with $R_6$. At a gain of 17 dB, the simulated circuit had a bandwidth of 11 MHz. All capacitors need to be large.
Ideas for Exploration: (i) Try to increase the bandwidth of the system by selecting suitable high-frequency transistors that have low junction capacitances.

7.14.7 Research Project 1
The circuit shown in Fig. 7.57 is that of an audio compressor or constant volume amplifier. It provides a near constant amplitude output signal for widely varying input signal amplitude by incorporating automatic gain control. Such a circuit is useful in reducing the dynamic range of music signals in order to enable better processing of these signals particularly in the recording industry. The first stage is an emitter follower that is biased for maximum symmetrical swing. The second
stage is a JFET that is used as a voltage-controlled resistor. With a 15 V supply, the drain of this JFET is set at approximately 2 V by resistors $R_4$ and $R_5$ which form a potential divider. Resistor $R_6 = 220 \, k$ grounds the gate of the JFET and $R_7 = 2.2 \, k$ along with the drain voltage set the drain current which positions the operating point in the ohmic region. The drain-source resistance in conjunction with $R_7$ provides the dynamic adjustment that results in automatic gain control. The output at the source of the FET drives the common emitter amplifier $Tr_3$ while the emitter follower $Tr_4$ buffers the final output. These latter two stages follow standard design procedure. The output of $Tr_4$ is rectified by diode $D_1$ on the negative half-cycle, the positive half-cycle going to ground via $D_2$. $R_{11}$ and $C_6$ filter this rectified signal and apply a negative voltage at the gate of the JFET. Thus, for large amplitude signals, the amplitude of this negative voltage increases and this increases the drain-source resistance of the JFET, as a result of which the signal across $R_7$ and hence the output signal is reduced. The converse occurs for a reduced output.

![Fig. 7.57 Audio compressor](image-url)
**Ideas for Exploration:** (i) Determine the dynamic range of the circuit by applying a signal of increasing amplitude and recording the corresponding output amplitude changes. A large input signal amplitude change will produce a reduced amplitude change at the output. (ii) Experiment with different values of $R_{11}$ and $C_6$ and determine the response of the circuit to these changes.

### 7.14.8 Research Project 2

A common problem when playing old records is scratches on the vinyl surface which generate high-frequency noise. This project involves the design of a *scratch filter* to remove this noise. (An introduction to active filters is presented in Chap. 11) The basic system is shown in Fig. 7.58. It comprises two connected RC networks with one capacitor grounded and the other connected to the output of the buffer. The transfer function for this system with $R_1 = R_2 = R$ and $C_1 = C$, $C_2 = 2C$ is given by

$$\frac{V_o}{V_i} = \frac{1}{1 + \sqrt{2} \frac{f_c}{f_c} + \left(\frac{f_c}{f_c}\right)^2}$$

(7.132)

where

$$f_c = \frac{1}{2 \sqrt{2} \pi RC}$$

(7.133)

![Basic System](image1.png)

![Circuit Implementation](image2.png)

*Fig. 7.58* Scratch filter

This is a second-order response referred to as a Butterworth response that has the characteristic of being maximally flat. The roll-off
rate is −40 dB/dec. With an appropriately placed corner frequency $f_c$, unwanted high-frequency signals produced by vinyl scratches can be eliminated. The circuit implementing this approach is shown in Fig. 7.58 which uses a bipolar supply of ±15 V. Here, an emitter follower is the active buffer. Base bias is provided by $R_B = 120$ k and $R_E = 15$ k sets the quiescent current at about 1 mA. For an upper cut-off frequency of 10 kHz, using $C = 2.2$ nF, Eq. (7.133) gives $R = 4.7$ k.

Ideas for Exploration: (i) Use a feedback pair in place of the single transistor. This will allow an even larger value for $R_B$ and also gain can be introduced.

### 7.14.9 Research Project 3

Using this single transistor configuration, explore the development of a rumble filter that removes unwanted low-frequency (less than 50 Hz) components from an audio signal. The two filter network resistors and the two network capacitors in Fig. 7.58 must be interchanged. Also, $R_B$ would not now be necessary as base bias would be provided by the filter network resistor $R_1$. The basic system is shown in Fig. 7.59 and the associated transfer function with $C_1 = C_2 = C$ and $R_1 = R$, $R_2 = R/2$ is given by

\[
\frac{V_o}{V_i} = \frac{(j\frac{f}{f_c})^2}{1 + \sqrt{2}j\frac{f}{f_c} + (j\frac{f}{f_c})^2}
\]  

(7.134)

where the corner frequency is

\[
f_c = \frac{\sqrt{2}}{2\pi RC}
\]  

(7.135)
This is a Butterworth response for the high-pass filter. For a lower cut-off frequency of 50 Hz, using \( C = 1 \mu F \), Eq. (7.135) gives \( R = 4.5 \, k \).

Idea for Exploration: (i) Use a feedback pair in place of the single transistor. This enables gain to be introduced.

7.14.10 Research Project 4

A tone control circuit adjusts the amplitude of high (treble) and low (bass) frequencies in an audio signal in order to improve the listening quality perception of the signal. It is usually placed just before the power amplifier in the audio signal chain. The most widely used circuit for accomplishing this is the *Baxandall tone control circuit*. An implementation of this is shown in Fig. 7.60. The stage driving the Baxandall tone control network at A is an emitter follower while the two-stage amplifier following the network at B is a standard design with feedback biasing discussed in Chap. 5. Feedback from the two-stage amplifier is applied to the network at C. Potentiometer \( VR_B \) lifts/cuts the bass frequencies, while potentiometer \( VR_T \) lifts/cuts the treble frequencies. The project involves researching Baxandall tone control theory and designing the network.
Ideas for Exploration: (i) Use bootstrapping to increase the gain in the second stage. This will provide increased feedback and hence lower distortion.

Problems

1. Draw and label the equivalent voltage amplifier. Indicate the levels of the input and output resistances relative to the source and load resistances and show how negative feedback can be applied around the amplifier.

2. Draw and label the equivalent current amplifier. Indicate the levels of the input and output resistances relative to the source and load resistances, and show how negative feedback can be applied around the amplifier.

3. State four advantages of negative feedback in amplifiers, and show how such feedback can be implemented around a transresistance amplifier.
4.

Determine the amount of negative feedback in an operational amplifier having an open-loop gain of 110 dB and a closed-loop gain of 20 dB.

5.

Explain what is meant by “gain stabilization” in a negative feedback amplifier and why it is important in the design of such amplifiers.

6.

Show that the magnitude of the fractional change in the gain of an open-loop amplifier is reduced by a factor equal to the loop gain in the closed-loop amplifier.

7.

An amplifier with gain 1500 has a gain change of 15% due to aging. Calculate the change in gain of the feedback amplifier if the feedback factor $\beta = 0.2$.

8.

An amplifier with a transfer function $A = \frac{k}{1+jf/f_o}$ has a low-frequency open-loop gain of $k = 120,000$ and an open-loop bandwidth of $f_o = 1$ Hz. For a closed-loop gain of 100, calculate the closed-loop bandwidth of the amplifier.

9.

Show that negative feedback reduces the distortion in the output stage of an amplifier by a factor equal to the loop gain.

10.

Discuss the effect of negative feedback on the input and output resistances of the four classes of amplifiers.

11.

Show that the bandwidth of a feedback amplifier increases with the application of negative feedback.

12.

Evaluate the voltage gain, input resistance, and output resistance for the voltage feedback amplifier in Fig. 7.61. For the transistors $h_{fe} = 120$, $h_{ie} = 5$ k, $h_{re} = h_{oe} = 0$.

13.

For the current amplifier shown in Fig. 7.62, determine the
closed-loop current gain, input resistance, and output resistance. For the transistors $h_{fe} = 100$, $h_{ie} = 2.5 k$, $h_{re} = h_{oe} = 0$. Determine $R_S$ to give a voltage gain of 12.

14. For the transconductance amplifier of Fig. 7.63, determine the closed-loop transconductance $G_M$, the closed-loop input impedance and the closed-loop output impedance.

15. For the trans-resistance amplifier of Fig. 7.64, determine $R_M$, $R_{ip}$, $R_{of}$ and the value of $R_S$ to give the system a voltage gain of 25. Use $h_{fe} = 120$ and $h_{ie} = 250$.

16. For an operational amplifier with a GBP of 8 MHz, determine the closed-loop bandwidth if the closed-loop gain is 12.

17. Design a four-transistor feedback amplifier using the topology in Fig. 7.40. Use a 24 V symmetrical supply and small signal transistors with gain of 150. Design the system for a closed-loop gain of 8.

18. Determine the open-loop voltage gain for the circuit mentioned in Question 17.

19. Design a transistor amplifier with a gain of 8 using the configuration of Fig. 7.49. Use a 25 V supply and transistors with current gain of 150.

20. For the feedback amplifier shown in Fig. 7.65, determine the current in each transistor, assuming they are all matched.
Fig. 7.61 Diagram for Question 12
Fig. 7.62 Diagram for Question 13

Fig. 7.63 Diagram for Question 14
Fig. 7.64  Diagram for Question 15
**Fig. 7.65** Diagram for Question 20

**Bibliography**


The operational amplifier or op-amp is one of the most widely used linear integrated circuits today. Its great popularity arises from its versatility, usefulness, low cost, and ease of use. It was introduced in the 1940s mainly for use in analog computers where it performed mathematical operations (hence the name) including addition, multiplication, integration, and differentiation. The device later found ready application in a wide range of circuits and functions, many of which will be discussed in this chapter. At the end of the chapter, the student will be able to:

- Understand the operation of the device.
- Derive the mathematical relations that govern its operations.
- Use the device in a range of linear circuit applications.

### 8.1 Introduction

The operational amplifier in Fig. 8.1 is a direct-coupled voltage amplifier that performs certain mathematical operations. It has a differential input and a single-ended output. It responds only to the
voltage difference $V_D$ between the two inputs given by $V_D = V_1 - V_2$ and not to their common potential. It amplifies this differential input voltage by a large factor $A_d$ which is the differential gain of the amplifier and delivers an output voltage given by

$$V_0 = A_d (V_1 - V_2) = A_d V_D$$  \hspace{1cm} (8.1)

**Fig. 8.1** Symbol for the op-amp with a dual power supply

A positive-going signal at the input defined as the non-inverting (+) input produces a positive-going signal at the output, while a positive-going signal at the input defined as the inverting (−) input produces a negative-going signal at the output.

The ideal operational amplifier possesses several important properties. Its voltage gain is infinite (very large), i.e., $A_d = \infty$, and is constant for all frequencies which means that the operational amplifier has infinite bandwidth. It has zero output impedance and infinite input impedance. The ideal operational amplifier also has the property that $V_o = 0$ when $V_D = 0$. In other words, no offset voltage is present at its output terminal when the differential input voltage is zero. The operational amplifier can, therefore, be represented by the ideal voltage-controlled voltage source shown in Fig. 8.2. Because $A_d = \infty$, the differential input voltage in an ideal operational amplifier is zero. Also, since the input resistance in either input terminal is infinite, there is no current flow into or out of either terminal.
The operational amplifier is an active device typically powered by a bipolar or dual-polarity supply ± V. This enables both input and output to be referred to ground or zero potential. Depending on the technology, it is constructed from bipolar transistors and/or field-effect transistors. The operational amplifier may operate from a ±15 V supply or a supply as low as ±0.9 V. The output of the operational amplifier is always constrained to fall between the supply rails + V and − V, both of which are usually equal. Usually, the details of the power supply of the operational amplifier are assumed to be standard and will henceforth be omitted unless otherwise stated.

To understand why $A_d$ must be large, we look back at (8.1) which defines the linear behavior of the operational amplifier. Now in order for $V_o$ to be finite and contained within the operational amplifier power supply limits, the product $A_d V_D$ must be finite. Under this constraint, as $A_d$ becomes large or $A_d \to \infty$, $V_D$ must become small or tend to zero. As a result for $A_d$ large, $V_D \approx 0$ or $V_1 \approx V_2$. The role of having a large gain can also be visualized in terms of the operational amplifier transfer characteristics as shown in Fig. 8.3. Here, the x-axis can be represented in terms of mV or μ V depending on the DC gain of the particular operational amplifier. The y-axis shows $V_o$ in volts up to the power supply limits. The ideal operational amplifier shown as the thick line has a hard-limiting transfer characteristic of a slope of $\infty$. A real operational amplifier has a “soft” characteristic as shown in Fig. 8.3. From henceforth we will always use the ideal model of the operational amplifier unless stated otherwise.

Fig. 8.2 The ideal voltage-controlled voltage source
In summary, therefore, the five important properties of the operational amplifier are listed below:

1. The voltage gain is infinite, i.e., \( A_d = \infty \).
2. The input resistance is infinite.
3. The output resistance is zero.
4. The bandwidth is infinite.
5. There is zero input offset voltage, i.e., \( V_O = 0 \) when \( V_D = 0 \).

In the following sections, we assume that these properties are true and examine several important configurations of the ideal operational amplifier.

### 8.2 The Inverting Amplifier
An amplifier which inverts an input signal while providing gain can be easily realized using the ideal operational amplifier as shown in Fig. 8.4. It is referred to as the inverting configuration. In this configuration, the non-inverting input is grounded, and the input signal is applied to the inverting input through resistor $R_1$, with negative feedback applied from the output through $R_2$. In response to an input signal $V_i$, a current $I_1$ flows into $R_1$, $I_2$ flows through $R_2$, and $I_A$ flows into the inverting terminal. From Kirchhoff’s current law (KCL),

$$I_1 = I_2 + I_A$$  \hspace{1cm} (8.2)

![Inverting amplifier](image)

**Fig. 8.4** Inverting amplifier

Since the op-amp has an infinite input resistance, no current flows into the inverting input and hence $I_A = 0$. Therefore, (8.2) reduces to

$$I_1 = I_2$$  \hspace{1cm} (8.3)

The current $I_1$ through $R_1$ is given by

$$I_1 = \frac{V_i - V_D}{R_1}$$  \hspace{1cm} (8.4)

where $V_D$ is the voltage at the inverting input of the op-amp. Since the amplifier gain is infinite, then from (8.1) for a finite output $V_o$, the voltage $V_D = V_o / A_d \to 0$ as $A_d \to \infty$. Hence from (8.4),

$$V_D = V_o / A_d \to 0$$  \hspace{1cm} (8.5)
Finally, the current $I_2$ in $R_2$ is given by

$$I_2 = \frac{V_D - V_o}{R_2} \quad (8.6)$$

Since $V_D = 0$, Eq. (8.6) becomes

$$I_2 = \frac{-V_o}{R_2} \quad (8.7)$$

It follows from Eqs. (8.3), (8.5), and (8.7) that

$$\Delta V = \frac{I_{DC} T_H}{C} = \frac{I_{DC}}{C f} \quad (8.8)$$

from which we get

$$\frac{V_o}{V_i} = -\frac{R_2}{R_1} \quad (8.9)$$

Equation (8.9) is an expression for the voltage gain of the inverting amplifier. The negative sign indicates that the output voltage signal is inverted relative to the input voltage signal. The input impedance $Z_i$ to the inverting amplifier is given by

$$Z_i = \frac{V_i}{I_i} \quad (8.10)$$

From (8.5), $I_i = I_1 = V_i/R_1$ and, therefore,

$$Z_i = \frac{V_i}{V_i/R_1} = R_1 \quad (8.11)$$

In this configuration, since $V_D = 0$ and the non-inverting terminal is at zero potential, it follows that the inverting terminal is also a zero potential, even though it is not directly connected to the ground. It is, therefore, called a *virtual earth*. Note that if the non-inverting terminal was at a potential different from zero, the inverting terminal
will not still be a virtual earth. It in fact will assume the potential of the non-inverting terminal. The high amplifier gain ensures that the inverting input is always at the same potential as the non-inverting input; the two terminals track each other.

Note, the gain $-\frac{R_2}{R_1}$ is often termed the closed-loop gain since it represents the gain under feedback or in the closed-loop system. If we let $R_1 = 1 \, \text{k}\Omega$ and $R_2 = 5 \, \text{k}\Omega$, then the gain is $-5$. Of course, if $R_2 = R_1$, then the gain is $-1$, and the circuit produces signal inversion (corresponding to a phase shift of $180^\circ$) with unity gain.

**Example 8.1** Design an operational amplifier circuit that has a gain of $-2$.

**Solution** Using the inverting configuration, let $R_1 = 10 \, \text{k}$. Then from Eq. (8.9), $R_2 = 2 \, R_1 = 20 \, \text{k}$.

**Example 8.2** If an inverting amplifier has $R_1 = 5 \, \text{k}$ and $R_2 = 20 \, \text{k}$, determine the gain of the system.

**Solution** Using (8.9), $A_V = -\frac{R_2}{R_1} = -\frac{20 \, \text{k}}{5 \, \text{k}} = -4$.

In choosing $R_1$ and $R_2$, their values should not be too small as to produce loading effects or not too large which may result in parasitic capacitance effects. Values in the range $1 \, \text{k}$ to $1 \, \text{M}$ are suitable. Thus, for a gain of $10$, for example, $R_1 = 10 \, \text{k}$ and $R_2 = 100 \, \text{k}$ are reasonable values.

**8.2.1 Inverting AC Amplifier**

If the circuit is used to amplify AC signals only, then a capacitor $C$ can be added at the input as shown in Fig. 8.5. The value of $C$ sets the lower $-3 \, \text{dB}$ cutoff frequency $f_L$ at

$$I_o = y_f V_i + y_o V_o$$  \hspace{1cm} (8.12)
If the source from which the circuit is driven has a resistance $R_S$, then

$$C = \frac{1}{2\pi f L (R_1 + R_S)}$$  \hspace{1cm} (8.13)

### 8.3 The Non-inverting Amplifier

Another important configuration is the non-inverting configuration shown in Fig. 8.6. It produces a gain equal to or greater than one as we will show. In this configuration, the input signal is applied to the non-inverting input, while negative feedback from the output is applied to the inverting input through resistor $R_2$. The inverting input is connected to ground through $R_1$. In response to an input signal $V_i$, currents $I_1$, $I_2$, and $I_A$ that are similar to what was seen in the inverting configuration flow. From KCL,

$$I_1 = I_2 + I_A$$  \hspace{1cm} (8.14)
Because of the infinite input impedance of the op-amp, \( I_A = 0 \), and therefore, (8.14) becomes

\[
I_1 = I_2 \tag{8.15}
\]

From Kirchhoff’s voltage law (KVL),

\[
V_i = V_D + I_1 R_1 \tag{8.16}
\]

Since \( V_D = 0 \), it follows that

\[
V_i = I_1 R_1 \tag{8.17}
\]

i.e., the input voltage is dropped across resistor \( R_1 \). From (8.17),

\[
I_1 = \frac{V_i}{R_1} \tag{8.18}
\]

But the voltage at the junction of \( R_1 \) and \( R_2 \) is \( V_i \). Hence

\[
I_2 = \frac{V_o - V_i}{R_2} \tag{8.19}
\]

Using (8.15), (8.18), and (8.19)
\[
\frac{V_i}{R_1} = \frac{V_o - V_i}{R_2}
\]

which reduces to

\[
\frac{V_o}{V_i} = 1 + \frac{R_2}{R_1}
\]

This is an expression for the voltage gain of the non-inverting amplifier. While the inverting amplifier inverts the input signal, the non-inverting amplifier does not. Further, while the minimum gain of the inverting amplifier is zero (corresponding to \(R_2 = 0\)), the minimum gain of the non-inverting amplifier is 1 (corresponding to \(R_2 = 0\)). The output then follows the input with 0° phase shift. The input impedance \(Z_i\) of the non-inverting amplifier is given by

\[
Z_i = \frac{V_i}{I_i} = \infty
\]

since \(I_i = 0\).

**Example 8.3**  Design a non-inverting amplifier with a gain of 10.

**Solution**  Using the non-inverting configuration, let \(R_1 = 1\) k. Then from Eq. (8.21),

\[
10 = 1 + \frac{R_2}{1k}
\]

giving \(R_2 = 9\) k.

**Example 8.4**  A non-inverting amplifier has \(R_1 = 2\) k and \(R_2 = 22\) k; determine the gain of the system.

**Solution**  Using (8.21),

\[
A_V = 1 + \frac{R_2}{R_1} = 1 + \frac{22\text{ k}}{2\text{ k}} = 12.
\]

In a practical non-inverting amplifier, a bias current needs to be provided to the non-inverting input terminal for the proper operation of the circuit. This bias may come from a direct-coupled circuit that is connected to the input. In general, however, a bias resistor \(R_B\) must be introduced as shown in Fig. 8.7 and should be as low as possible. Since the effective input impedance is now reduced to \(R_B\), these conflicting
requirements dictate that this resistor has an intermediate value between say 10 k and 1 M.

As shown above, the non-inverting amplifier is intrinsically capable of very high input impedance since the input is connected directly to the non-inverting terminal. This high impedance is, however, limited by the bias resistor $R_B$. This can be overcome by bootstrapping $R_B$ as shown in Fig. 8.7 by applying a signal in phase with $V_i$ at the lower end of $R_B$ using capacitor $C_2$. The effective value of $R_B$ is increased by a factor equal to the loop gain of the amplifier. In order to show this, from Fig. 8.8, consider the following:
For a feedback amplifier, the voltage gain $A_V$ is given by

$$A_V = \frac{V_o}{V_i} = \frac{A}{1 + A\beta}$$

(8.23)

where $A$ is the open-loop gain of the amplifier and $\beta = R_1/(R_1 + R_2)$ is the feedback factor. Using (8.23), the feedback voltage $V_f$ is given by

$$V_f = \beta V_o = V_i \frac{A\beta}{1 + A\beta}$$

(8.24)

Therefore, the current $I_B$ through $R_B$ is given by

$$I_B = \frac{(V_i - V_f)}{R_B} = V_i \frac{1}{(1 + A\beta) R_B}$$

(8.25)

Hence the input impedance $Z_i = V_i/I_B$ to the bootstrapped amplifier is given by
\[ Z_i = \beta/40I_C + (1 + \beta) R_E \] (8.26)

For a 741 operational amplifier, \( R_B \) is typically 100 k with \( A = 10^5 \) at low frequencies. \( C_2 \) sets the lower operating frequency below which the technique becomes ineffective. Because of the availability of high input impedance op-amps with low bias current requirements, this technique may not be necessary since the value of \( R_B \) can be quite high in such devices. Also, since bootstrapping is only effective for AC signals, \( C_1 \) is introduced to eliminate DC.

### 8.3.1 Non-inverting AC Amplifier

For the amplification of AC signals, a capacitor \( C \) must be added in series at the input as shown in Fig. 8.9. Its value is set by the resulting lower cutoff frequency \( f_L \) and is given by

\[ C = 1/(2\pi f_L R_B) \] (8.27)

![Non-inverting AC amplifier](image)

**Fig. 8.9** Non-inverting AC amplifier

If the circuit is driven from a source having impedance \( R_S \), then

\[ C = 1/[2\pi f_L (R_B + R_S)] \] (8.28)
In this situation, bias resistor $R_B$ is absolutely necessary. The bootstrapped version of this circuit is of course that shown in Fig. 8.8.

### 8.4 Voltage Follower

A special case of the non-inverting amplifier is the unity-gain stage shown in Fig. 8.10. Here, $R_1$ goes to infinity (removed), and $R_2$ goes to zero (short-circuited). $V_O$ is then exactly equal to $V_i$ since $V_D = 0$ corresponding to a gain of $+1$. Thus,

$$\frac{V_o}{V_i} = 1$$  \hspace{1cm} (8.29)

![Voltage follower](image)

**Fig. 8.10** Voltage follower

The resulting circuit shown in Fig. 8.10 has high input impedance, low output impedance, and a unity-gain closed-loop transfer function. The high input impedance $Z_i = \infty$ is again reduced by any bias resistor that may be required at the input.

Again, for AC signals, a high input impedance may be restored by using bootstrapping as shown in Fig. 8.11. From Eq. (8.26), since $β = 1$, the input impedance is given by $Z_i = (1 + A)R_B$. For a 741, $A = 10^5$ at low frequencies, and therefore, the low-frequency input impedance is given by $Z_i = (1 + 10^5) \times 100 \, k = 10^4 \, M$ which is an extremely high value!
As mentioned in Sect. 8.1, the operational amplifier derives its name from the fact that it is capable of performing mathematical operations. One such operation is the ability to perform the sum of input signals with the added advantage of having gains larger than one. To see how this is possible, we examine an extension of the inverting amplifier circuit shown in Fig. 8.12. Here, several \((n)\) input signals drive input resistors connected to the inverting terminal. By noting that the inverting node of the operational amplifier because of negative feedback acts as a virtual ground, then KCL dictates that

\[
\frac{V_1}{R_1} - 0 + \frac{V_2}{R_2} - 0 + \frac{V_3}{R_3} - 0 + \cdots + \frac{V_n}{R_n} - 0 = \frac{0 - V_o}{R_f}
\]

which reduces to

\[
V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3 + \cdots + \frac{R_f}{R_n}V_n\right)
\]
Hence the output voltage is the inverted sum of the scaled input voltages. Because each input resistor is connected to a virtual earth, it follows that the input resistance seen by each source $V_k$ ($k = 1, 2, 3, \ldots n$) is $R_k$. This makes the summing amplifier very useful for mixing audio signals from different sources. As in the single input inverting amplifier, the circuit performs inversion of the inputs.

The overall gain of the circuit is set by $R_f$ while the individual channel gains are set by the individual input resistors $R_1, R_2, R_3, \ldots, R_n$ which are also the input impedances of the respective inputs. Note that if $R_1 = R_2 = R_3 = \ldots = R_n = R_f$, then

$$V_o = - \frac{R_f}{R_i} (V_1 + V_2 + V_3 + \cdots + V_n) \quad (8.32)$$

Further if $R_1 = R_2 = R_3 = \ldots = R_n = R_f$, then

$$V_o = - (V_1 + V_2 + V_3 + \cdots + V_n) \quad (8.33)$$
which is a true summing inverter. Finally, linear signal mixing takes place at the summing junction without interaction between inputs since all signal source resistors feed into a virtual earth. The circuit can accommodate almost any number of inputs by adding input resistors at the summing point, but this is limited by noise and amplifier overload considerations.

**Example 8.5**  Design an operational amplifier circuit to realize \( V_o = -2V_1 - 3V_2 - V_3 \).

**Solution**  Comparing the requirement with Eq. (8.31), we must satisfy the following relations: \( R_f/R_1 = 2 \), \( R_f/R_2 = 3 \), and \( R_f/R_3 = 1 \). The obvious choice in this case is to choose \( R_2 \) with the largest gain term to be the smallest possible resistor we wish to use; in this case, let \( R_2 = 1 \) k\( \Omega \). It follows then that \( R_f = 3 \) k\( \Omega \), \( R_1 = 1.5 \) k\( \Omega \) and \( R_3 = 3 \) k\( \Omega \).

**Example 8.6**  Determine the output voltage \( V_o \) for the circuit shown in Fig. 8.13.

*Fig. 8.13*  Diagram for Example 8.6
**Example 8.7**  Determine the output voltage $V_o$ for the circuit shown in Fig. 8.14.

\[ V_A = 2 \times \frac{-10}{5} = -4 \, \text{V}; \quad V_o = -4 \times \left(1 + \frac{2}{1}\right) = -12 \, \text{V}. \]

*Fig. 8.14*  Diagram for Example 8.7

**Solution**

**Example 8.8**  Determine the output voltage $V_o$ for the circuit shown in Fig. 8.15.

\[ V_A = 1 \times \frac{-9}{3} = -3 \, \text{V}; \quad V_o = -3 \times \frac{4}{2} = 6 \, \text{V}. \]

*Fig. 8.15*  Diagram for Example 8.8

**Solution**

**Example 8.9**  Determine the output voltage $V_o$ for the circuit shown in Fig. 8.16.

\[ \frac{-V_A}{5} = \frac{2}{5} + \frac{1}{5} + \frac{4}{5}; \quad V_A = 1; \quad V_o = 1 \times \left(1 + \frac{1}{1}\right) = 2 \, \text{V}. \]
Solution $\frac{5-2}{6} = \frac{2-V_A}{3}; V_A = 0.5 \text{ V}; V_o = 0.5 \times \left(1 + \frac{3}{1}\right) = 2 \text{ V} \quad \text{(Fig. 8.16)}$.

### 8.6 The Differential Amplifier

A circuit capable of finding the difference of two analog signals is shown in Fig. 8.17. Note that this circuit offers different input impedances to each of its input sources. For $V_1$ the input resistance is $R_1$, while for $V_2$ its $R_a + R_b$. Rather than use KCL as we have done earlier, we can make use of the superposition principle to derive an expression for $V_o$. First, we short $V_2$ keeping $V_1$ active and recognizing that in that configuration $R_a$ which is in parallel with $R_b$ has no effect on the circuit and can be replaced by a short to ground. The circuit, therefore, resembles the inverting amplifier configuration: that is, $V_o' = -\frac{R_2}{R_1}V_1$.

Next, we short $V_1$ and note that the circuit resembles the non-inverting configuration this time except that the input $V_2$ is scaled by $\frac{R_b}{R_a+R_b}$ at the non-inverting terminal of the operational amplifier. Hence the output
voltage is given by \( V_o = \frac{R_b}{R_a+R_b} \left(1 + \frac{R_2}{R_1}\right) V_2 \). Adding the two results from superposition \((V_o = V'_o + V''_o)\) yields the result

\[
V_o = -\frac{R_2}{R_1} \left(V_1 - \frac{1 + \frac{R_1}{R_2}}{1 + \frac{R_a}{R_b}} \cdot V_2\right)
\]  

(8.34)

**Fig. 8.17** Differential amplifier

Two interesting scenarios arise out of the circuit of Fig. 8.17. The first occurs when the resistance ratios are all equal. That is, \( \frac{R_2}{R_1} = \frac{R_b}{R_a} \). In that case, (8.34) simplifies to

\[
V_o = -\frac{R_2}{R_1} (V_1 - V_2)
\]

(8.35)

and the output is thus proportional to the true difference of two inputs (but inverted).

The second case occurs when \( R_a = 0 \) and \( R_b = \infty \). This is shown in Fig. 8.18. In that case, \( V_o \) is given by
A special case of the difference amplifier

The advantage of the circuit of Fig. 8.18 over Fig. 8.17 is that it uses less components and offers a single high input impedance node. Its disadvantage is that it is capable of realizing only a limited range of functions. In either case, both Figs. 8.17 and 8.18 find uses in the design of instrumentation amplifiers.

Example 8.10  Design a circuit to realize the expression $V_o = V_2 - V_1$.

Solution  From (8.35), this condition occurs when we have equal resistances in the circuit of Fig. 8.13. In that case, choose $R_1 = R_2 = 10 \, \text{k}$ and $R_a = R_b = 10 \, \text{k}$.

Example 8.11  Design a circuit to realize $V_o = 3 \, V_2 - 2 \, V_1$.

Solution  Right away the circuit of Fig. 8.18 and Eq. (8.36) come to mind. We will use Fig. 8.18 because of the advantages previously mentioned. Hence the design equations are $\frac{R_2}{R_1} = 2$. Note, $1 + \frac{R_2}{R_1} = 3$ is satisfied by default. Letting $R_1 = 1 \, \text{k}$ yields $R_2 = 2 \, \text{k}$ which is the desired result.

Example 8.12  For the special case of the difference amplifier shown in Fig. 8.19, show that the relationship between the output and the output voltage $V_o$ is given by

$$V_o = \left(1 + \frac{R_2}{R_1}\right)V_2 - \frac{R_2}{R_1}V_1$$

(8.36)

**Fig. 8.18** A special case of the difference amplifier

$$V_o = \left(1 + \frac{R_2}{R_1}\right)V_2 - \frac{R_2}{R_1}V_1$$
inputs is $V_o = \frac{R_2}{R_1} (V_1 - V_2)$.

![Differential amplifier](image)

**Solution**  The differential amplifier amplifies the difference between two signals to be amplified. The potential at the non-inverting terminal is not zero, but instead is set by the potential divider arrangement of $R_1$ and $R_2$ and is given by

$$V_x = \frac{R_2}{R_1 + R_2} V_2 \quad (8.37)$$

Since the terminals of the op-amp track each other, it follows that the voltage at the inverting terminal is also $V_x$. Hence the current in resistor $R_1$ is given by

$$A_f = \frac{A}{1 + \beta A} \quad (8.38)$$

while that in resistor $R_2$ is given by

$$ (8.39)$$
\[ A_f = \frac{A}{1 + \beta A} \]

But
\[ I_1 = I_2 \]  \hspace{1cm} (8.40)

Therefore,
\[ \frac{V_1 - V_x}{R_1} = \frac{V_x - V_o}{R_2} \]  \hspace{1cm} (8.41)

Substituting for \( V_x \) using Eq. (8.37) yields
\[ \frac{V_1 - \frac{R_2}{R_1+R_2} V_2}{R_1} = \frac{R_2}{R_1+R_2} \frac{V_2 - V_o}{R_2} \]  \hspace{1cm} (8.42)

After manipulation, it gives
\[ V_o = -\frac{R_2}{R_1} (V_1 - V_2) \]  \hspace{1cm} (8.43)

If \( R_1 = R_2 \), then (8.43) reduces to
\[ V_o = -(V_1 - V_2) \]  \hspace{1cm} (8.44)

This means that with equal resistors throughout, the circuit functions as an inverting subtractor.

**Exercise 8.1**  Show that in the realization of \( V_o = 2 V_1 - 3 V_2 \), only Fig. 8.17 can be used and one solution is to choose \( R_a = R_b = R_1 = 1 \text{ k} \) and \( R_2 = 3 \text{ k} \).

### 8.7 Integrator

The integrator, sometimes referred to as the Miller integrator, is shown in Fig. 8.20. In this, the feedback resistor \( R_2 \) in the inverting amplifier is replaced by a capacitor \( C \). For this circuit,
\[ I_1 = I_2 \]

and this leads to

\[ \frac{V_i}{R} = -C \frac{dV_o}{dt} \]  

(8.46)

\[ \text{Fig. 8.20 Integrator} \]

Hence

\[ V_o = -\frac{1}{RC} \int V_i \cdot dt + c \]  

(8.47)

where \( c \) is the constant of integration. If, at the start of the integration, the output voltage is zero, then \( c = 0 \). If, for example, \( V_i \) is a constant voltage \( k \) and the capacitor is initially uncharged in which case \( c = 0 \), then \( V_o = -kt/RC \), and the output keeps rising until the op-amp saturates. At DC, the circuit functions as an open-loop amplifier, and therefore, offset currents flowing into \( C \) would result in an error voltage at the output. The magnitude of this voltage can be reduced by including a resistor \( R_C \) in parallel with \( C \) as shown in Fig. 8.21. This limits the low-frequency gain, and hence minimizes the voltage output error. The circuit operates as an integrator providing \( R_C \gg R \) and this it does above the frequency \( f = 1/2\pi R_C C \). Integrators find many users in filter design, signal processing, A/D converters, and much more.
\section*{8.8 Differentiator}

A circuit capable of performing analog differentiation is shown in Fig. 8.22. It is called a differentiator. In this circuit, the input resistor $R_1$ of the inverting amplifier is replaced by capacitor $C$.

Again,

\begin{equation}
I_1 = I_2
\end{equation} (8.48)
and hence

\[ \frac{V_i}{R} = -C \frac{dV_o}{dt} \]  \hspace{1cm} (8.49)

from which

\[ V_o = -CR \frac{dV_i}{dt} \]  \hspace{1cm} (8.50)

If, for example, \( V_i \) is a constant voltage \( k \), then \( V_o = 0 \) since \( d/dt(k) = 0 \). If \( V_i(t) = A \sin \omega t \), the output of the differentiator will be a cosine function with amplitude \( A\omega RC \), angular frequency \( \omega \), and a phase shift of 180°. The gain of this circuit increases with increasing frequency, and this makes the circuit susceptible to high-frequency noise. Moreover, the feedback resulting from this arrangement makes the circuit prone to instability. Both of these problems can be reduced by the inclusion of a resistor \( R_C \) in series with the capacitor as shown in Fig. 8.23. The circuit functions as a differentiator providing \( R_C \ll R \) and does so below the frequency given by \( f = 1/2\pi R_C C \).

![Fig. 8.23 Modified differentiator](image)

### 8.9 Transimpedance Amplifier

The operational amplifier can also function as a transimpedance amplifier or current-to-voltage converter. As a transimpedance
amplifier, it converts an input current into an output voltage as shown in Fig. 8.24. Note that this circuit is almost identical to the inverting amplifier configuration except that $R_1$ is absent and the amplifier is current driven. In this case, it is easy to show that according to KCL, $V_o = -I_i R_2$. The inverting terminal acts as a virtual earth as before, allowing for current driving at the inverting terminal. In addition, this terminal has low impedance due to negative feedback. If the non-inverting terminal is at a different potential from the ground, say $V_{ref}$, then it follows that the inverting terminal will also be at that voltage since they track each other, and hence $V_o = -I_i R_2 + V_{ref}$.

---

**Fig. 8.24** A transimpedance amplifier

### 8.10 Transconductance Amplifier

A transconductance amplifier performs a voltage-to-current conversion into a load. To accomplish this, we consider the circuit of Fig. 8.25 and view $R_L$ as a load resistor that we wish to drive. Then the current though $R_1$ given by $I_1 = V_i / R_1$ must be equal to the current $I_L$ through $R_L$. This current is independent of $R_L$ and depends only on the input voltage $V_i$ and $R_i$. The load resistor $R_L$ is a floating load since neither end is connected to the ground.
Example 8.13  Design a transconductance amplifier which drives a floating load $R_L = 2 \, k$ with a transconductance of 1 mA/V.

Solution  The desired transconductance is 1 mA/V and therefore $1/R_1 = 1 \, mA/V$ giving $R_1 = 1 \, k$.

8.11 The Instrumentation Amplifier

In many applications, there is a need to have an amplifier that can provide large amounts of gain so as to adequately amplify μV signals at moderate frequencies. Examples may include signals from temperature or pressure sensors (e.g., strain gauges), medical instruments, and other industrial transducers. A single op-amp cannot generally do the job since at gain of 1000; the device is unlikely to have sufficient bandwidth for practical applications. In fact, at a gain of 1000, the bandwidth of the op-amp can be expected to be $1/1000$ of its gain-bandwidth product (GBP). An alternative approach to amplification is to cascade several stages of smaller gain, but this introduces unwanted complications such as offsets and added noise at the final output stage. One of the best approaches is the three op-amp instrumentation amplifier shown in Fig. 8.26.
Operation of this device can be best understood if it is thought of as consisting of three sub-circuits. The first is a differential amplifier $A_3$ as discussed in Sect. 8.6 and shown in Fig. 8.17, and the other two are special cases of the difference amplifier $A_1$ and $A_2$ shown previously in Fig. 8.18. In most commercial instrumentation amplifiers, the resistor $R_G$ is typically applied externally as shown in Fig. 8.27 with some devices also offering $R_F$ externally (example: Analog Devices AD625). According, therefore, to Eqs. (8.36) and (8.34), the node voltages $V_3$, $V_4$, and $V_o$ can be expressed as

$$V_3 = \left(1 + \frac{R_F}{R_G}\right)V_1 - \frac{R_F}{R_G}V_y$$  \hspace{1cm} (8.51)

$$V_4 = \left(1 + \frac{R_F}{R_G}\right)V_2 - \frac{R_F}{R_G}V_x$$  \hspace{1cm} (8.52)

$$V_o = \frac{R_2}{R_1}\left(1 + \frac{R_1}{R_2} \cdot \frac{R_a}{R_b} \cdot V_4 - V_3\right)$$  \hspace{1cm} (8.53)
For matched resistors, $R_1 = R_a$ and $R_2 = R_b$ and noting that voltages $V_x$ and $V_y$ are equal to $V_1$ and $V_2$, respectively, Eqs. (8.51) to (8.53) can be solved to yield an output voltage expressed as

$$V_o = \frac{R_2}{R_1} \left(1 + \frac{2R_F}{R_G}\right)(V_2 - V_1)$$  \hspace{1cm} (8.54)

Clearly, the product of the first two terms in the right-hand side of (8.54) can yield very large gains if chosen appropriately. The ratio $V_o/(V_2 - V_1)$ can be thought of as the differential gain

$$A_D = \frac{V_o}{V_2 - V_1} = \frac{R_2}{R_1} \left(1 + \frac{2R_F}{R_G}\right)$$  \hspace{1cm} (8.55)

for this amplifier which can be easily changed by varying the single resistor $R_G$. The gain can also be changed by varying the other resistors, but for this case, several resistors of equal value would have to be changed simultaneously, and that becomes challenging in a practical sense.

**Exercise 8.2** The circuit shown in Fig. 8.28 is an alternative variable gain amplifier similar to the instrumentation amplifier just examined except that the inputs are not high impedance. Show for this, circuit that its output voltage $V_o$ is given by
when $R_2 = R_4$ and $R_3 = R_1$. Can you identify any possible drawbacks of this circuit?

\[
V_o = \left( \frac{R_4}{R_3} \right) \left( \frac{R_F}{R_G} \right) V_2 - \left( \frac{R_4 + R_3}{R_1 + R_2} \right) \left( \frac{R_F}{R_G} \right) V_1 = \left( \frac{R_2}{R_1} \right) \left( \frac{R_F}{R_G} \right) (V_2 - V_1)
\]

\(8.56\)

\[\text{Fig. 8.28} \quad \text{Alternative variable gain differential amplifier}\]

### 8.12 A Realistic Operational Amplifier

In the previous section, the model of Fig. 8.2 represented an ideal operational amplifier, and the circuits considered utilized this model. However, a practical op-amp varies somewhat from this with respect to the internal parameters of the operational amplifier such as input and output resistances. Also, while the gain was assumed to be infinite, all amplifiers have finite gain. Thus, a more realistic model that incorporates finite resistances and gain is shown in Fig. 8.29 where the input resistance $R_i$ is not infinite and the output resistance $R_o$ is not zero. For bipolar operational amplifiers, $R_i$ can be of the order of tens of MΩ, while for CMOS operational amplifiers, it can be around 10GΩ which is much larger. Similarly, $R_o$ is usually of the order of tens of ohms for both bipolar and CMOS operational amplifiers and is expected to be low. Note that in the case of bipolar operational amplifiers, a small bias current $i_1 \approx i_2$ is present at the input terminals. For CMOS operational amplifiers, this current is virtually non-existent and can be neglected.
altogether. Practical op-amps also have offset voltages $\pm V_{os}$ not modeled in Fig. 8.29, but its effect is to cause the output to be non-zero when the differential input is zero. Finally, the open-loop voltage gain varies across op-amps but is normally large. Typically values range from 1000 to $10^7$. The ubiquitous 741 has a typical voltage gain of $10^5$.

**Table 8.1** A comparison of various op-amp technologies with the ideal op-amp

<table>
<thead>
<tr>
<th></th>
<th>Bipolar</th>
<th>JFET</th>
<th>CMOS</th>
<th>Ideal op-amp</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_i$</td>
<td>6 MΩ</td>
<td>$10^{13}$ Ω</td>
<td>$10^{12}$ Ω</td>
<td>$\infty$</td>
</tr>
<tr>
<td>$R_o$</td>
<td>&lt;100 Ω</td>
<td>&lt;100 Ω</td>
<td>&lt;100 Ω</td>
<td>0</td>
</tr>
<tr>
<td>$A_d$</td>
<td>$10^3$–$10^6$</td>
<td>$10^3$–$10^6$</td>
<td>$10^3$–$10^6$</td>
<td>$\infty$</td>
</tr>
<tr>
<td>$i_1 \approx i_2$</td>
<td>$\pm 40$ μA</td>
<td>$\pm 1$ pA</td>
<td>&lt;1 pA</td>
<td>0</td>
</tr>
<tr>
<td>$\pm V_{os}$</td>
<td>25 μV</td>
<td>5 mV</td>
<td>$\approx 0$</td>
<td>0</td>
</tr>
</tbody>
</table>

As it turns out, the presence of $R_i$ and $R_o$ does not alter the results derived with the ideal op-amp model. For example, consider the
practical model in the inverting configuration of an op-amp where $R_i$ and $R_o$ have been included in the inverting configuration as shown in Fig. 8.30.

![Inverting Amplifier Circuit](image)

**Fig. 8.30** Inverting amplifier with finite input and output impedances

As before, using KCL yields

\[
\frac{V_a - V_i}{R_1} + \frac{V_a - V_o}{R_2} + \frac{V_a - 0}{R_i} = 0
\]

(8.57)

\[
\frac{V_o - (-A_o V_d)}{R_o} + \frac{V_o - V_a}{R_2} = 0
\]

(8.58)

Solving (8.57) and (8.58) yields

\[
\frac{V_o}{V_i} = -\frac{R_2}{R_1} \cdot \frac{1}{1 + \frac{(R_o+R_2)(\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_i})}{A_o - \frac{R_o}{R_2}}}
\]

(8.59)
Letting $R_1 = 1 \text{k}$ and $R_2 = 10 \text{k}$ and substituting typical values of $R_o = 100 \Omega$, $R_i = 100 \text{k}$ and $A_o = 10^5$ yield $\frac{V_o}{V_i} = -9.998879$. This value is almost exactly equal to the result obtained using the expression $-R_2/R_1$ or Eq. (8.9) which gives $-R_2/R_1 = -10$. Thus, our assumptions used in the ideal model hold to a very good approximation for the practical case.

### 8.12.1 Single Supply Operation

In the case of the dual power supply operational amplifier, the output is always referenced to the ground. However, in the case of the single supply operational amplifier, the output is typically referenced to mid-supply. Some special op-amps such as the LM324-Quad op-amp are specifically designed to operate on single supplies, but virtually any dual supply op-amp can be operated on a single supply if properly configured. What is needed is that one of the input terminals be referenced to mid-supply as shown in Fig. 8.31 for an inverting amplifier configuration. Here, the series-connected resistors $R$ are set equal so that a voltage that is half of the supply voltage is generated. The main consideration in the choice of the values of $R$ would be the current drain on the supply. The large capacitor $C_{bp}$ is present to ensure the voltage at the inverting terminal is grounded for AC signals. Resistors $R_1$ and $R_2$ function in the normal feedback mode to yield an inverting gain $-R_2/R_1$. Note that raising the non-inverting input terminal to mid-supply automatically raises the inverting terminal to the same voltage through negative feedback. The feedback will also cause the output of the op-amp to be at mid-supply voltage. In order to block this DC, capacitor $C_2$ is added but can be removed if DC coupling at this voltage level is required. A coupling capacitor $C_1$ is also necessary at the input because of the DC at the inverting terminal as shown in Fig. 8.31.
In order to use the op-amp in a non-inverting configuration from a single supply, the circuit of Fig. 8.32 can be employed. The circuit of Fig. 8.32 is essentially the dual of the previous one shown in Fig. 8.31 and operates in the same manner except that the gain is $1 + R_2/R_1$. This circuit no longer enjoys very high input impedance due to the presence of resistors $R$ at the non-inverting input of the op-amp. Therefore, the value of $R$ in this configuration is typically chosen in the megohms range, but having large resistors at the input increases the noise contribution to the amplifier.
Example 8.14    Design an inverting amplifier with a gain of −10 using the LM741 that operates from a 10 V power supply.

Solution    For a 10 V supply, choose $R = 10 \, \text{kΩ}$, thereby allowing 0.5 mA to flow through this potential divider. For a gain of −10, let $R_2 = 100 \, \text{kΩ}$ and $R_1 = 10 \, \text{kΩ}$. For a frequency response down to about 10 Hz, $C_1 = 1/2\pi \times 10 \times R_1 = 1.6 \, \mu\text{F}$. Use $C_1 = 2 \, \mu\text{F}$. A similar value can be used for $C_2$. Finally, $C_{bp} = 1/2\pi \times 10 \times 5 \times 10^3 = 3.2 \, \mu\text{F}$. Use $C_{bp} = 10 \, \mu\text{F}$ or larger.

8.13 Frequency Effects
In the previous sections, it was assumed that the large op-amp gain $A_d$ is constant for all frequencies and effects on gain caused by internal component capacitances were ignored. In all operational amplifiers, however, the gain $A_d$ is actually a frequency-dependent quantity, that is, $A_d \equiv A_d(s)$. In this section, therefore, we examine the effect of the
frequency-dependent gain $A_d(s)$ as it applies to real op-amps and its effect on overall closed-loop gain and bandwidth. The op-amp is a multi-stage voltage amplifier having several poles (and zeros) in its transfer function. This manifests itself as a roll-off rate of the frequency response plot that is greater than $-20$ dB/decade. Previously in Sect. 7.10 of Chap. 7 where feedback amplifiers were discussed, for such a system to be stable in the presence of feedback, we have established that the roll-off rate of the frequency response characteristic where it intersects the closed-loop gain plot must be no greater than $-20$ dB/decade. This is achieved by compensation such that the amplifier behaves as a single pole system, and this was also discussed in Chap. 7. As pointed out there, the op-amp is an excellent example of a voltage amplifier as it has a very high input impedance and low output impedance. Since most op-amps will find uses at unity gain whether as a buffer or an inverter, they are designed or internally compensated so that one pole dominates, and hence are unity-gain stable. In this section, we treat the op-amp as a single pole system and apply the theory developed earlier to the op-amp.

Thus, an op-amp is a voltage amplifier with a high input impedance and low output impedance. The input and output signals being voltages, the feedback type is voltage-series as shown in Fig. 8.33. This is the **non-inverting** configuration.

![Voltage amplifier](image)

*(a) without feedback  (b) with series feedback*

*Fig. 8.33  Voltage amplifier*
The transfer function \( A_v = V_o/V_i \) of the open-loop amplifier in Fig. 8.33a is represented as

\[
A_v = \frac{A_o}{1 + jf/f_o}
\]  

(8.60)

where \( A_o \) is the low-frequency gain and \( f_o \) is the open-loop bandwidth. The transfer function \( A_{vf} = V_o/V_i \) of the closed-loop amplifier in Fig. 8.33b is given by

\[
R = \frac{V_{in} - V_Z}{I_{Zmn} + I_L}
\]  

(8.61)

where \( \beta = R_1/(R_1 + R_2) \) is the feedback factor. Substituting for \( A_v \) using (8.60) and manipulating, we get

\[
A_{vf} = \frac{\left(1 + \frac{R_2}{R_1}\right) \cdot \frac{A_o \beta}{1 + A_o \beta}}{1 + jf/f_o \left(1 + A_o \beta\right)}
\]  

(8.62)

At low frequencies, Eq. (8.62) reduces to

\[
A_{vf}(DC) = \left(1 + \frac{R_2}{R_1}\right) \cdot \frac{A_o \beta}{1 + A_o \beta}
\]  

(8.63)

In the operational amplifier, \( A_o \) is very large, and hence the loop gain \( A_L = A_o \beta \) is such that \( A_L = A_o \beta \gg 1 \). As a result, Eq. (8.63) reduces to

\[
A_{vf}(DC) = 1 + \frac{R_2}{R_1} = 1/\beta
\]  

(8.64)

which is Eq. (8.21) that was previously derived. Note that from (8.64), \( A_L = A_o \beta = A_o/A_f(DC) \), i.e., the loop gain is equal to the open-loop gain divided by the closed-loop gain. In general, \( A_o \beta \gg 1 \) reduces (8.62) to

\[
dA_f = \frac{dA}{(1 + \beta A)^2}
\]  

(8.65)

where
is the closed-loop bandwidth.

Thus from (8.66), the closed-loop bandwidth $\bar{f}_o$ is increased by the factor of the loop gain as compared with the open-loop bandwidth $f_o$, directly as a result of feedback. Moreover, it is directly proportional to the loop gain $A_o\beta$. Since $A_o$ is fixed by expressing (8.66) in terms of $A_{vf}(DC)$ as

$$\bar{f}_o = f_o A_o / A_{vf}(DC)$$  \hspace{1cm} (8.67)

it is clear that the closed-loop bandwidth $\bar{f}_o$ is inversely proportional to the closed-loop low-frequency gain $A_{vf}(DC)$. The loop gain $A_L = A_o\beta = A_o / A_{vf}(DC)$ is the ratio of the open-loop gain and the closed-loop gain. When expressed in $dB$, it is given by

$$A_L (dB) = 20 \log A_o - 20 \log A_{vf}(DC)$$

$$= \text{low-freq open-loop gain (dB)} - \text{low-freq closed-loop gain (dB)}$$  \hspace{1cm} (8.68)

This represents the amount of feedback applied in the system as shown in Fig. 8.34. The maximum feedback occurs when $\beta = 1$ and is given by $A_{L(max)} = 20 \log A_0$. This is the unity-gain configuration and is obtained by setting $R_1 \to \infty$ and/or $R_2 = 0$ in Fig. 8.33. The corresponding bandwidth is given by

$$\bar{f}_o = f_o A_o$$  \hspace{1cm} (8.69)

which is referred to as the GBP of the voltage amplifier.
Finally, from (8.67),

\[ A_{vf}(DC) | \frac{f_o}{A_o} = A_{o}f_o = GBP = \text{constant} \]  

(8.70)

This equation states: closed-loop gain \( \times \) closed-loop bandwidth = GBP = constant.

**Example 8.15** An operational amplifier has an open-loop bandwidth \( f_o = 10 \text{ Hz} \) with \( GBP = 1 \text{ MHz} \). Determine the bandwidth for closed-loop gains (i) 10 and (ii) 100.

**Solution** (i) Using Eq. (8.70), the bandwidth for a closed-loop gain of 10 is \( \overline{f_o} = \frac{GBP}{A_{vf}(DC)} = 1 \text{ MHz}/10 = 100 \text{ kHz} \). (ii) Similarly, the bandwidth for a closed-loop gain of 100 is \( \overline{f_o} = \frac{GBP}{A_{f}(DC)} = 1 \text{ MHz}/100 = 10 \text{ kHz} \).

### 8.13.1 Inverting Configuration

The non-inverting amplifier can be converted to the **inverting** configuration by interchanging the signal input and ground points as shown in Fig. 8.35. By straightforward analysis using first principles, the transfer function \( A_f \equiv V_o/V_i \) of the closed-loop amplifier is given by
At low frequencies, Eq. (8.71) reduces to

$$f_T = \frac{\beta_o}{2\pi r_{b'c} (C_{b'c} + C_{b''c})}$$

which for large loop gains such that \(A_o\beta \gg 1\) becomes

$$I_C = \frac{V_{BB} - V_{BE}}{R_E + R_B/\beta}$$

The full Eq. (8.71) for large loop gains reduces to

$$A_{vf} = \frac{-R_2/R_1}{1 + jf/f_o}, A_o\beta \gg 1$$

where

$$f_o = f_oA_o\beta$$

is the closed-loop bandwidth and the low-frequency closed-loop gain

\(A_{vf} \equiv \frac{V_o}{V_i}(DC)\) is given by
\[ A_{vf}(DC) = -\frac{R_2}{R_1} = 1 - 1/\beta \quad (8.76) \]

The expression for the closed-loop bandwidth (8.75) of the inverting configuration is exactly the same as the expression (8.66) for the closed-loop bandwidth of the non-inverting configuration. Since the magnitude of the low-frequency gain \( \frac{R_2}{R_1} \) is less than that of the non-inverting configuration \( 1 + \frac{R_2}{R_1} \), the frequency response plot is shifted downward relative to that of the non-inverting configuration as shown in Fig. 8.36.

![Frequency response of inverting amplifier](image)

*Fig. 8.36* Frequency response of inverting amplifier

It follows also that the closed-loop bandwidth for the inverting configuration also varies as \( \beta \) is varied, and hence as the low-frequency gain \( A_{vf}(DC) \) is varied. Specifically, using (8.76) in (8.75) gives

\[ V_Z' = \left(1 + \frac{R_2}{R_1}\right)(V_Z + 0.7). \quad (8.77) \]

The maximum feedback 20 log \( A_o \) which occurs for \( \beta = 1 \) results in \( A_{vf}(DC) = 0 \). This corresponds to \( R_1 \to \infty \) and/or \( R_2 = 0 \).

Finally, in the inverting mode, it is possible to replace \( R_1 \) and \( V_i \) by a current source such that the input signal is a current \( I_i \) as shown in Fig.
8.37. Let $R_2 = R_F$. The circuit now functions as a transimpedance amplifier (current in, voltage out), but the feedback remains voltage-series. The transfer function $R_{mf} = V_o/I_i$ is given by

$$R_{mf} = \frac{-R_F \cdot A_o}{1 + jf/f_o (1 + A_o)}$$

(8.78)

which reduces to

$$R_{mf} = \frac{-R_F}{1 + jf/f_o}$$

(8.79)

where

$$f_o = f_o A_o$$

(8.80)

and the low-frequency closed-loop transimpedance $R_{mf}(DC)$ is given by

$$R_{mf}(DC) = -R_F$$

(8.81)

---

**Fig. 8.37** Transimpedance amplifier

This is the well-known current-to-voltage converter. Since the feedback mode is still voltage-series and the impedance of the current source is (ideally) infinite, it follows that $R_1 \rightarrow \infty$ and hence $\beta \rightarrow 1$. This configuration, therefore, corresponds to maximum voltage-series feedback with $20 \log A_o$ dB, and as is evident from (8.80), the closed-loop bandwidth $\overline{f_o}$ is the GBP of the associated amplifier. It is interesting to note that because of the high impedance of the signal
source, the closed-loop bandwidth $f_o$ is independent of the closed-loop low-frequency transimpedance $R_F$, and hence can be varied without affecting the bandwidth.

### 8.14 Non-ideal Effects

Apart from bandwidth issues, there are other factors or non-ideal effects that greatly influence the performance of an op-amp. These include offset voltages and currents, common mode rejection ratio, dynamic range, and slewing. In considering some of these, we begin with some definitions.

**Offset Voltages ($V_{os}$)**

Offset voltages in an op-amp occur because of mismatch in the input stages which results in an output voltage even when the differential input voltage is zero. Hence an offset voltage can be viewed as the voltage that must exist between the two input terminals of the op-amp in order to make the output voltage zero. Such voltages can have values of both polarities. A typical range of values might be ±10 μV to ±10 mV for bipolar op-amps and as high as ±50 mV for FET input op-amps.

**Input Offset Currents ($I_{os}$)**

Offset currents exist because there is a finite current flowing in/out of the input terminals that is required to bias the input transistors of the op-amp. By definition, $I_{os}$ is equal to the difference of the input bias currents or

$$I_{os} = \pm |I_{B1} - I_{B2}|$$  \hspace{1cm} (8.82)

where $I_{B1}$ and $I_{B1}$ are the input bias currents which may flow into or out of the op-amp. Sometimes a manufacture may specify an op-amp’s input bias current ($I_B$) which is the average of the two currents $I_{B1}$ and $I_{B2}$. That is,

$$I_B = \frac{1}{2} (I_{B1} + I_{B2})$$  \hspace{1cm} (8.83)
Bias currents are worse for op-amps made with bipolar input transistors than for those made with FET transistors. The input bias current $I_B$ is typically in the range 10 nA to 1 μA for bipolar op-amps and <100 pA for FET input op-amps. Although typically in the nanoampere to microampere range, input offset currents cause problems by creating unwanted voltage drops across input resistors. The overall effect is to cause the output of the op-amp to have a small offset voltage depending on the amplifier configuration used.

**Common Mode Rejection Ratio (CMRR)**

Common mode rejection ratio (CMRR) is the ratio of the differential gain of the op-amp to the common mode gain expressed in dB. Stated mathematically it is

$$R_{mf} = \frac{R_m}{1 + \beta R_m}$$

(8.84)

Common mode gain $A_{cm}$ is the ratio of the output voltage of an op-amp to the input voltage applied to both inputs simultaneously, i.e., with the inputs of the op-amp electrically connected. Under these conditions, there ought to be no output voltage from the op-amp as it ideally responds only to a differential voltage. The principal reason for an output in these circumstances is that the gain at one input is slightly different from that of the other. This is an undesirable effect since the objective of having differential inputs is to cancel any common mode signals that may be present. In op-amp circuits employing negative feedback, common mode gain is usually not a problem, but in instrumentation amplifiers without overall feedback, it can become problematic. Because $A_d$ is frequency dependent, it means that the CMRR is also frequency dependent. Manufacturers usually specify only the low-frequency value of the CMRR as its value decreases with increasing frequency. Expressed in dB the CMRR is given by

$$\text{CMRR} = 20 \log_{10} \left( \frac{A_{diff}}{A_{cm}} \right)$$

(8.85)
For a typical op-amp, CMRR is in the range 60–70 dB. More high-performance op-amps, however, have CMRR of the order of 120 dB.

**Power Supply Rejection Ratio (PSRR)**

Power supply rejection ratio (PSRR) is a measure of the level of insensitivity of the op-amp input to power supply changes. Expressed mathematically, it can be defined in dB as

\[
PSRR = 20 \log_{10} \left| \frac{\Delta V_{\text{supply}}}{\Delta V_{\text{in}}} \right| = \frac{1}{S}
\]  

(8.86)

where \( S \) is the power supply voltage sensitivity which is the change in input voltage \( \Delta V_{\text{in}} \) per unit change in supply voltage \( \Delta V_{\text{supply}} \). Because op-amps have two supplies, PSRR is usually defined for each supply.

**Slew Rate (SR)**

Slew rate (SR) is the maximum rate of change of the output voltage \( V_o \). It is typically specified in volts per microsecond and is usually stated by the manufacturer. SR limiting is a non-linear characteristic that can occur in all op-amps. It occurs when the maximum rate of change of the output voltage is reached. For general-purpose op-amps, this rate is typically in the range of 0.1–10 V/μs. For more special-purpose op-amps, it can reach as high as a few hundred V/μs to a few thousand V/μs. In the subsequent subsections, we discuss each of these effects in more details and look at ways of addressing them and their implications in a practical design.

### 8.14.1 Offset Voltage and Currents

As mentioned previously, manufacturing differences in the input stage of an op-amp are primarily responsible for the presence of offset voltages. Also, finite input currents at the input stages in the presence of resistances give rise to offset voltages at the output of the op-amp. In order to make sense of this effect, we consider the closed-loop model in Fig. 8.38. Here, we model the offset voltage by \( V_{os} \) and the two input
bias currents by \( I_{B1} \) and \( I_{B2} \). Note that it is their difference \( I_{B1} - I_{B2} \) that gives rise to an input offset current. Straightforward analysis of this circuit using superposition yields an output of the form

\[
V_o = I_{B1} R_2 - I_{B2} R_c \left( 1 + \frac{R_2}{R_1} \right) + V_{os} \left( 1 + \frac{R_2}{R_1} \right)
\]  

(8.87)

which after manipulation can be written as

\[
V_o = \left( I_{B1} - I_{B2} \right) R_2 + I_{B2} \left[ R_2 - R_c \left( 1 + \frac{R_2}{R_1} \right) \right] + V_{os} \left( 1 + \frac{R_2}{R_1} \right)
\]

(8.88)

Equation (8.88) indicates that the output is made up of three terms: the first one due to the input offset current \( I_{os} \) and the third term due to the input offset voltage \( V_{os} \). The middle term is due to one of the input bias currents, and it can be observed that it can be immediately canceled if we choose \( R_c = R_1 // R_2 \). In other words, to reduce the middle term to zero, we can add a resistor to the non-inverting input whose value is given by \( R_c = R_1 // R_2 \). Of course, if the non-inverting terminal is directly connected to the ground (\( R_c = 0 \)), the size of \( R_2 \) and \( I_{B1} \) will help to determine the output offset voltage. The first term in (8.88) indicates that to reduce its contribution to offset voltage for a given op-
amp, $R_2$ must be small. Of course, this comes at the expense of a reduction in gain. The minimum value of $R_2$ depends on the output signal swing and the load to which the op-amp is connected. Reducing $R_2$ also affects the third term in (8.88), but in this case it is the ratio $R_2/R_1$ that must be considered since this ratio also affects the closed-loop gain.

In some op-amps, it is possible to null the output voltage produced by the offset sources using an external voltage or as in the case of the 741 op-amp a potentiometer connected across two offsets “null” points. For the 741, these are pins 1 and 5 on the 8-pin DIP package with the potentiometer wiper connected to the negative supply. Note, however, that temperature changes in the components will eventually cause the output voltage to change with temperature. For other op-amps, laser trimming techniques are used to keep the output offset voltage to a minimum.

**Example 8.16** Using the specifications for the LF351 JFET input op-amp, determine the output offset voltage for the uncompensated and compensated inverting amplifier with resistors $R_2 = 10 \, \text{k}$ and $R_1 = 1 \, \text{k}$.

**Solution** From the data sheet of the LF351 op-amp, it lists maximum values of $V_{os} = \pm 10 \, \text{mV}$, $I_B = 200 \, \text{pA}$ and $I_{os} = \pm 100 \, \text{pA}$ all at 25 °C. We shall assume room temperature operation. For the uncompensated op-amp, $R_c = 0$, but $I_{B2}$ is not specified as required by (8.88). We can, however, make a best guess estimate by using (8.82) and (8.83) to solve for $I_{B2}$. Solving yields two values for $I_{B2}$ of 450 pA and 350 pA, but let us use the smaller of the two numbers. Substitution of the relevant numbers into (8.88) yields

$$V_{o_{0(nc)}} = 10 \, \text{k} \Omega (\pm 10 \, \text{pA}) + 350 \, \text{pA} (10 \, \text{k} \Omega) + (\pm 10 \, \text{mV}) \left(1 + \frac{10 \, \text{k} \Omega}{1 \, \text{k} \Omega}\right) = \pm 0.1 \, \text{mV} + 3.5 \, \text{mV} \pm 110 \, \text{mV}$$

In other words, the output offset voltage lies within the range $-110 \, \text{mV} \leq V_{0(nc)} \leq 110 \, \text{mV}$. Clearly, for the uncompensated amplifier, the offset voltage is the term that dominates because $I_{os}$ and $I_B$ are so small. With that in mind if the nominal value of $V_{os(nom)} = \pm 5 \, \text{mV}$ is used, then
the output voltage lies in the range \(-55 \text{ mV} \leq V_{o(\text{nom, nc})} \leq 55 \text{ mV}\). For the compensated amplifier, the situation does not change much since the second term in (8.88) is zero. Thus the output voltage lies in the range \(-110 \text{ mV} \leq V_{o(c)} \leq 110 \text{ mV}\) and with the nominal value in the range \(-55 \text{ mV} \leq V_{o(\text{nom,c})} \leq 55 \text{ mV}\). Therefore, in this case, compensation can be omitted, but it will not be the case for all op-amps.

### 8.14.2 CMRR and PSRR

As stated earlier, the CMRR is a measure of how well an op-amp amplifies differential signals and rejects common mode ones as given by the ratio

\[
R_{of} \equiv \frac{V}{I} = R_o (1 + \beta A_i)
\]  

(8.89)

where we shall assume that we are working at low frequencies so that \(A_d = A_o\) can be used. An equation that fully describes the effects of both differential and common mode gain is, therefore, given by

\[
V_o = A_d (V_1 - V_2) + A_{cm} \left( \frac{V_1 + V_2}{2} \right) = A_d V_D + A_{cm} V_{cm}.
\]  

(8.90)

In Eq. (8.90), the factor of \(\frac{1}{2}\) is there because under common mode conditions when \(V_1 = V_2 = V_{cm}\), then \(V_o = A_{cm} V_{cm}\) which is consistent with the definition of common mode gain. Equation (8.90) can, therefore, be rewritten as

\[
V_o = A_o \left[ V_D + \frac{V_{cm}}{\text{CMRR}} \right]
\]  

(8.91)

or

\[
V_o \approx A_o \left[ V_1 - V_2 \left( 1 - \frac{1}{\text{CMRR}} \right) \right]
\]  

(8.92)

if \(V_1 \approx V_2\). Both representations are equally valid, but (8.92) indicates that we can simply add a voltage source of value \(V_2/\text{CMRR}\) to the
positive input on an op-amp to model its effect. Such a model is shown in Fig. 8.39.

**Fig. 8.39** Op-amp model that accounts for both CMRR and PSRR

In a similar manner, we can describe the PSRR by the equation

\[ V_o = A_o V_D + S \Delta V_{\text{supply}} A_o \]

or

\[ V_o = A_o \left( V_D + \frac{\Delta V_{\text{supply}}}{\text{PSRR}} \right) \]  \hspace{1cm} (8.93)

As in the case of the CMRR, we can add a voltage source of value \( \Delta V_{\text{supply}}/\text{PSRR} \) to the non-inverting terminal. A model that incorporates both CMRR and PSRR is shown in Fig. 8.39. Finally note that it is not uncommon to find the CMRR and the PSRR of the same order for a given op-amp.

**Exercise 8.3** Show that by using the circuit of Fig. 8.18 with \( V_1 = V_2 = V_i \), the CMRR of an op-amp can be measured with the value

\[ V_o = \frac{V_{CC}}{2} \cdot \frac{R_L}{R_E + R_L} \]

**8.14.3 CMRR of the Instrumentation Amplifier**

For the instrumentation amplifier previously discussed in Sect. 8.11, it can be shown that its common mode gain is given by

\[ A_{cm} = \frac{V_o}{V_{cm}} = \frac{R_a}{R_a + R_b} \left( 1 + \frac{R_2}{R_1} \right) - \frac{R_2}{R_1} \]  \hspace{1cm} (8.94)

Using (8.55), therefore, the CMRR for this circuit becomes
Clearly, if \( R_1 = R_a \) and \( R_2 = R_b \) as stated before, then the CMRR → \( \infty \). In practice, this will not be the case because of resistance tolerances. However, it is not uncommon to easily achieve CMRRs in excess of 100 dB. Like op-amps, the CMRR in instrumentation amplifiers is frequency dependent, but its frequency dependency usually comes from parasitic capacitances at its input nodes.

### 8.14.4 Slew Rate

Slew Rate (SR) limiting occurs when an op-amp is required to change its output at a rate that the internal dynamics of the op-amp do not allow. It represents the maximum rate of change of the output voltage expressed in V/μs. To understand this limitation, consider the simplified model of a typical three-stage op-amp in Fig. 8.40 represented by a differential transconductor stage, a second gain stage and a third stage buffer for driving low-impedance nodes. The second stage usually contains a compensation capacitor \( C_c \) and the first-stage transconductor has a bias current \( I_b \) to bias the differential input pair. If the input voltage suddenly receives a large differential voltage, then the output of the transconductance stage will either sink current into \( C_c \) or source current from \( C_c \) depending on the polarity of the differential voltage. In either case, that current approaches the bias current value so that \( I_o \approx \pm I_b \). Assuming for the moment that \( I_o \) flows into \( C_c \) so that the positive sign can be used, then the corresponding rate of change of output voltage from amplifier \( A_2 \) is given by

\[
\frac{dV_c}{dt} = \frac{I_b}{C_c}
\]
Since this voltage is directly conveyed to the output buffer, it follows that $V_o = V_c$ so that the output voltage of the op-amp experiences a rate of change of voltage which we define as the SR of

$$SR^+ = \frac{dV_o}{dt} = \frac{I_b}{C_c}$$  \hspace{1cm} (8.97)

The positive sign is included in (8.97) to show that it represents the positive SR. By a similar reasoning, if the polarity of the input differential voltage was reversed, then $-I_b$ would flow out of $C_c$ generating a negative SR of

$$SR^- = \frac{dV_o}{dt} = -\frac{I_b}{C_c}$$  \hspace{1cm} (8.98)

The primary reason there are two different values for positive and negative SRs is that sometimes the input stage is not completely symmetric and different values of output current $I_o$ exist for negative and positive differential inputs. A typical value is, therefore, quoted by most manufacturers with a square wave or step input being the most commonly used test signal.

The topology shown in Fig. 8.40 is not the only topology used in designing op-amps. New high SR op-amps such as the LT1364 employ a different topology that offers higher SRs than the approach of Fig. 8.40 and is shown in Fig. 8.41. This is achieved by sensing currents that are...
proportional to the difference of the differential inputs. Buffers provide high-impedance inputs to the op-amp. Resistor $R$ limits the maximum current that can flow through the buffers. The sensed currents are then copied, and their difference is used to drive a high-impedance node labeled $z$ in Fig. 8.41 to achieve high gain in the op-amp. The voltage at that node is buffered to preserve the high gain. The high SR arises because $C_c$ can be made small, while the sensed currents $I_{1,2}$ can be large.

**Fig. 8.41** An alternative op-amp model

If the output of the op-amp is a sine wave described by the equation $V_o(t) = V_a \sin \omega t$ where $V_a$ is the amplitude and $\omega$ is the angular frequency, then the output signal achieves its maximum slope at its zero crossings and is given by

$$R_{of} = \frac{R_o}{1 + \beta R_M} = \frac{R_L//R_F}{1 + \beta R_M} \quad (8.99)$$

For linear op-amp operation, the SR given in (8.99) must not exceed the SR of the op-amp; otherwise SR limiting occurs. This imposes an upper bound on the frequency of operation of the op-amp for a given sinusoidal output amplitude. That bound is sometimes referred to as the full power bandwidth ($BW_p$) and is given by

$$\quad (8.100)$$
\[ BW_p = \frac{SR}{2\pi V_a}. \]

Equation (8.100) indicates that bandwidth can be traded for output amplitude and vice versa to avoid SR limiting. As an example, consider an op-amp with a slew rate of \( SR = 13 \text{ V/\mu s} \) and maximum peak output voltage \( V_a = 14 \text{ V} \) being powered from a \( \pm 15 \text{ V} \) supply. The full power bandwidth can then be calculated to be

\[ BW_p = 13 \times 10^6/(2\pi \times 14) = 148 \text{ kHz}. \]

Its theoretical peak-to-peak output swing versus frequency will, therefore, resemble the plot shown in Fig. 8.42. Therefore, in order to operate this op-amp at 1 MHz, the maximum peak output voltage \( V_a \) that can be delivered using (8.100) is given by \( V_a = SR/2\pi BW_p = 13 \times 10^6/2 \times \pi \times 10^6 = 2.1 \text{ V}. \)

Finally, manufacturers often specify a plot like that in Fig. 8.42 but seldom provide \( BW_p \) in their specifications because it depends on the supply voltage, gain, and load conditions.
8.15 The Current Feedback Amplifier

The current feedback amplifier (CFA) is a transimpedance amplifier. It accepts a current at the input and delivers a voltage at the output and has a low input impedance and a low output impedance. It, therefore, employs voltage-shunt feedback in which the output voltage is sampled and the feedback signal is a current. Because of its topology, it typically has larger bandwidths than the op-amp and an extremely high SRs. Indeed, bandwidths as high as 2 GHz and SRs of the order of thousands of V/μs are possible with the CFA. However, the CFA suffers from several disadvantages compared with the op-amp including more noise, larger DC offsets and certain feedback restrictions.

The operation of the CFA can best be understood by considering the idealized model shown in Fig. 8.43. Between the two inputs is an
idealized buffer with infinite impedance on the non-inverting input and zero impedance on the inverting terminal. As a result of the buffer, the inverting terminal will always follow the non-inverting terminal much like an op-amp but of course for a different reason. In an op-amp, negative feedback causes this following action, but it is the buffer in the case of the CFA. At the zero-impedance inverting terminal, a current out of this terminal generates an output voltage $V_o$ through a transimpedance $Z(s)$ given by

$$V_o = Z(s)I_i$$  \hspace{1cm} (8.101)

![Simplified model of the CFA](image)

**Fig. 8.43** Simplified model of the CFA

It is because of this why it is sometimes called a transimpedance amplifier. At the output, we assume that the current-controlled voltage source has zero impedance. The transimpedance $Z(s)$ is assumed to follow the one pole model given by

$$Z(jf) = \frac{Z_o}{1 + jf/f_o}$$  \hspace{1cm} (8.102)

where $f_o$ is the $-3$ dB transresistance pole frequency and $Z_o$ is the low-frequency transresistance.

In order to utilize the CFA in a transimpedance application, let us consider the circuit of Fig. 8.44 with feedback resistor $R_2$. An input
current \( I_i \) is injected into the low-impedance inverting node, and we wish to determine the output voltage \( V_o \). Because the input resistance at the inverting input is zero, the voltage at this terminal is also zero. Using KCL at this terminal yields

\[
I_R \geq I_C / 10 \quad (8.103)
\]

Using KCL at this terminal yields

\[
I_R \geq I_C / 10
\]

**Fig. 8.44** The CFA configured as a trans-resistance amplifier

For the device,

\[
V_o = -I_e Z \quad (8.104)
\]

and

\[
I_2 = (0 - V_o) / R_2 = -V_o / R_2 \quad (8.105)
\]

Hence (8.103) becomes

\[
I_i = \frac{-V_o}{Z} + \frac{-V_o}{R_2} = \frac{-V_o}{R_2 / |Z|} \quad (8.106)
\]

Then the transfer function \( V_o / I_i \) is given by

\[
\frac{V_o}{I_i} = -R_2 \left( \frac{1}{1 + R_2 / |Z|} \right) \quad (8.107)
\]

If \( Z \to \infty \), then \( \frac{V_o}{I_i} = -R_2 \). Considering now the frequency effects associated with the transimpedance given by \( Z(jf) = \frac{Z_0}{1 +jf / f_o} \), then
(8.107) becomes

\[
\frac{V_o}{I_i} = -R_2/Z = -R_2 \frac{Z_o \beta / (1 + Z_o \beta)}{1 + jf / f_o (1 + Z_o \beta)}
\]  

(8.108)

where \( \beta = I_2/V_o = 1/R_2 \) is the feedback factor and \( Z_o \beta \) is the loop gain. In CFAs, \( Z_o \gg 1 \), and hence \( Z_o \beta \gg 1 \). Equation (8.108), therefore, reduces to

\[
\frac{V_i - V_o}{R_G} = g_m V_i + \frac{V_o}{r_d / R_D}
\]  

(8.109)

From this, the closed-loop bandwidth is given by

\[
\bar{f}_o = f_o (1 + Z_o \beta)
\]  

(8.110)

Since \( Z_o \beta \gg 1 \), this reduces to

\[
\bar{f}_o = f_o Z_o \beta = f_o Z_o / R_2
\]  

(8.111)

From (8.109), the low-frequency trans-resistance is \(-R_2\), and from (8.111), it can be seen that the closed-loop bandwidth varies with \( R_2 \).
A plot of Eq. (8.109) with $Z_o = 3 \, \text{M}$ and $f_o = 5000 \, \text{Hz}$ showing transresistance (log scale) versus frequency for varying values of $R_2$ is shown in Fig. 8.45. For example, for $R_2 = 1 \, \text{k}$, the magnitude of the low-frequency transresistance is $R_2 = 1 \, \text{k}$ giving $\log 10^3 = 3$ on the log scale, and from (8.111), the closed-loop bandwidth is

$$f_o = f_o Z_o / R_2 = 5 \times 10^3 \times 3 \times 10^6 / 10^3 = 15 \, \text{MHz}.$$ 

Clearly, as $R_2$ decreases in value, the bandwidth of the amplifier increases, and the curves of Fig. 8.45 closely resemble those of the closed-loop gain of the op-amp as $R_2$ changes. Conversely if $R_2$ increases, the transresistance increases, but the bandwidth decreases.
Can the value of $R_2$ be reduced to zero? The answer to this is no. The reason for this lies in the fact that (8.102) represents a single pole model and extra poles due to circuit design exist in the circuit. As $R_2$ decreases, the effect of additional circuit poles will cause peaking in the frequency response of the amplifier. If $R_2$ is decreased even further, it is possible that the circuit may break into oscillations. For this reason, CFA manufacturers usually specify a minimum value for $R_2$ below which the CFA performance suffers considerably. Typical values of $R_2$ fall in the few kilo-ohms range and are rarely less than 1 kΩ.

**8.15.1 Inverting Amplifier**

If an input resistor $R_1$ is now added to the inverting terminal and a voltage source drives this amplifier, an inverting voltage amplifier results as shown in Fig. 8.46. For this configuration, noting that the input resistance at the inverting terminal is zero, then $I_i = V_i/R_1$, and therefore, substituting for $I_i$ in Eq. (8.109) yields the transfer function given by

$$\frac{V_o}{V_i} = \frac{-R_2/R_1}{1 + jf/fo(1 + Z_0\beta)}$$

(8.112)

which for low frequencies becomes

$$\frac{V_o}{V_i} = \frac{R_2}{R_1}$$

(8.113)

![Fig. 8.46 CFA inverting amplifier](image)
Equation (8.113) indicates that the expression \(-R_2/R_1\) for the closed-loop gain of the inverting amplifier for the CFA is the same as that for the op-amp. The \(-3\) dB closed-loop bandwidth is given by

\[
\bar{f}_o = f_o (1 + Z_o \beta) = f_o \left(1 + Z_o / R_2\right)
\]

which is the same as the transresistance case in Eq. (8.110). Note that while this value is dependent on \(R_2\), it is not dependent on \(R_1\). Thus, the closed-loop bandwidth of the CFA in the inverting configuration is independent of resistor \(R_1\). This fact makes the CFA very attractive compared to the op-amp whose gain and bandwidth are directly related by the GBP. It follows that resistor \(R_1\) may be changed to vary the CFAs closed-loop gain via \(-R_2/R_1\) and the bandwidth will remain constant provided \(R_2\) is fixed.

### 8.15.2 Non-inverting Amplifier

To utilize the CFA in a non-inverting application, let us consider the circuit of Fig. 8.47 with feedback resistor \(R_2\) and grounded resistor \(R_1\). The input voltage is applied to the non-inverting high-impedance terminal. Then from KCL,

\[
V_{oc} = A_y V_i
\]  

(8.115)
Noting that $V_D = 0$ from (8.115), we have

$$\frac{V_1 - V_x}{R_1} = \frac{V_x - V_o}{R_2}$$  \hspace{1cm} (8.116)

After substitution for $Z$ and manipulation, we get

$$\frac{V_o}{V_i} = \frac{(1 + \frac{R_2}{R_1}) \cdot \left(\frac{Z_0 \beta}{1 + Z_0 \beta}\right)}{1 + jf/f_o (1 + Z_0 \beta)}$$  \hspace{1cm} (8.117)

which for $Z_0 \beta \gg 1$ becomes

$$\frac{V_o}{V_i} = \frac{1 + \frac{R_2}{R_1}}{1 + jf/f_o (1 + Z_0 \beta)}$$  \hspace{1cm} (8.118)

At low frequencies, this reduces to

$$\frac{V_o}{V_i} = 1 + \frac{R_2}{R_1}$$  \hspace{1cm} (8.119)
Equation (8.119) indicates that the expression \((1 + R_2/R_1)\) for the closed-loop gain of the non-inverting amplifier for the CFA is the same as that for the op-amp. The −3 dB closed-loop bandwidth is given by

\[
\bar{f}_o = f_o \left(1 + Z_o \beta\right) = f_o \left(1 + Z_o/R_2\right)
\]

which is the same as the transresistance and the inverting cases. Once again note that while this value is dependent on \(R_2\), it is not dependent on \(R_1\). Thus, the closed-loop bandwidth of the CFA in the non-inverting configuration is independent of resistor \(R_1\). It follows that resistor \(R_1\) may be changed to vary the CFAs closed-loop gain by way of \((1 + R_2/R_1)\) and the bandwidth will remain constant provided \(R_2\) is fixed. Plots of the closed-loop gain for an ideal CFA with \(Z_o = 3\) M, \(R_2 = 2\) k and \(f_o = 9000\) Hz in the non-inverting configuration are shown in Fig. 8.48. Using (8.120), the bandwidth can be seen to remain constant at \(f_o = 9000 \times 3 \times 10^6/2 \times 10^3 = 13.5\) MHz with changing gain effected by changing \(R_1\).
Example 8.17  For an ideal CFA having $Z_o = 2 \, \text{M}$ and $f_o = 5 \, \text{kHz}$, determine the closed-loop bandwidth for $R_2 = 5 \, \text{k}$.

Solution  Using (8.120)

$$f_o = f_o (1 + Z_o/R_2) = 5 \times 10^3 \times 2 \times 10^6/5 \times 10^3 = 2 \, \text{MHz}.$$  

As in the case of the op-amp, if $R_1 \to \infty$, then the closed-loop gain is unity, and the bandwidth is given of course by Eq. (8.120). While in the case of the op-amp, we can go further and set $R_2 = 0$ to yield the classical buffer, this cannot be done in a CFA since $R_2$ determines the amount of feedback around the device and lowering its value increases
the amount of feedback. The CFA will become unstable if this value is reduced below about 1 k as explained earlier. To use the CFA as a buffer, it must, therefore, be connected as shown in Fig. 8.49 where $R_F = 1 \text{k}$. 

![CFA Figure]

**Fig. 8.49** The CFA connected as a buffer

### 8.15.3 Mixer

As a summing amplifier or mixer, the CFA performs particularly well since the inverting input has an already low impedance, thereby allowing the mixing of currents without interference. This low impedance is made even lower by the applied negative feedback. The bandwidth of the mixer is also not affected by the input source resistances since the CFA bandwidth is fixed by the feedback resistor $R_f$ as shown in Fig. 8.50. Note this is in direct contrast to a mixer designed using op-amps in which the low-impedance inverting node is only made low by negative feedback. The op-amp also suffers from the fact that its bandwidth as a mixer is dependent on the input resistors $R_i$, $i = 1, 2, \ldots, n$. 
The CFA can also be used as a differential amplifier in much the same way as its op-amp counterpart. In that case, the circuit shown in Fig. 8.51 can be used, and the output is given by

\[ V_o = -\frac{R_2}{R_1} (V_1 - V_2) \]  

(8.121)
The important consideration when using this amplifier configuration is that resistor $R_2$ sets the bandwidth of the amplifier and the remaining resistors are defined around this value depending on the gains required. Finally, note the special case of the difference amplifier governed by Eq. (8.36) with $R_1 = 0$ and $R_2 = \infty$ driven by $V_2$ also apply to this circuit.

8.15.5 Integrator
The most notable exception to the CFA’s general use is as an integrator. The problem that the CFA has in the integrator configuration is that the impedance of the feedback capacitor $C_f$ is frequency dependent and can fall below the minimum value of $R_2$ set for stable operation. This configuration should, therefore, be avoided.

8.15.6 Further Bandwidth Considerations
In real CFAs, however, the bandwidth situation is never quite as Fig. 8.48 indicates and as Eq. (8.120) predicts. The bandwidth unfortunately does vary somewhat with changing closed-loop gain as a result of variation in resistor $R_1$. The main reason for this is the finite input impedance at the input to the buffer at the input of the device. If we include impedances $r_x$ and $r_o$ in the CFA model as illustrated in Fig.
then it can be shown that the new closed-loop bandwidth using the non-inverting amplifier is given by

\[ f_{cl} \approx \frac{f_0 Z_0}{R_2} \left( \frac{1}{r_x \left( \frac{1}{R_1} + \frac{1}{R_2} + \frac{r_o}{R_1 R_2} \right) + \frac{r_o}{R_2} + 1} \right) \]  

\[ (8.122) \]

**Fig. 8.52** Small-signal model of the CFA to include finite impedances

Since \( r_o \ll R_2 \), Eq. (8.122) reduces to

\[ f_{cl} \approx \frac{f_0 Z_0}{R_2} \left( \frac{1}{r_x \left( \frac{1}{R_1} + \frac{1}{R_2} + \frac{r_o}{R_1 R_2} \right) + \frac{r_o}{R_2}} \right) \]  

\[ (8.123) \]

Equation (8.123) predicts that the bandwidth will decrease as \( R_1 \) decreases although the change is not as marked as that for an op-amp. Of course if \( r_x = 0 \), Eq. (8.123) reverts to Eq. (8.120). For the previous case where \( R_2 = 2 \, \text{k} \), \( Z_0 = 3 \, \text{M} \) and \( f_0 = 9 \, \text{kHz} \) that led to Fig. 8.48, the bandwidth changes if the input impedances \( r_x = 50 \, \Omega \) and \( r_o = 100 \, \Omega \) are included as shown in Fig. 8.53. For the values of \( R_1 \) given in Fig. 8.48,
the bandwidths are 10.1, 11.7, 12, and 12.4 MHz in the order of increasing $R_1$. Finally, it should be noted that the input impedance $r_x$ at the inverting input is not purely resistive but rather has an inductive component associated with it. Hence its impedance eventually rises with frequency. For most applications, this is not a problem since the shunt feedback reduces it even further from its open-loop value.

![Frequency response plot for varying gains with finite impedances](image)

**Fig. 8.53** Frequency response plot for varying gains with finite impedances

### 8.16 Applications

In this section, we discuss several circuits based on the op-amp. Most of them employ the 741 op-amp which is perhaps the most popular device. Typical parameters for this and three other devices are presented in Table 8.2.
### Table 8.2 Characteristics of several unity-gain stable op-amps

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>741</th>
<th>OPA134</th>
<th>OPA452</th>
<th>LF351</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_o$</td>
<td>Open-loop voltage gain</td>
<td>100 dB</td>
<td>120 dB</td>
<td>110 dB</td>
<td>106 dB</td>
</tr>
<tr>
<td>$Z_i$</td>
<td>Input impedance</td>
<td>1 M</td>
<td>10G</td>
<td>10G</td>
<td>1G</td>
</tr>
<tr>
<td>$I_b$</td>
<td>Input bias current</td>
<td>200 nA</td>
<td>±100 pA</td>
<td>±100 pA</td>
<td>±100 pA</td>
</tr>
<tr>
<td>$V_S$</td>
<td>Maximum supply voltage</td>
<td>±18 V</td>
<td>±18 V</td>
<td>±40 V</td>
<td>±18 V</td>
</tr>
<tr>
<td>$V_{imx}$</td>
<td>Maximum input voltage</td>
<td>±13 V</td>
<td>±15 V</td>
<td>±34.5 V</td>
<td>±15 V</td>
</tr>
<tr>
<td>$V_{omx}$</td>
<td>Maximum output voltage</td>
<td>±14 V</td>
<td>±15.5 V</td>
<td>±34.5 V</td>
<td>±12.5 V</td>
</tr>
<tr>
<td>$I_{omx}$</td>
<td>Maximum output current</td>
<td>±25 mA</td>
<td>±35 mA</td>
<td>±50 mA</td>
<td>±30 mA</td>
</tr>
<tr>
<td>$V_{io}$</td>
<td>Input offset voltage</td>
<td>2 mV</td>
<td>±3 mV</td>
<td>±3 mV</td>
<td>±5 mV</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common mode rejection ratio</td>
<td>90 dB</td>
<td>90 dB</td>
<td>94 dB</td>
<td>86 dB</td>
</tr>
<tr>
<td>GBP</td>
<td>Gain bandwidth product</td>
<td>1 MHz</td>
<td>8 MHz</td>
<td>1.8 MHz</td>
<td>4 MHz</td>
</tr>
</tbody>
</table>

In all of these applications, the power supply to the op-amp should be decoupled by connecting 1 microfarad capacitors at the power supply pins of the op-amp to the ground.

**8.16.1 DC Non-inverting Amplifier**

The circuit in Fig. 8.54 is a non-inverting amplifier that can amplify DC. The gain is $1 + \frac{R_2}{R_1} = 1 + \frac{100 \, k}{1 \, k} = 101$. If $R_1 = 1.01 \, k$, then the gain is 100.

If the source is another op-amp circuit with a direct connection, then the bias needed will be supplied by that circuit. In that case, the (low-frequency) input impedance of the circuit is the open-loop resistance multiplied by the loop gain which can be very high. If a direct path to the driving circuit is not available, then a resistor $R_B = 100 \, k$ must be connected between the non-inverting input and ground to provide the bias. In such a case, the input impedance is now 100 k.
Ideas for Exploration: (i) Convert the circuit into a variable gain amplifier by replacing resistor $R_2$ by a 100 k potentiometer with the feedback connection to the inverting terminal coming from the wiper of the potentiometer. With this arrangement the gain can be varied from 1 to 101. (ii) Introduce offset nulling in order to minimize offset voltage at the output. Consult the manufacturer’s literature on implementing this.

8.16.2 AC Non-inverting Amplifier

The circuit in Fig. 8.55 is an AC non-inverting amplifier. A bias resistor $R_B = 100 \, \text{k}$ is included as there is no other DC path to provide a bias current. The gain is $1 + \frac{100 \, \text{k}}{1 \, \text{k}} = 101$. For a low-frequency response down to 20 Hz, the input coupling capacitor value is given by $C = \frac{1}{2} \times \pi \times 20 \times 10^5 = 0.08 \, \mu\text{F}$. A value of $C = 0.1 \, \mu\text{F}$ is used. A coupling capacitor at the output may be necessary if the amplifier is expected to connect to a circuit which has DC that may be affected. A similar value capacitor connected at the output will suffice.
Ideas for Exploration: (i) Convert the circuit into a variable gain amplifier by replacing resistor $R_2$ by a 100 k potentiometer with the feedback connection to the inverting terminal coming from the wiper. With this arrangement, the gain can be varied from 1 to 101. (ii) Introduce a capacitor $C_2$ as shown Fig. 8.56 in order to introduce 100% DC feedback that will enhance DC stability.
8.16.3 Bootstrapped AC Amplifier

In the circuit in Fig. 8.56, by moving the resistor $R_B$ to the position shown in Fig. 8.57, this resistor is effectively bootstrapped. As a result, the low-frequency input impedance goes from $Z_i = 100 \, k$ to $Z_i = 100 \, k \times \text{loop gain} = 100 \, k \times 10^3 = 100 \, M$ where loop gain is given by open-loop gain/closed-loop gain. Capacitor $C_2$ is calculated by ensuring that its reactance at the lowest frequency under consideration is small compared with $R_B$. Using 1 Hz, we have $C_2 = \frac{1}{2} \times \pi \times 1 \times 10^5 = 1.6 \, \mu F$. The gain of the system continues to be 101.

Fig. 8.56  AC non-inverting amplifier with 100% DC feedback

Ideas for Exploration: (i) Convert the circuit into a variable gain amplifier by replacing resistor $R_2$ by a 100 k potentiometer with the feedback connection to the inverting terminal coming from the wiper. With this arrangement the gain can be varied from 1 to 101.
8.16.4 DC Voltage Follower

This circuit in Fig. 8.58 is that of a voltage follower which responds down to DC. It is derived from the non-inverting amplifier by setting $R_2 = 0$ and removing $R_1$. The output follows the input to within a few millivolts, and this can be further improved by using offset nulling. Since this constitutes 100% feedback, i.e., $\beta = 1$, the input impedance is at its highest value. Specifically, the open-loop input impedance of the 741 which is $1 \, \text{M}$ is increased by the factor of the loop gain $A\beta = 10^5$ to $1 \, \text{M} \times 10^5 = 10^{11} \, \Omega$.

![Fig. 8.58 DC voltage follower](image)

Idea for Exploration: (i) Modify the DC voltage follower to create an AC voltage follower as shown in Fig. 8.59a. Here, a larger value of $R_B$ is used since the input impedance to the non-inverting input is because of the feedback being very high. (ii) Modify the AC circuit to increase the input impedance as shown in Fig. 8.59b.
This circuit in Fig. 8.60a is an inverting amplifier. It has a gain $-R_2/R_1 = -100 \text{k}/10 \text{k} = -10$. Unlike the non-inverting case, the input impedance is $R_1 = 10 \text{k}$ which is comparatively low. The output signal is out of phase with the input signal. In order to reduce any voltage offset at the output, a resistor $R_3 = R_1//R_2 = 9 \text{k}$ is placed between the non-inverting terminal and ground as shown in Fig. 8.60b.
Ideas for Exploration: (i) Convert the circuit into a variable gain amplifier by replacing resistor $R_2$ by a 1 M potentiometer in series with a 10 k resistor as shown in Fig. 8.61. With this arrangement, the gain can be varied from $-1$ to $-100$.

8.16.6 Modified Inverting Amplifier

A modification of the inverting amplifier is shown in Fig. 8.62. Here, the voltage feedback signal is obtained from the potential divider.
comprising $R_3$ and $R_4$. The voltage gain for this circuit is given by

$$-\frac{R_2}{R_1} \left( 1 + \frac{R_4}{R_3} \right) = -101.$$ 

Because of the presence of the potential divider $R_3$ and $R_4$, larger resistor values can be used for $R_1$ and $R_2$, thereby enabling a larger input impedance $R_1 = 1 \text{ M}$.

![Diagram of modified inverting amplifier](image)

**Fig. 8.62** Modified inverting amplifier

**Ideas for Exploration:** (i) Convert the circuit into a variable gain amplifier by replacing resistor $R_4$ by a variable 100 k resistor. With this arrangement, the gain can be varied from $-1$ to $-101$. Note, however, that at low gains, $R_3$ will be a load on the op-amp, and hence may have to be increased.

### 8.16.7 AC Inverting Amplifier

This inverting amplifier processes AC by the inclusion of coupling capacitors $C_1$ and $C_2$ as shown in Fig. 8.63. These capacitors block any DC and ensure that only AC passes through the amplifier. Using a lower cutoff frequency of 20 Hz and noting the input impedance to the amplifier is $R_1 = 10 \text{ k}$, then capacitor $C_1$ is given by
\[ C_1 = \frac{1}{2} \times \pi \times 20 \times 10^4 = 0.8 \, \mu F. \] A value of 1 \, \mu F is suitable for both capacitors.

Fig. 8.63  AC inverting amplifier

*Ideas for Exploration*: (i) Convert the circuit into a variable gain inverting amplifier by replacing resistor \( R_2 \) by a 1 M potentiometer in series with a 10 k resistor as shown in Fig. 8.61 for the DC case. With this arrangement, the gain can be varied from −1 to −100.

8.16.8 Differential Amplifier

The circuit in Fig. 8.64 is that of a differential amplifier. It has a gain \(-R_2/R_1 = -100 \, k/10 \, k = -10\) and an output given by \( V_o = -10(V_1 - V_2)\). If all resistors are made equal say 100 k, then the circuit would have unity gain and would be that of a subtractor with output given by \( V_o = V_2 - V_1 \).
This circuit shown in Fig. 8.65 is that of a DC voltmeter. It uses the 741 op-amp in a voltage-to-current configuration since the meter is included in a current-series feedback loop. Thus, the current $I_m$ through the meter $M$ is sampled by resistor $R_m$ across which a feedback voltage is developed that is applied in series with the input voltage $V_i$. The result is that the ratio $I_m/V_i$ is stabilized because of the feedback and the current $I_m$ through the meter is simply $I_m = V_i/R_m$. The input impedance to the non-inverting input is already high without feedback (1 MΩ) and is increased by the feedback. With $R_m = 100$ Ω, full-scale deflection with a 1 mA milliammeter occurs with $V_i = 100$ mV. Diodes $D_1$ and $D_2$ along with resistor $R_{10} = 10$ kΩ protect the input of the op-amp from excessive voltage, while diodes $D_3$ and $D_4$ in conjunction with resistor $R_{11} = 3.3$ kΩ protect the meter from current overload. The resistor chain $R_1$ to $R_9$ forms an attenuator that provides a voltage range 0.1–1000 V in nine ranges. These values are as follows: $R_1 = (680$ kΩ + 120 kΩ), $R_2 = 100$ kΩ, $R_3 = (68$ kΩ + 12 kΩ), $R_4 = 10$ kΩ, $R_5 = (6.8$ kΩ + 1.2 kΩ), $R_6 = 1$ kΩ, $R_7 = (680$ Ω + 120 Ω), $R_8 = 100$ Ω and $R_9 = 100$ Ω. Finally, any
offset voltage must be reduced to zero, and this is done using potentiometer $VR_1$, while the input leads are shorted together.

![DC voltmeter](image)

*Fig. 8.65 DC voltmeter*

**Ideas for Exploration:** (i) Convert the circuit into a current meter by connecting a resistor $R_C$ across the input terminals as shown in Fig. 8.66. The current to be measured is passed through this resistor, and the choice of $R_C$ is given by $R_C = 0.1 \text{ V}/I_{mx}$ where $I_{mx}$ is the maximum
Thus, for a 1 mA range, $R_C = 0.1/1 \text{ mA} = 100 \Omega$, or for a 100 μA range, $R_C = 0.1/100 \text{ μA} = 1 \text{k}$.

**Fig. 8.66** Modification for conversion to current meter

### 8.16.10 High-Impedance DC Voltmeter

The circuit shown in Fig. 8.67 is a high-impedance voltmeter using a MOSFET op-amp the CA3140E. It uses essentially the same basic configuration as that in Fig. 8.65. Thus using $I_m = V_i/R_m$, for $V_i = 0.1 \text{ V}$ and $I_m = 100 \text{ μA}$, then $R_m = V_i/I_m = 0.1 \text{ V}/100 \text{ μA} = 1 \text{k}$. No meter protection circuitry is used in this design. The resistor chain $R_1$ to $R_9$ of Fig. 8.65 forms an attenuator that provides a voltage range 0.1–1000 V in nine ranges. The resistor values are as follows: $R_1 = (6.8 \text{ M} + 1.2 \text{ M})$, $R_2 = 1 \text{ M}$, $R_3 = (680 \text{ k} + 120 \text{ k})$, $R_4 = 100 \text{ k}$, $R_5 = (68 \text{ k} + 12 \text{ k})$, $R_6 = 10 \text{ k}$, $R_7 = (6.8 \text{ k} + 1.2 \text{ k})$, $R_8 = 1 \text{ k}$ and $R_9 = 1 \text{ k}$. Also, any offset voltage must be reduced to zero, and this is done using potentiometer $VR_1 = 10 \text{k}$, while the input leads are shorted together. Resistor $R_{10} = 1 \text{ M}$ and capacitor $C_1 = 10 \text{ nF}$ form a low-pass filter to remove high-frequency noise from the signal.
Ideas for Exploration: (i) Convert the circuit into a current meter by connecting a resistor $R_C$ across the input terminals as shown in Fig. 8.66. The current to be measured is passed through this resistor, and the choice of $R_C$ is given by $R_C = 0.1 \ V / I_{mx}$ where $I_{mx}$ is the maximum current. Thus, for a 1 mA range, $R_C = 0.1/1 \ mA = 100 \ \Omega$, or for a 100 $\mu$A range, $R_C = 0.1/100 \ \mu$A = 1 k.

8.16.11 Stable Voltage Reference

A stable reference voltage can be realized using an op-amp and a 5.6 V Zener. In Zener diodes below about 5.6 V, the Zener effect discussed in Chap. 1 is predominant, as a result of which the device exhibits a negative temperature coefficient. For devices above this voltage, the avalanche effect also discussed in Chap. 1 is the major operating effect, and this is marked by a positive temperature coefficient. In a 5.6 V diode, the two effects approximately cancel each other with the result that the device exhibits a temperature-stable voltage. This device is used in creating a very stable voltage reference as shown in Fig. 8.68. The voltage from the 5.6 V Zener diode $D_1$ is applied at the non-inverting input of the op-amp which is connected in the non-inverting configuration with a modest gain giving an output of $5.6(1 + R_2/R_1) = 6.6 \ V$. Feedback ensures that the output voltage is accurate and stable. Current to the Zener is supplied from the stabilized
output of the op-amp through a constant current diode (CCD). This enhances system performance since the supply is stable and any residual ripple is reduced by the CCD. The voltage output needs to be higher than the Zener voltage so that there is a minimum voltage across the CCD. Line regulation for this circuit is better than 0.005%, and the ripple rejection is greater than 80 dB.

Fig. 8.68 Stable voltage reference

Idea for Exploration: (i) Use the LM336 reference diode from Texas Instruments instead of a 5.6 V Zener in a voltage reference circuit. This diode provides 2.5 V, has a low temperature coefficient, and operates from 400 μA to 10 mA with a low dynamic resistance.

8.16.12 Linear Scale Ohmmeter

The circuit in Fig. 8.69 is that of an ohmmeter that has a linear scale. In this circuit, a stable reference voltage from the 5.6 V Zener $D_1$ (with current supplied by $R_1 = 2.2$ kΩ) is developed via the transistor across resistor $R_2 = 1$ kΩ. This voltage which is approximately 5 V drives the inverting amplifier through range resistors $R_3 = 1$ kΩ, $R_4 = 10$ kΩ, $R_5 = 100$ kΩ, and $R_6 = 1$ MΩ. These along with the feedback resistor $R_x$ which is the resistor to be measured set the gain of the amplifier. The output of the op-amp drives a 1 mA meter in series with $R_7 = 2.7$ kΩ and $VR_1 = 5$ kΩ. The
output of the op-amp is given by \( V_o = \frac{R_x}{R_R} V \) where \( R_R \) represents one of the range resistors. It follows that the output voltage is proportional to \( R_x \) the resistance to be measured. In order to calibrate the instrument, resistor \( R_x \) is set equal to the value of the selected range, for example, \( R_x = 10 \text{ k} \) on the 10 k range \((R_4 = 10 \text{ k} \text{ selected})\). Then the op-amp will be set for unity gain and will, therefore, output approximately 5 V. \( VR_1 \) is adjusted for full-scale deflection on the 1 mA meter. If high precision resistors (2% tolerance) are used for the range resistors, then all the ranges will be calibrated following this procedure on one range. Resistor \( R_8 = 1 \text{ k} \) reduces offset voltage of the op-amp. Zener diode \( D_2 \) with voltage 5.6 V along with \( R_9 = 1 \text{ k} \) protects the meter by limiting the voltage across the meter during over-range conditions.

![Linear scale ohmmeter diagram](image)

**Fig. 8.69** Linear scale ohmmeter

*Ideas for Exploration*: (i) The CA3140 op-amp is a direct replacement for the 741 and can operate on voltages down to 4 V either
single or dual supply. Use one of these op-amps to replace the 741 and use another to design a split supply to enable operation from a single 9 V battery.

8.16.13 AC Voltmeter

The circuit shown in Fig. 8.70 is that of a simple AC voltmeter. The meter is placed in a diode bridge $D_1$ to $D_4$ to allow the measurement of AC signals. Diode $D_5$ protects the meter from over-current, while capacitor $C_2 = 10 \ \mu F$ provides filtering to remove ripples from the current through the meter. Offset nulling may not be necessary in this circuit because of the presence of the diodes. Resistors $R_{m1}$ to $R_{m4}$ enable variation of voltage ranges. Thus using $I_m = V_i/R_m$, for $V_i = 0.1 \ V$ and $I_m = 1 \ mA$, then $R_{m1} = V_i/I_m = 0.1 \ V/1 \ mA = 100 \ \Omega$. Similarly, $R_{m2} = 1 \ k$ for $V_i = 1 \ V$, $R_{m3} = 10 \ k$ for $V_i = 10 \ V$ and $R_{m4} = 100 \ k$ for $V_i = 100 \ V$. Resistor $R_B = 100 \ k$ provides bias to the non-inverting input of the op-amp, and capacitor $C_1 = 1 \ \mu F$ couples the AC signal to the input.
Ideas for Exploration: (i) Convert this circuit to an AC/DC instrument by removing $C_1$ and applying the input voltage directly to the non-inverting terminal.

8.16.14 High-Impedance AC Voltmeter

The circuit of Fig. 8.71 uses a 741 op-amp in the non-inverting configuration to realize a high-impedance AC voltmeter. The 100 μA microammeter is placed in a diode bridge $D_1$ to $D_4$ to allow the measurement of AC signals, while diode $D_5$ protects the meter from over-current. These diodes can be 1N914 small-signal silicon diodes. Capacitor $C_3 = 10 \mu F$ provides filtering to remove ripples from the current through the meter. Potentiometer $VR_1 = 5 \, k$ is used for
calibration of the meter, and $R_{10} = 1 \, k$ limits the minimum resistance across the microammeter. Using $I_m = V_i/R_m$, for $V_i = 0.1 \, V$ and $I_m = 100 \, \mu A$, then $R_m = V_i/I_m = 0.1 \, V/100 \, \mu A = 1 \, k$. Bias resistor $R_B = 100 \, k$ is bootstrapped, thereby significantly increasing the input impedance of the instrument. The resistor chain $R_1$ to $R_9$ from the DC voltmeter project (Fig. 8.65) but with values $R_1 = (6.8 \, M + 1.2 \, M)$, $R_2 = 1 \, M$, $R_3 = (680 \, k + 120 \, k)$, $R_4 = 100 \, k$, $R_5 = (68 \, k + 12 \, k)$, $R_6 = 10 \, k$, $R_7 = (6.8 \, k + 1.2 \, k)$, $R_8 = 1 \, k$, and $R_9 = 1 \, k$ forms an attenuator that provides a voltage range $0.1–1000 \, V$ in nine ranges. Capacitor $C_1 = 1 \, \mu F$ is a coupling capacitor to remove DC from the input signal, while capacitor $C_2 = 100 \, \mu F$ provides the bootstrapping action.

![Fig. 8.71 High-impedance AC voltmeter](image)

### 8.16.15 Howland Current Pump

The Howland current pump (Fig. 8.72) is a voltage-controlled current source that delivers a current that is independent of the load into which the current is being delivered and is dependent on the controlling voltage to the system. The system comprises an op-amp with voltage-
series feedback to its inverting terminal and a resistive feedback connection to the non-inverting terminal. The load $R_L$ is connected to the non-inverting terminal. For the balance condition $R_4/R_3 = R_2/R_1$, the output current $I$ is given by $I = V_i/R_1$. The output impedance is given by $Z_T = R_1//R_2\left(1 + \frac{A}{1+R_2/R_1}\right)$. The low-frequency output impedance is $Z_T(\text{DC}) = R_1//R_2\left(1 + \frac{A_o}{1+R_2/R_1}\right)$. For example, with $R_1 = R_2 = R_3 = R_4 = 1$ k and using an op-amp with $A_o = 10^5$, then $Z_T(\text{DC}) = 10^3//10^3(1 + 10^5/2) \approx 25$ M.

![Howland current pump](image_url)

*Fig. 8.72* Howland current pump


### 8.16.16 Alternative Current Pump
A current pump that does not require a balance condition and achieves a higher output impedance than the Howland current pump is shown in Fig. 8.73. It comprises an op-amp whose output current \( I \) to the load flows through a resistor \( R \), thereby developing a voltage \( IR \) across this resistor. This floating voltage is detected by a unity-gain instrumentation amplifier at its differential inputs and delivered as feedback to the inverting input of the op-amp. Noting that \( V_o = (V_i - V_f)A \), \( V_o = I(R + R_L) \) and \( V_f = IR \), then the output current \( I \) is given by \( I = \frac{V_i}{1 + R_L/A_R} \). As \( A \to \infty \), \( I = \frac{V_i}{R} \). Thus, the high gain of the op-amp ensures that the output current \( I \) is independent of the load \( R_L \) and dependent only on the input voltage and the resistor \( R \). By grounding the input and applying a voltage source at the output, the output impedance \( Z_T \) of the circuit is found to be \( Z_T = R(1 + A) \). The low-frequency output impedance \( Z_T(DC) = R(1 + A_o) \). For example, with \( R = 1 \, \text{k} \) and using an op-amp such as the 741 with \( A_o = 10^5 \), then \( Z_T(DC) = 10^3 \, (1 + 10^5) = 100 \, \text{M} \). This output impedance for this circuit is higher than that achievable in the Howland current pump which (for comparable resistor values) is 25 M.

*Fig. 8.73* Alternative current pump

*Ideas for Exploration*: (i) Introduce gain in the instrumentation amplifier and examine the effect on the performance of the circuit.

**8.16.17 AC/DC Universal Voltmeter**
The circuit of Fig. 8.74 is a voltmeter that can measure both AC and DC signals. It also uses a MOSFET op-amp the CA3140E in the same basic configuration as that in Fig. 8.67. Here, however, the meter is placed in a diode bridge $D_1$ to $D_4$ to allow the processing of AC signals. Diode $D_5$ protects the meter from over-current, while capacitor $C_1 = 10 \mu F$ provides filtering to enable a smooth meter response. Potentiometer $VR_1 = 5 \text{k}$ along with $R_{10} = 1 \text{k}$ is used to calibrate the instrument. No offset nulling is necessary in this circuit because of the presence of the diodes. Thus using $I_m = V_i/R_{mv}$ for $V_i = 0.1 \text{ V}$ and $I_m = 100 \mu A$, then $R_m = V_i/I_m = 0.1 \text{ V}/100 \mu A = 1 \text{k}$. The resistor chain $R_1$ to $R_9$ from Fig. 8.65 with values $R_1 = (6.8 \text{ M} + 1.2 \text{ M})$, $R_2 = 1 \text{ M}$, $R_3 = (680 \text{ k} + 120 \text{ k})$, $R_4 = 100 \text{ k}$, $R_5 = (68 \text{ k} + 12 \text{ k})$, $R_6 = 10 \text{ k}$, $R_7 = (6.8 \text{ k} + 1.2 \text{ k})$, $R_8 = 1 \text{ k}$, and $R_9 = 1 \text{k}$ forms an attenuator that provides a voltage range $0.1\text{–}1000 \text{ V}$ in nine ranges.

![Fig. 8.74 AC/DC universal voltmeter](image)

**Ideas for Exploration:** (i) Introduce a polarity detector by taking the output of the op-amp to a comparator driving two leds.

### 8.16.18 Op-Amp with Transformer-Coupled Output

Op-amps have specified output voltage and current capability. For example, the 741 can deliver a peak output voltage of about $12 \text{ V}$ and a peak output current of about $25 \text{ mA}$ when operated from a $\pm15 \text{ V}$ supply. It, therefore, cannot directly drive a low-impedance load such as an $8 \Omega$ speaker since the maximum peak current demand would be $12$
\[
\frac{V}{8 \Omega} = 1.5 \text{ A which exceeds the maximum current rating of the device.}
\]

One method of addressing this is to use a step-down transformer between the output of the op-amp and the speaker as shown in Fig. 8.75. Let the peak output voltage of the op-amp be \(V_{opk}\) and the peak voltage into the speaker from the transformer be \(V_{spk}\). Then

\[
\frac{V_{opk}}{V_{spk}} = n
\]

where \(n\) is the transformer turns ratio. From transformer principles, \(I_{opk}/I_{spk} = 1/n\) where \(I_{opk}\) and \(I_{spk}\) are the peak output current of the op-amp and the peak current into the speaker from the transformer, respectively. Let \(C_f = g_m R_B C_f\) and \(V_{spk}/I_{spk} = R_L\). Then,

\[
\frac{R'_L}{R_L} = n^2 \quad \text{and} \quad n = \sqrt{\frac{R'_L}{R_L}}.
\]

With this turns ratio, an impedance \(R_L\) at the output of the transformer secondary is reflected as \(R'_L\) at the input of the transformer primary. This limits the output current of the op-amp to its rated output current when delivering its rated output voltage. Thus, for the 741, \(R'_L = 12\ \text{V}/25\ \text{mA} = 480\ \Omega\) and \(R_L = 8\ \Omega\) giving

\[
n = \sqrt{480/8} = 7.7.
\]

Use \(n = 8\). Therefore, a step-down transformer with a turns ratio \(n = 8\) will enable the full voltage and current capacity of the 741 op-amp to be delivered to the 8 \(\Omega\) speaker. The average power to the speaker is then

\[
P = \frac{V_{opk} I_{opk}}{\sqrt{2}} = 12 \times 25 \text{ mA}/2 = 150 \text{ mW}.
\]

If the speaker is connected directly to the output of the op-amp, then the maximum power that can be delivered to the load is limited by the maximum current available from the op-amp and is given by

\[
(I_{opk}/\sqrt{2})^2 \times R_L = (0.025/\sqrt{2})^2 \times 8 = 2.5 \text{ mW}.
\]
Ideas for Exploration: (i) Design a transformer-coupled system using an op-amp powered by ±12 V to drive an 8 Ω loudspeaker and determine the full power into that load; (ii) Repeat the design with a 15 Ω load.

8.16.19 Op-Amp Transistor Gain Tester

The circuit shown in Fig. 8.76 is that of a transistor gain tester using an op-amp. Resistor $R_1 = 1$ k supplies the 10 V zener diode $D_1$ with a current of $(18 - 10)/1.2$ k = 6.7 mA. The Zener diode in conjunction with resistors $R_2 = 4.7$ k and $R_3 = 5.3$ k sets a fixed voltage $V_{ref} = 5.3$ V at the inverting terminal of the op-amp and, therefore, 4.7 V across $R_2$. Resistor $R_3$ can be realized using standard values 15 k and 8.2 k in parallel. The output of the op-amp supplies current to the base of the transistor $Tr_x$ under test through a resistor $R_5$ which provides some protection for the transistor during overload. This base current is measured by the 100 μA microammeter in series with the base. The collector of the transistor is connected to the power supply through $R_4$ and also to the non-inverting input of the op-amp. The voltage 4.7 V across resistor $R_2$ is now effectively placed across $R_4$ by the action of the op-amp. By setting $R_4 = 4.7$ k, this results in a 1 mA current through $R_4$ and into the collector of the transistor. Feedback action via the op-amp turns on the transistor to allow this collector current to flow. The base current $I_m$ measured by the microammeter then allows the
transistor current gain $\beta$ to be determined using $\beta = 1000/I_m$ where $I_m$ is in microamperes. Resistor $R_3$ can be a 4.7 k resistor and diode $D_2$ is a small-signal diode also for meter protection. The circuit can be powered by two 9 V batteries and the op-amp supply terminals are connected directly across the zener supply.

**Fig. 8.76** Transistor gain tester

*Ideas for Exploration:* (i) Explain the reason that feedback around the op-amp is applied to the non-inverting and not the inverting terminal; (ii) Re-design the system to enable the current-gain testing of pnp transistors; (iii) Re-design the system to use a single 9 V battery and a suitable low-voltage op-amp.

**8.16.20 Research Project 1**

The circuit shown in Fig. 8.77 is that of a constant volume amplifier. It provides an approximately constant amplitude output signal for varying input signal amplitude by incorporating a system of automatic gain control. This circuit is useful in reducing the dynamic range of music and other signals without introducing significant distortion. Resistor $R_5 = 1$ M grounds the gate of the JFET and $R_3 = 330$ k along with the drain voltage set the drain current such that the operating point is in the ohmic region. The drain-source resistance in conjunction with $R_3 = 330$ k provides the dynamic adjustment of the op-amp
feedback that results in automatic gain control. The JFET operates as a voltage-controlled resistor with the control voltage being derived from the output signal of the op-amp. This signal is rectified by diode $D_1$ on the negative half-cycle, filtered by $R_4$ and $C_1$ and this negative voltage applied at the gate of the JFET. Thus, for low-level signals, the amplitude of this negative voltage is low, and hence the drain-source resistance is a few hundred ohms. This means that the feedback signal at point A is low and, therefore, amplifier gain is high and the output of the op-amp is at a reasonable level. When the signal amplitude is large, the amplitude of this negative voltage increases and this increases the drain-source resistance of the JFET, as a result of which the feedback signal at point A is high thereby reducing the circuit gain and across $R_3$, and hence the output of the op-amp is reduced to a reasonable level. Capacitor $C_2$ eliminates DC offset voltages from the output signal. The project is to design the circuit.

![Constant volume amplifier](image)

**Fig. 8.77** Constant volume amplifier

*Ideas for Exploration:* (i) Determine the dynamic range of the circuit by applying a signal of increasing amplitude and recording the
corresponding output amplitude changes. A large input signal amplitude change will produce a reduced amplitude change at the output. (ii) Experiment with different values of $R_3$ and $C_1$ and determine the response of the circuit to these changes.

### 8.16.21 Research Project 2

This project involves the design of a **Baxandall tone control circuit** that was introduced in Chap. 7 using discrete transistors. Here, the project is to design this system around the 741 op-amp as shown in Fig. 8.78, using the theory of the Baxandall tone control employed in Chap. 7. The signal driving the Baxandall tone control network enters at A and may come from an op-amp pre-amplifier. The output of the network at B enters the inverting input of the op-amp. Feedback from the output of the op-amp is applied to the network at B. Potentiometer $VR_B$ lifts/cuts the bass frequencies, while potentiometer $VR_T$ lifts/cuts the treble frequencies. The project involves researching Baxandall tone control theory and designing the network.

![Baxandall tone control](image)

**Fig. 8.78** Baxandall tone control

*Ideas for Exploration: (i) Design a pre-amplifier circuit using a 741 op-amp with a suitable gain to drive the tone control circuit. (ii) Refer to the article The Texan 20 + 20 W IC Stereo Amplifier by Richard Mann, Parts 1 to 4, Practical Wireless, May 1972, p 48 to August 1972, p 318.*
8.16.22 Research Project 3
This project requires the design of an **RIAA pre-amplifier** using an op-amp as shown in Fig. 8.79. The signal from a phonograph disk (record) has a characteristic in which the high frequencies have a higher amplitude than the low frequencies. Because of this, the pre-amplifier for such a signal must possess a frequency response characteristic that is exactly the inverse of this. The standard developed by the Record Industry Association of America (RIAA) for magnetic phonograph cartridges that establishes the exact nature of this equalization characteristic was discussed in Chap. 7. The characteristic comprises poles at 50 and 2100 Hz and a zero at 500 Hz. A practical implementation of this using a 741 op-amp is shown in Fig. 8.79. It uses the op-amp in a non-inverting configuration with a CR network in the signal feedback loop which creates the RIAA equalization characteristic. The standard input resistance for magnetic pickups is 47 k as shown in the diagram.

![Fig. 8.79 RIAA pre-amplifier](image)

8.16.23 Research Project 4

A common problem when playing old records is scratches on the vinyl surface which generate high-frequency noise. This project involves the design of a **scratch filter** to remove this noise as was discussed in Chap. 7, but here using a 741 op-amp. The system is shown in Fig. 8.80. It comprises two connected RC networks with one capacitor grounded and the other connected to the output of the buffer. The transfer function for this system with $R_1 = R_2 = R$ and $C_1 = C$, $C_2 = 2C$ is given by

$$ \frac{V_o}{V_i} = \frac{1}{1 + \sqrt{2}j\frac{f_c}{f_c} + \left(j\frac{f_c}{f_c}\right)^2} $$

(8.124)

where

$$ f_c = \frac{1}{2 \sqrt{2\pi}RC} $$

(8.125)

![Scratch filter using op-amp](image)

This is a second-order response referred to as a Butterworth response that has the characteristic of being maximally flat. With an appropriately placed corner frequency $f_c$, unwanted high-frequency signals produced by vinyl scratches can be eliminated. For an upper cutoff frequency of 10 kHz, using $C = 2.2$ nF, Eq. (8.125) gives $R = 4.7$ k.

**Ideas for Exploration:** (i) Minimize DC offset by introducing a resistor in the feedback connection between the output of the op-amp and the inverting terminal.

8.16.24 Research Project 5
Using the voltage follower op-amp configuration, explore the development of a **rumble filter** that removes unwanted low-frequency (less than 50 Hz) components from an audio signal as discussed in Chap. 7. The two filter network resistors and the two network capacitors in Fig. 8.80 must be interchanged. Resistor $R_1$ which is part of the filter network also provides bias to the non-inverting input of the op-amp. The op-amp filter is shown in Fig. 8.81 and the associated transfer function with $C_1 = C_2 = C$ and $R_1 = R$, $R_2 = R/2$ is given by

$$
\frac{V_o}{V_i} = \frac{(j\frac{f}{f_c})^2}{1 + \sqrt{2}j\frac{f}{f_c} + (j\frac{f}{f_c})^2}
$$

(8.126)

where the corner frequency is

$$
f_c = \frac{\sqrt{2}}{2\pi RC}
$$

(8.127)

![Fig. 8.81 Rumble filter using op-amp](image)

This is a Butterworth response for the high-pass filter.

*Ideas for Exploration:* (i) Minimize DC offset by introducing a resistor in the feedback connection between the output of the op-amp and the inverting terminal.

### 8.16.25 Research Project 6

This project is an **experimental electronic thermometer** that uses a silicon diode such as the 1N4148 as a temperature sensor. This is
possible because the voltage across such a device decreases with temperature by 2 mV for every degree rise in temperature, i.e., −2 mV/°C. The system is shown in Fig. 8.82 where the diode $D_1$ is in the feedback loop of an op-amp OPA1. A constant voltage $V_x$ is developed across voltage divider $R_1, R_2$, and $VR_1$ and is available at the wiper of potentiometer $VR_1$. This voltage is applied at the non-inverting terminal of OPA1 resulting in a constant current $V_x/R_3 ≈ 2mA$ through the diode and a voltage $V_A = V_x + 0.7 + \Delta V$ at the output of OPA1. Here, 0.7 V is the nominal voltage across the diode and $\Delta V = −2\Delta T$ is the voltage change due to temperature rise $\Delta T$. The differential amplifier OPA2 subtracts voltage $V_A = V_x + 0.7 + \Delta V$ at the output of OPA1 from a fixed voltage $V_B = V_x + 0.7$ available at the junction of $R_1$ and the potentiometer giving $V_o = (V_B - V_A)R_5/R_4 = −6.8\Delta V = 13.6\Delta T mV$ at the output of the differential amplifier. Here, we have used $R_4 = 1k$ and $R_5 = 6.8k$ in order to provide some amplification of the result of the subtraction. This voltage then drives a microammeter $M_1$ through a resistor $R = R_6 + VR_2$ resulting in a current $I_m = V_o/R = 13.6\Delta T/R$. If $VR_2$ is adjusted such that $R = 13.6k$, then $I_m = \Delta T \mu A$. This can be accomplished by setting $R_6 = 10k$ and adjusting $VR_2 = 10k$. Thus potentiometer $VR_1$ is adjusted to give $I_m = 0$ at $T = 0 °C$ and potentiometer $VR_2$ is adjusted to give $I_m = 100 \mu A$ at $T = 100 °C$. The op-amps are supplied power from ±9 V regulated supplies and the +9 V drives the potential divider.
**Ideas for Exploration:** (i) Explore the design of an electronic thermometer using the LM335 temperature sensor. This device has a linear temperature characteristic of 10 mV/K and is calibrated to give 2.73 V at 0°C (273 K).

**Problems**
1. For each of the circuits shown in Fig. 8.83, determine $V_o$.
2. Design an inverting amplifier with a voltage gain of $-5$.
3. Design an inverting amplifier with a voltage gain of $-8$ and an input resistance of 10 k.
4. Design a non-inverting amplifier with a voltage gain of 8.
5. Design a non-inverting amplifier with a voltage gain of 8 and an
input resistance of 150 kΩ.

6. A non-inverting amplifier has \( R_1 = 5 \, \text{k}\Omega \) and \( R_2 = 25 \, \text{k}\Omega \). Determine the gain of the system.

7. Configure an op-amp circuit to realize the operation \( V_O = 5 \, V_1 - 2 \, V_2 \). If a third input was added to the differential amplifier such that \( V_O = 5 \, V_1 - 2 \, V_2 + 3 \, V_3 \), realize such a circuit using a single op-amp.

8. Design a non-inverting amplifier with a gain of 12 using an op-amp that operates from a single-ended 15 V supply.

9. Design an inverting amplifier with a gain of −9 using an op-amp that operates from a single-ended 18 V supply.

10. Show that the closed-loop bandwidth of a unity-gain stable op-amp is equal to the open-loop bandwidth multiplied by the loop gain. Such an operational amplifier has a \( GBP = 20 \, \text{MHz} \). Determine the closed-loop bandwidth for gains of (a) 10 and (b) 50.

11. A (unity-gain stable) op-amp has a \( GBP = 8 \, \text{MHz} \). Determine the gain for a bandwidth of 1 MHz.

12. A (unity-gain stable) op-amp has an open-loop bandwidth of 20 Hz and a low-frequency open-loop gain of 120 dB. Determine the GBP of the device.

13. A particular op-amp has an input resistance \( R_i = 1 \, \text{M}\Omega \), \( R_o = 100 \, \Omega \) and open-loop DC gain \( A_o = 2000 \). Estimate the error in the gain of this op-amp if used as an inverting amplifier, when \( R_1 = 1 \, \text{k}\Omega \) and \( R_2 = 10 \, \text{k}\Omega \). Repeat for the case \( R_1 = 1 \, \text{M}\Omega \) and \( R_2 = 10 \, \text{M}\Omega \). Which choice of resistors results in a lower gain error while maintaining the same gain?

   For the transimpedance amplifier of Fig. 8.84, show that the input
14. For the transimpedance amplifier of Fig. 8.84, show that the input impedance as seen to the right of the source is given by
\[ R_i = R_2/(1 + A_o). \] If \( R_2 = 10 \text{ k} \) and \( A_o = 1000 \), determine the range of \( R_s \) such that the output voltage \( V_o \) deviates from its ideal value by 1\%.

15. The circuit shown in Fig. 8.85 contains a floating load and has the characteristics of an ideal current amplifier. Show that for this circuit \( i_o \) and \( i_i \) are related by
\[ i_o \approx - \left(1 + \frac{R_2}{R_1}\right) i_i. \] Determine the input impedance as seen at the inverting terminal of this amplifier.

16. Consider the variable gain difference amplifier shown in Fig. 8.86 where resistor \( R_G \) is used to change the gain. Show for this amplifier, the output voltage is given by
\[ V_o = \frac{2R_2}{R_1} \left(1 + \frac{R_2}{R_G}\right)(V_2 - V_1). \]

17. An ideal CFA has \( Z_o = 5 \text{ M} \) and \( f_o = 1 \text{ kHz} \). Determine the closed-loop gain and closed-loop bandwidth in the inverting and non-inverting configurations for \( R_1 = 1 \text{ k} \) and \( R_2 = 10 \text{ k} \).

18. An op-amp has a SR of 5 V/\( \mu \text{s} \) and a maximum output voltage swing of ±8 V. Determine the full power bandwidth \( BW_p \). What is the maximum voltage output the device can deliver at 500 kHz?

19. A CFA has the characteristics \( f_o = 7.5 \text{ kHz} \), \( Z_o = 4.5 \text{ M} \) and \( r_x = 50 \Omega \). Determine the value of the feedback resistor \( R_2 \) in order to achieve a closed-loop bandwidth of 10 MHz. For this value of feedback resistor in the inverting configuration, determine the value of the input resistor \( R_1 \) in order to achieve a gain of −10.

20. Design a transformer coupled op-amp amplifier in the non-inverting configuration powered by a ±15 V supply to drive a 4 Ω loudspeaker and determine the full power into that load. Assume the maximum output voltage is 12 V and the maximum output
the maximum output voltage is 14 V and the maximum output current is 25 mA.

Fig. 8.83 Circuits for Question 1
Fig. 8.84  Circuit for Question 14

Fig. 8.85  Circuit for Question 15
Fig. 8.86 Circuit for Question 16

Bibliography
9. Power Amplifiers

An amplifier is a device for receiving a signal at its input and delivering a larger signal at its output. They are used in a wide range of applications including music systems, in driving industrial loads, and elsewhere. In small-signal amplifiers, the active devices are operated such that the voltage and current changes are small and the devices are operated in their approximately linear regions. In such amplifiers, the main factors are amplifier linearity, gain, and noise performance.

Large-signal amplifiers, also called power amplifiers, experience relatively large changes in current and voltage and are usually expected to deliver large amounts of power to an external load. This class of amplifiers usually range from hundreds of milliwatts to hundreds of watts. The features that characterize such amplifiers are power output, gain, load rating, and total harmonic distortion. In this chapter, we consider the operation of power amplifiers and how to design working power amplifier circuits. At the end of the chapter, the student will be able to:

- Explain the operation of transistor power amplifiers.
- Explain the operation of different classes of power amplifiers.
- Design transistor power amplifiers using several topologies.
• Utilize power amplifier integrated circuits.

9.1 Amplifier Classes
Amplifiers may be classified by class, i.e., the extent the active output devices of the amplifiers conduct while delivering an output. In a class A amplifier, the output device(s) conducts for the complete waveform cycle, i.e., 360°. In a class AB amplifier, the output devices conduct for more than half of the signal cycle but less than the complete cycle, i.e., more than 180° but less than 360°. Therefore, the output device turns off for a brief period during the cycle in which case, another device must conduct and deliver the output signal. In a class B amplifier, the output device conducts for half of the signal cycle, i.e., 180°, and turns off for the other half of the cycle. In order to reproduce a complete signal, two such amplifiers must be connected to the load. These will conduct alternatively so that the full cycle is reproduced. A class C amplifier is one in which the output device conducts for less than half-cycle, i.e., 180°. It is difficult to fully reproduce a complete wave cycle with such an amplifier and distortion is the result. A class D amplifier is one in which the output device is alternatively fully on or fully off.

9.2 Fixed-Bias Class A Amplifier
The common-emitter fixed-bias amplifier discussed in Chap. 2 actually operates in class A since the device never turns off during the signal cycle. This same arrangement may be used as a power amplifier by replacing the small-signal transistor by a power transistor as shown in Fig. 9.1.
A signal at the input of the amplifier causes the collector current of the transistor to change, and hence an output voltage is developed across $R_L$ the load resistor. Class A operation follows from the fact that a DC bias is established in the transistor with the device operating along the DC “load line” as shown in Fig. 9.2. The Q point represents the DC voltage and current in the transistor when no signal is present. As is evident, the transistor is always on as movement up and down the load line occurs in response to an input signal.
The signal power in $R_L$, $P_L$ is given by

$$P_L(AC) = \frac{1}{T} \int_{0}^{T} i_C^2 R_L dt \tag{9.1}$$

The peak value of the maximum collector AC current is given by

$$A_V = \frac{V_o}{V_i} = g_m R_L \tag{9.2}$$

and occurs when the transistor is symmetrically biased. Under these conditions, the maximum AC power to the load becomes

$$\tag{9.3}$$
\[ P_L(AC)_{\text{max}} = \left( \frac{i_{\text{pk}} \text{(max)}}{\sqrt{2}} \right)^2 R_L = \left( \frac{V_{\text{CC}}}{2 \sqrt{2} R_L} \right)^2 R_L = \frac{V_{\text{CC}}^2}{8 R_L} \]

In low-power audio systems, a loudspeaker is sometimes the load resistor \( R_L \), and the low impedance (8 \( \Omega \)) gives the load line a very steep slope. However, while the system quiescent current will be permanently passing through the loudspeaker, changes in the value of this current as a result of signal input to the transistor result in audio output from the speaker. Consider the common-emitter amplifier in Fig. 9.3 where an 8 \( \Omega \) loudspeaker has replaced the load resistor in Fig. 9.3 and a moderate quiescent current of say \( I_C = 100 \text{ mA} \) flows in the transistor collector. This current results in a voltage drop across the speaker of \( I_C R_L = 100 \text{ mA} \times 8 \text{ \( \Omega \)} = 0.8 \text{ V} \) which, with a supply voltage of 12 \( \text{ V} \), cannot result in maximum symmetrical swing. For maximum symmetrical swing, the load resistance would need to be 6 \( \text{ V} / 100 \text{ mA} = 60 \text{ \( \Omega \)} \). It is possible to achieve this with the 8 \( \text{ \( \Omega \)} \) speaker by using a transformer, and this is discussed in the next section. For the current arrangement, the maximum symmetrical change \( \Delta I_C \) in the collector current is \( \Delta I_{\text{pk}} = 100 \text{ mA} \), i.e., a minimum \( I_C \) of zero and a maximum \( I_C \) of 200 \( \text{ mA} \). While this causes only a small change in the collector voltage of the transistor, power is delivered to the speaker, and is given by

\[ P_L(AC) = \left( \frac{\Delta I_{\text{pk}}}{\sqrt{2}} \right)^2 R_L = \left( \frac{0.1}{\sqrt{2}} \right)^2 \times 8 = 40 \text{ mW} \]

There is, however, significant power dissipation in the transistor which may have to be mounted on a heatsink in order to prevent overheating. This approach was explored in a research project in Chap. 5, and we can now outline the design process.
Example 9.1 Using the configuration in Fig. 9.3 and a transistor with a current gain of 50, design a low-power amplifier to deliver 75 mW into an 8 Ω load using a 9 V supply.

Solution Using Eq. (9.3), the peak collector current change required to produce 75 mW in an 8 Ω speaker is given by 

\[ \left( \frac{\Delta I_{Cpk}}{\sqrt{2}} \right)^2 \times 8 = 75 \times 10^{-3}. \]

This yields \( \Delta I_{Cpk} = 137 \) mA and, therefore, the quiescent current in the power transistor needs to be about 150 mA. The value of \( R_B \) required is given by \( 9 = I_B R_B + 0.7 \) where 

\[ I_B = I_C/50 = 0.15 \text{ A}/50 = 3 \times 10^{-3}. \]

Hence \( R_B = (9-0.7)/I_B = 8.3/3 \times 10^{-3} = 2.8 \text{ k} \).

Example 9.2 If the 8 Ω speaker in the above amplifier is replaced by a 15 Ω speaker, calculate the output power.
**Solution**  In this circuit with a 15 Ω speaker, the power output is given by
\[
\left( \frac{\Delta I_{C_{pk}}}{\sqrt{2}} \right)^2 \times R_L = \left( \frac{137 \text{ mA}}{\sqrt{2}} \right)^2 \times 15 = 141 \text{ mW}
\]. Thus, if the 8 Ω speaker is replaced by a 15 Ω speaker, the power output increases from 75 to 141 mW.

This basic power amplifier system is subject to an effect referred to as thermal runaway. As the system operates, the transistor heats up and the collector current increases. This causes increased heat dissipation in the transistor which causes further increase in collector current. This self-reinforcing cycle may eventually result in the failure of the transistor. Various strategies are available to prevent this phenomenon from occurring. A simple method is to use collector-base feedback biasing which requires that the bias resistor \( R_B \) be returned to the collector of the transistor instead of the power supply. The result is that any increase in collector current with temperature will cause an increased voltage drop across the speaker which in turn results in a reduction in the collector voltage of the transistor. The result is that the base current flowing through \( R_B \) is reduced thereby reducing the collector current. Higher values of speaker resistance enhance this collector current stabilizing action.

Further improvement of this circuit can be realized by replacing the power transistor with a power Darlington or power MOSFET (which does not suffer from thermal runaway) that results in a higher input impedance and the addition of a preamplifier stage to increase the sensitivity of the overall system. This enhanced arrangement using a power Darlington is shown in Fig. 9.4.
Because of the low resistance of the speaker, the voltage drop across it is low \((0.15 \times 8 = 1.2 \text{ V})\), and therefore, most of the supply voltage would be dropped across the transistor. This does not allow for maximum (symmetrical) swing of the collector voltage. This can be corrected by the use of a step-down transformer in the collector circuit such that a greater impedance is reflected in the collector circuit of the output transistor. This will be discussed under transformer-coupled amplifiers.

### 9.2.1 Efficiency Calculations

Power amplifiers act as power converters as they deliver large amounts of power to a load. They are driven by an input signal and convert power available from a power supply (input or DC power) to useful signal output power in the load (AC power). The efficiency of the amplifier \(\eta\) is a measure of the effectiveness of this conversion and is given by

\[
\eta = \frac{P_{AC}}{P_{DC}} \times 100\%
\]

where \(P_{AC}\) is the output power delivered to the load and \(P_{DC}\) is the input DC power from the supply. In general, not all of \(P_{DC}\) is converted to \(P_{AC}\) i.e., \(\eta < 100\%\), and the component of the input power that is not converted to AC output power is dissipated as heat in the active output devices.
Example 9.3  A power amplifier has an efficiency of 20% and delivers an output power of 25 W to a resistive load. Calculate the power dissipated and the DC input power to the amplifier.

Solution

\[ G_1 = -g_{m1}R_L \cdot \therefore P_{DC} = \frac{P_{AC}}{\eta} \times 100 = \frac{25 \times 100}{20} = 125 \text{ W}. \]

Hence power dissipated \( P_{\text{dis}} \) is given by \( P_{\text{dis}} = 125 \text{ W} - 25 \text{ W} = 100 \text{ W}. \)

Example 9.4  A large signal amplifier delivers an output power of 5 W and consumes 20 W from the associated DC supply. Calculate its efficiency.

Solution

\[ \eta = \frac{P_{AC}}{P_{DC}} \times 100 = \frac{5}{20} \times 100 = 25\%. \]

Power considerations are extremely important in large-signal amplifiers because of the large voltages and currents involved. For example, a power transistor will be destroyed if its power dissipation capacity is exceeded. In small-signal amplifiers, it was noted that the Q-point must lie below the maximum dissipation rating if the transistor is not to be destroyed. Here we explore new rules to ensure safe operation in power amplifiers.

The average power dissipated by any device is given by

\[ P_{\text{AVG}} = \frac{1}{T} \int_{0}^{T} V(t)i(t)dt \quad \text{(9.5)} \]

where \( V(t) \) is the voltage across the device, \( i(t) \) is the current through it, and \( T \) is the period of the time-varying portion of \( V \) or \( i \). For the fixed-bias Class A amplifier, the average power \( P_{DC} \) delivered by the power supply, neglecting the small power associated with the bias, is given by

\[ P_{DC} = \frac{1}{T} \int_{0}^{T} V_{CC}i_C dt = \frac{1}{T} \int_{0}^{T} V_{CC} (I_C + i_C(t)) dt = V_{CC}I_C \quad \text{(9.6)} \]
where \( i_c \) is the signal component and \( I_C \) is the DC component of \( i_C \). The power dissipated in the transistor \( P_c \) is calculated using

\[
P_c = P_{DC} - P_{AC}
= P_{DC} - \frac{1}{T} \int_0^T i_C^2 R_L dt
= P_{DC} - \frac{1}{T} \int_0^T (I_C + i_c)^2 R_L dt
= P_{DC} - I_C^2 R_L - \frac{1}{T} \int_0^T i_c^2 R_L dt
\]  

(9.7)

From this equation, it can be seen that maximum power dissipation in the transistor occurs when the signal current \( i_c \) is zero which corresponds to no signal present, in which case,

\[
P_{c(max)} = V_{CEq} I_{Cq}
\]  

(9.8)

The peak voltage across the load is \( V_{CC}/2 \), and hence the maximum power dissipated in the load is

\[
P_{AC max} = \frac{(V_{CC}/2 \sqrt{2})^2}{R_L}
\]

Therefore, the maximum efficiency \( \eta_{max} \) is given by

\[
\eta_{max} = \frac{P_{AC max}}{P_{DC}} \times 100 = \frac{V_{CC}^2/8R_L}{V_{CC}I_C} \times 100
\]  

(9.9)

Since \( I_C = \frac{V_{CC}/2}{R_L} \),

\[
\eta_{max} = \frac{V_{CC}^2}{8R_L} \times 100 = \frac{V_{CC}^2}{2R_L} \times 100 = 25\%
\]  

(9.10)

This means that the maximum efficiency of the class A common-emitter amplifier is 25%.

### 9.3 Transformer-Coupled Class A Amplifier

In order to increase the efficiency, the DC power dissipated in the load \( R_L \) may be reduced by coupling the load to the transistor using a step-down transformer as shown in Fig. 9.5.
Assuming the resistance of the transformer primary is zero, then the DC load line is vertical, passing through $V_{CC}$ on the $V_{CE}$ axis as shown in Fig. 9.6. Because of the transformer, the load $R_L$ seen by the transistor collector is given by

$$1 + \frac{R_2}{R_1} = 3$$  \hspace{1cm} (9.11)

where $n$ is the turns ratio of the transformer. With this arrangement, a larger output voltage swing for the same collector current change can be realized as compared with the case where $R_L$ was placed in the collector circuit. In fact, the AC load line intercepts $V_{CE}$ axis at a value greater than $V_{CC}$. The value of $\overline{R_L}$ determines the slope of the AC load line. If $\overline{R_L}$ is chosen such that $V_{CEp_k} = 2V_{CC}$ and $I_{Cp_k} = 2I_{Cq}$, then

maximum symmetrical swing is possible. Then, input power is given by $V_{CC}I_{Cq}$ and output power (AC) is given by $\frac{V_{CC}}{\sqrt{2}} \times \frac{I_{Cq}}{\sqrt{2}}$. Hence

$$1 + \frac{R_2}{R_1} = 3$$  \hspace{1cm} (9.12)
The output voltage in this arrangement is able to exceed the supply voltage because of the inductive effect of the transformer primary as shown in the AC load line of Fig. 9.6. Thus, the maximum efficiency of a transformer-coupled amplifier is 50%, which is twice as good as the efficiency of the class A amplifier with the load in the collector where there was DC power dissipation in the load. Again, for the transformer-coupled case, the maximum transistor dissipation occurs when there is no signal present and is given by

\[ P_C = V_{CEq} I_{Cq} = \frac{V_{CC}^2}{R_L} \]  \hspace{1cm} (9.13)

since \( V_{CEq} = V_{CC} \) and \( I_{Cq} = \frac{V_{CC}}{R_L} \).

**Example 9.5** Using the configuration shown in Fig. 9.5, design a transformer-coupled amplifier delivering 1 W into 8 Ω and operating
from a 20 V supply. Use a power Darlington with $\beta = 1000$.

**Solution**  The power into the load is given by

$$P_L = \frac{\left(\frac{V_{pk}}{\sqrt{2}}\right)^2}{R_L}$$

where $V_{pk}$ is the peak voltage across the speaker from the output of the transformer secondary. Thus, for 1 W output into 8 $\Omega$,

$$1 = \left(\frac{V_{pk}}{\sqrt{2}}\right)^2 / 8$$

which yields $V_{pk} = 4$ V and $I_{pk} = 4$ V/8 = 0.5 A. Since the power supply is 20 V, the peak change in collector voltage is $\Delta V_{CEpk} = 20$ V. This is the input signal voltage to the transformer primary in the collector. Hence the transformer turns ratio $n$ to realize this is $n = \Delta V_{CEpk} / V_{pk} = 20 / 4 = 5$. (Alternatively, the power supply voltage may be varied to accommodate a different transformer turns ratio.) The peak signal current into the transformer primary is $\Delta I_{Cpk} = I_{pk} / n = 0.5$ A/5 = 100 mA. Therefore, $I_{Cq} = \Delta I_{Cpk} = 100$ mA. Hence, noting that the Darlington transistor has a base-emitter voltage of 1.4 V, the fixed-bias resistor is calculated from

$$20 = R_B I_C / \beta + 1.4 = R_B \times 0.1 \text{ A}/30 + 1.4$$

giving $R_B = 186$ k. Note that the power supplied to the system is $V_{CC} I_{Cq} = 20 \text{ V} \times 0.1 \text{ A} = 2$ W which is double the output power of 1 W corresponding to 50% efficiency.

A preamplifier can also be used with this system to increase sensitivity as shown in Fig. 9.7. In this configuration, resistor $R_2$ ensures bias stability in the output stage, and $R_3$ provides feedback bias to $Tr_1$. 
Example 9.6  Using the configuration shown in Fig. 9.7, design a transformer-coupled amplifier delivering 1 W into $8 \, \Omega$ and operating from a 20 V supply. Use a power Darlington with $\beta = 1000$.

Solution  From Example 9.6 for 1 W output into $8 \, \Omega$, $V_{pk} = 4 \, V$ and $I_{pk} = 4 \, V/8 = 0.5 \, A$, where $V_{pk}$ is the peak voltage across the speaker from the output of the transformer secondary. Since the power supply is 20 V, if we allow 2 V at the emitter of $Tr_2$ for bias stability in the output stage, then the peak change in collector voltage is $\Delta V_{CEpk} = (20 - 2) = 18 \, V$. This is the input signal voltage to the transformer primary in the collector. Hence the transformer turns ratio $n$ to realize this is $n = \Delta V_{CEpk}/V_{pk} = 18/4 = 4.5$. Alternatively, the power supply voltage may be varied to accommodate a different transformer turns ratio. The peak signal current into the transformer primary is $\Delta I_{Cpk} = I_{pk}/n = 0.5 \, A/4.5 = 111 \, mA$. Therefore, $I_{Cq} = \Delta I_{Cpk} = 111 \, mA$. Resistor $R_2$ is given by $R_2 = 2 \, V/111 \, mA = 18 \, \Omega$. The base current of the Darlington is 111 mA/1000 = 0.11 mA. This must be supplied by the collector of $Tr_1$.
Choosing the collector current $I_{C1}$ in $Tr_1$ to be greater than 10 times this current, we use $I_{C1} = 2$ mA. Noting that the Darlington transistor has a base-emitter voltage of 1.4 V, the voltage at the collector of $Tr_1$ is 3.4 V. Therefore, resistor $R_1$ is found from $R_1 = (20-3.4)/2$ mA = 8.3 k. The base current of $Tr_1$ is given by $I_{C1}/100 = 2$ mA/100 = 20 μA. Therefore, the bias resistor $R_3$ is calculated from $R_3 = (2-0.7)/20$ μA = 65 k.

### 9.4 Class B Push–Pull Amplifier

In the class A amplifier considered earlier, the maximum efficiency was 50%. Part of the reason for this is the fact that in class A, the active device(s) is always on, even when no signal is present. Hence there is continuous heat dissipation in this device. In the class B amplifier, the active device conducts for only half of the signal cycle, and therefore, greater efficiency is possible. In order to provide full cycle conduction to the load in such circumstances, it is necessary to have at least two active devices, which will conduct for alternative half-cycles. Such an arrangement is traditionally called push–pull based on circuits used in the past. A modern approach to implementing such a design is by the use of a complimentary symmetry emitter follower as shown in Fig. 9.8.
The action of the circuit is as follows: when the input voltage $V_i$ is at zero, then $V_o$ is zero. When $V_i$ goes positive, the emitter follower action of $Tr_1$ causes $V_o$ to go positive, thereby resulting in a flow of current into $R_L$ from $Tr_1$. $Tr_2$ remains off during this positive half-cycle. When $V_i$ goes negative, $V_o$ goes negative by emitter follower action of $Tr_2$, and current flows out of the load into $Tr_2$. $Tr_1$ is off during this half-cycle. Thus $Tr_1$ supplies the load current during the positive half-cycle, while $Tr_2$ sinks the load current during the negative half-cycle.

Each transistor, therefore, operates for only approximately half of the signal cycle—class B. When the input signal is at zero, both transistors are off since $V_{BE} = 0$ for both and only a tiny leakage current flows. Therefore, as $V_i$ goes positive, $Tr_1$ must first turn on, i.e., the input voltage must exceed 0.7 V the threshold voltage. As a result, for the
early part of the positive half-cycle, $V_o$ remains zero until $V_i \geq 0.7$ such that $Tr_1$ turns on. After turn-on, $V_o$ then follows $V_i$. The effect is that part of the input voltage is not reproduced. This occurs when $V_i$ is increasing above zero and decreasing to zero.

Similarly, for the negative half-cycle, for $|V_i| < 0.7$, $V_o = 0$ and again part of the input signal is lost. The total effect is shown in Fig. 9.9, and the resulting distortion is called crossover distortion since it occurs as the delivery of the signal output $V_o$ crosses over from one transistor to the other. This distortion can be substantially reduced by biasing the transistors on as shown in Fig. 9.10 (class AB) such that when $V_i = 0$, both transistors are on with a small current $I_{Cq}$. In such a case, as $V_i$ goes positive since $Tr_1$ is already on, no turn on is required and $V_o$ immediately follows $V_i$. A similar action takes place on the negative half-cycle with $Tr_2$ already on. The overall effect is that the crossover distortion is eliminated as a smooth transition from one transistor to the other occurs.

![Fig. 9.9 Crossover distortion](image)
A simple method of forward biasing $Tr_1$ and $Tr_2$ is the use of forward-biased diodes as shown in Fig. 9.11. The resistors $R$ provide current to the diodes as well as the transistor bases. The diodes provide the bias voltage for the transistors and provide temperature stability for $I_{cq}$. For a transistor, $V_{BE}$ decreases with increasing temperature according to

$$\frac{\Delta V_{BE}}{\Delta T} \approx -2.5 \text{ mV/}^\circ\text{C}$$

\hspace{10cm} (9.14)
Since the voltage across a diode varies in approximately the same way, by placing $D_1$ and $D_2$ in physical contact with $Tr_1$ and $Tr_2$, $I_{cq}$ can be maintained approximately constant. By decreasing $R$, the voltage across the diodes is increased, and this in turn increases the base-emitter voltage of the transistors. $I_{cq}$, therefore, increases. This increase in $I_{cq}$ moves the amplifier into class AB and usually reduces the amount of cross over distortion. The optimum value of $I_{cq}$ is normally found experimentally by adjusting $I_{cq}$ for the minimum distortion. Since increase in $I_{cq}$ increases the heat dissipated in the transistors, a minimum $I_{cq}$ for minimum harmonic distortion is sought.

For the push–pull class B circuit, the power delivered by the supply $V_{CC}$ is
If \( I_{D(on)} \) during the positive half-cycle is given by

\[
i_c(t) = I_{C_{\text{max}}} \sin \omega t,
\]

then Eq. (9.15) becomes

\[
P_{CC1} = V_{CC} \frac{1}{T} \int_0^T i_c(t)dt
\]

Assuming symmetrical supplies, then \( I_{sc} = -h_feI_b \), and the total power \( P_{CC} \) supplied by the two supplies becomes

\[
P_{CC} = \frac{2}{\pi} V_{CC} I_{C_{\text{max}}}
\]

where \(|+V_{CC}| = |-V_{CC}| = V_{CC}\). The power delivered to \( R_L \) is

\[
P_L = \frac{1}{2} I_{C_{\text{max}}}^2 R_L
\]

The maximum power delivered to the load \( P_{L_{\text{max}}} \) is

\[
P_{L_{\text{max}}} = \frac{1}{2} \left( \frac{V_{CC}}{R_L} \right)^2 R_L = \frac{V_{CC}^2}{2R_L}
\]

The power \( P_D \) dissipated in the two transistors \( Tr_1 \) and \( Tr_2 \) is the difference between the power delivered by the power supply and the power delivered to the load, i.e.,

\[
P_D = P_{CC} - P_L = \frac{2}{\pi} V_{CC} I_{C_{\text{max}}} - \frac{1}{2} R_L (I_{C_{\text{max}}}^2)
\]

In order to determine the value of \( I_{C_{\text{max}}} \) for maximum dissipation, \( P_D \) is differentiated with respect to \( I_{C_{\text{max}}} \) and the result set to zero giving,

i.e.
\[ I_{C_{\text{max}}} = \frac{2V_{CC}}{\pi R_L} \]  \hspace{1cm} (9.21)

Substituting Eq. (9.21) into Eq. (9.20), we get

\[ P_D = \frac{2}{\pi} V_{CC} \left( \frac{2V_{CC}}{\pi R_L} \right) - \frac{1}{2} R_L \left( \frac{2V_{CC}}{\pi R_L} \right)^2 \]
\[ = \frac{1}{2} R_L \left( \frac{2V_{CC}}{\pi R_L} \right)^2 = \frac{2V_{CC}^2}{\pi^2 R_L} \]  \hspace{1cm} (9.22)

Hence each transistor must dissipate half of this energy, i.e., \( P_T = \frac{V_{CC}^2}{\pi^2 R_L} \). We note that

\[ \frac{P_{L_{\text{max}}}}{P_T} = \frac{V_{CC}^2}{2R_L} / \frac{V_{CC}^2}{\pi^2 R_L} = \frac{\pi^2}{2} = 4.93 \approx 5 \]  \hspace{1cm} (9.23)

Therefore, \( P_T \approx \frac{1}{5} P_{L_{\text{max}}} \) which means that in a class B amplifier, the maximum power dissipated in each transistor is 1/5 the power dissipated in the load. The efficiency \( \eta \) is given by

\[ \eta = \frac{P_L}{P_{CC}} \times 100 = \frac{1}{2} \frac{I_{C_{\text{max}}} R_L}{V_{CC}} \times 100 = \frac{\pi I_{C_{\text{max}}} R_L}{4 V_{CC}} \times 100 \]  \hspace{1cm} (9.24)

This is a maximum when \( I_{C_{\text{max}}} = \frac{V_{CC}}{R_L} \) giving \( \eta = 78.5\% \).

There are several characteristics which define the performance of a power amplifier. Some of these are discussed below:

**Power rating** in watts is a measure of the power output that can be delivered by the amplifier into a particular load, usually 8 or 4 \( \Omega \) for domestic amplifiers. The formula \( P = \frac{V_{rms}^2}{R_L} \) gives the continuous average power sometimes (erroneously) referred to as RMS power. The output power into 8 \( \Omega \) for a typical domestic power amplifier is of the order of 100 W. It is interesting to note that for the same amplifier output voltage, the power output into 4 \( \Omega \) is twice that into 8 \( \Omega \) since the current into the lower resistance increases. The **Gain** of an amplifier is the ratio of the output voltage amplitude to the input voltage amplitude and is usually measured in decibels. Thus the gain \( G \) in decibels is given by \( G \text{ dB} = 20 \log \left( \frac{V_{out}}{V_{in}} \right) \) where \( V_{in} \) is the amplitude
of the input voltage and $V_{out}$ is the amplitude of the output voltage. The gain of many amplifier circuits is between 10 and 50. The sensitivity is the input signal level in volts required to drive the amplifier to its full rated power output and for an amplifier can be about 1 V. The frequency response of an amplifier is a measure of the range of signal frequencies that the amplifier will reproduce at the rated gain within certain gain limits. Hi-fi amplifiers typically have a frequency response of 20 Hz to 20 kHz ±3 dB. Total harmonic distortion or THD is a measure of the amount of distortion of the input signal arising as a result of the addition by the amplifier of harmonics of the input signal to the output signal. It is usually given as a percentage and can range from about 0.001% to about 0.1% for high fidelity amplifiers, the lower the better. Finally, signal-to-noise ratio or SNR is the ratio of the desired signal level to the noise level at the output of the amplifier. This ratio is normally expressed in decibels.

### 9.5 Low-Power Amplifier Design

The low-power amplifier configuration shown in Fig. 9.12 is our first example of a practical power amplifier. It utilizes complimentary symmetry at the output based on transistor pairs in the emitter follower configuration and a common-emitter stage. Transistor $Tr_1$ is connected in a common-emitter configuration with its output developed across $R_2$. Because of the heavy current demand, medium power transistors are used in the emitter follower configuration to couple the voltage at the collector of $Tr_1$ to the load. The complementary symmetry arrangement enables the circuit to function in class B with each output transistor delivering current to the load on alternative half-cycles. Two diodes $D_1$ and $D_2$ connected in series provide the bias voltage that turns on transistors $Tr_2$ and $Tr_3$. This results in 1.4 V appearing across the base-emitter junctions of $Tr_2$ and $Tr_3$, thereby turning these transistors on and as a result reducing crossover distortion. Resistors $R_3$ and $R_4$ are small high wattage resistors that help to stabilize the quiescent current $I_{Cq}$ in the output stage. Biasing for the voltage amplifier $Tr_1$ is set by the resistor $R_1$. 
which also provides signal feedback from the output to the input. A single-ended supply is employed, and hence a voltage of $V_{CC}/2$ sits at the output of the amplifier. This must be, therefore, coupled to the speaker load via a large electrolytic capacitor $C_2$. The input coupling capacitor $C_1$ is necessary to preserve the DC bias at the base of $Tr_1$. It is important to note that in this circuit, while on the negative half-cycle, $Tr_1$ sinks base current from $Tr_2$; while on the positive half-cycle, $R_1$ supplies base current to $Tr_3$. Thus this resistor must be carefully chosen to ensure that adequate current can be supplied.

Fig. 9.12  Low-power amplifier
Example 9.7 Using the configuration in Fig. 9.12 design a low-power amplifier that delivers 250 mW into an 8 Ω speaker. All the transistors are silicon.

Solution For \( P = 250 \text{ mW} \) into 8 Ω, using \( P = \frac{V^2}{2R_L} \),

\[
V_{pk} = \sqrt{P \times 2 \times R_L} = \sqrt{0.25 \times 2 \times 8} = 2 \text{ V}.
\]

\( I_{pk} = \frac{2}{8} = 250 \text{ mA} \). In order to allow for transistor saturation losses, use a 9 V supply. This can be conveniently supplied by a 9 V battery. For maximum symmetrical output, the quiescent voltage at the output of the power amplifier is \( V_{CC}/2 = 9/2 = 4.5 \text{ V} \). When the peak voltage across the load is +2 V corresponding to the amplifier driving current into the speaker, the amplifier’s DC output voltage is \( 4.5 + 2 = 6.5 \text{ V} \). Ignoring the small voltage drop across \( R_3 \), the voltage at the base of \( Tr_3 \) is \( 6.5 + 0.7 = 7.2 \text{ V} \). Hence using a 9 V supply, the voltage drop across \( R_2 \) is 9–7.2 = 1.8 V. At that point, the maximum current \( I_{pk} = 250 \text{ mA} \) flows into the load, and hence \( I_B(Tr_3) \) is at its maximum and given by \( I_b(Tr_3) = 0.25 \text{ A}/100 = 2.5 \text{ mA} \) where 100 is the approximate current gain of the transistor \( Tr_3 \).

Since this current is supplied by \( R_2 \), it follows that \( R_2 = 1.8 \text{ V}/2.5 \text{ mA} = 720 \text{ Ω} \). However, in order to ensure that \( R_2 \) can always supply the necessary, the peak output current requirement is increased by a factor of 1.5 to \( I_{pk} = 375 \text{ mA} \). Hence \( R_2 \) now becomes \( R_2 = 1.8 \text{ V}/3.75 \text{ mA} = 480 \text{ Ω} \). Resistors \( R_3 \) and \( R_4 \) must be chosen to maximize bias current stability (large), while minimizing power dissipation from signal current (small). A value between 2 and 3 Ω for each of these resistors is reasonable. The quiescent current in \( Tr_1 \) is given by

\[
I_{Cq}(Tr_1) = (9-4.5 - 0.7)/480 \Omega \approx 8 \text{ mA}.
\]

Hence, taking the current gain of \( Tr_1 \) to be 100, the base current \( I_b(Tr_1) = 8 \text{ mA}/100 = 80 \mu\text{A} \). This gives the base current in \( R_1 \) as 80 μA and hence

\[
R_1 = \frac{(9/2-0.7)}{80 \mu\text{A}} = 47.5 \text{ k}Ω.
\]

Because the value of \( R_1 \) depends so directly on the current gain of \( Tr_1 \), its value may have to be adjusted in order to set the amplifier quiescent output voltage at 4.5 V for maximum symmetrical output swing. Capacitor \( C_2 \) must be sufficiently large in order to achieve a satisfactory
low-frequency amplifier response. For a 100 Hz low-frequency response, $C_2$ is given by $C_2 = \frac{1}{2\pi} \times 100 \times 8 = 199 \ \mu F$. A value of 200 $\mu F$ is, therefore, chosen. The input impedance of the amplifier is approximately $h_{ie}$ for $Tr_1$ which is

$$h_{ie} = \frac{h_{fe}}{40I_C} = \frac{100}{(40 \times 8 \ mA)} \approx 300 \ \Omega.$$  Therefore, the value of the input capacitor $C_1$ is given by $C_1 = \frac{1}{2\pi} \times 100 \times 300 = 5.3 \ \mu F$. A value of the at least 10 $\mu F$ is chosen. Transistors $Tr_2$ and $Tr_3$ must be medium-power transistors having a collector current rating of at least 250 mA the peak load current, a collector-emitter voltage $BV_{CEO}$ of at least 9 V and power rating of one fifth the amplifier output power. In practice, significant overrating is employed in order to ensure adequate safety margins. Transistors MPSA05 and MPSA55 are very suitable. Transistor $Tr_1$ dissipates only very modest power. Also, the maximum current is about twice the quiescent current giving 16 mA. Almost any general purpose small-signal transistor such as the 2N3904 will suffice. Finally, diodes $D_1$ and $D_2$ can be 1N4148 silicon diodes.

A technique for improving the distortion performance of this amplifier is shown in Fig. 9.13a. It involves the *bootstrapping* technique applied to the resistor $R_2$ such that the resistance seen by the collector of $Tr_1$ is increased, and this results in an increase in the open-loop gain of the amplifier.
This resistor is split into two resistors $R_{2a}$ and $R_{2b}$ and a capacitor $C_3$ connected from the amplifier output to the junction of these two resistors. The effect is that bootstrapping action by the emitter follower $Tr_3$ around $R_{2b}$ via $C_3$ increases the effective value of this resistor for signals. Thus $R_{2b}$ becomes $R_{2b}/(1 - \rho)$ where $\rho$ is the voltage gain of $Tr_3$ given by $\rho = \frac{g_m R_E}{1 + g_m R_E}$ and $R_E$ is the resistance being driven by the transistor emitter which is 8 Ω. For a current in the output of 20 mA say, then $f_D = 1 = \frac{1}{2\pi R_A(C_A + C_C)}$, $R_{2b} \rightarrow R'_{2b} = R_{2b}/(1-0.86) = 7.4R_{2b}$. Using $R_{2b} = 240$ Ω then $R'_{2b} = 7.4 \times 240 = 1.8$ k. Note that resistor $R_{2a}$ is part of the load of the amplifier output and is in parallel with the speaker.
It is possible to eliminate capacitor $C_3$ by connecting the speaker in place of resistor $R_{2a}$ as shown in Fig. 9.13b and making resistor $R_{2b}$ equal to $R_2$. This popular configuration has the disadvantage of DC current always flowing through the speaker.

### 9.5.1 Power Supply

These and other power amplifiers to be discussed in this chapter can generally be powered by unregulated power supplies which are fully discussed in Chap. 10. These supplies can either be single-ended or bipolar. However, the low-power systems may be powered from a battery supply.

### 9.6 Medium-Power Amplifier Design

The power amplifier of Fig. 9.12 is restricted to the power of less than about 1 W. At higher-power levels, the increased current demand at the bases of the two output transistors necessitates a large bias current in transistor $Tr_1$ which is undesirable. For increased power output, the basic configuration can be modified as shown in Fig. 9.14. It utilizes complimentary Darlington pairs instead of normal transistors at the output to couple the voltage at the collector of $Tr_1$ to the load. The high current gain of these devices reduces the quiescent current level in $Tr_1$ while still enabling high output current. The *bootstrapping* technique involving resistor $R_2$ in the previous low-power amplifier may be applied here to good effect because of the higher input impedance presented by the Darlington pairs. Instead, a constant current source involving $Tr_4$ and its associated components is used. This circuit ensures that all the quiescent current in $Tr_1$ is available to drive $Tr_3$ during the positive half-cycle. More importantly, the combination of a current-source load and the high input impedance presented by the Darlington output pair results in a higher open-loop gain for the circuit. Significant voltage–shunt feedback is then applied via $R_2$ while $R_1$ ensures that this feedback is not short-circuited to ground by the input source.
Bias voltage for the Darlington pair may be a string of four diodes connected in series so that these on voltages appear across the four base-emitter junctions of the Darlington pair. This turns on the pair, thereby ensuring that crossover distortion is reduced. A diode string unfortunately does not permit easy variation of the bias voltage and the setting of the quiescent current in the output stage. A better approach is to use a $V_{BE}$ multiplier as shown in Fig. 9.15. This circuit acts as a variable Zener diode, producing reasonably wide variation in the voltage $V_Z$ across its terminals by varying $R_b$. In practice, $V_Z$ would be
varied until the quiescent current in the output transistors is between 10 and 100 mA or alternatively until crossover distortion is minimized.

![Variable Zener](image)

**Fig. 9.15** Variable Zener

**Example 9.8** Design a 10 W power amplifier using the configuration in Fig. 9.14 along with the variable Zener for biasing.

**Solution** For maximum symmetrical output, the quiescent voltage at the output of the power amplifier is $V_{CC}/2$. For $P = 10$ W into 8 Ω, using $V_{pk} = \sqrt{2PR_L}$, $V_{pk} = \sqrt{2 \times 10 \times 8} = 12.6$ V. In order to allow for transistor saturation losses, the peak voltage swing is set at $12.6 + 5 = 17.6$ V. Hence $V_{CC} = 2 \times 17.6 = 35$ V. The peak output current is given by $I_{pk} = 12.6/8 = 1.6$ A. Using a current gain of 1000 for each Darlington pair, the maximum output current results in maximum base currents for the Darlington of $I_b(Tr_{2,3})$ given by $I_b(Tr_{2,3}) = 1.6$ A/1000 = 1.6 mA. This current flows into the collector of $Tr_1$ during negative-going half-cycles or is supplied from the constant current flowing out of the collector of $Tr_4$ during positive-going half-cycles. However, in order to ensure that $Tr_4$ can always supply the necessary
current, the constant current is set at 5 mA which is more than three times the requirement for the base current to the Darlington pairs. Resistors $R_3$ and $R_4$ are chosen to maximize bias current stability while minimizing power dissipation from signal current. Since higher output currents are involved, the power dissipation is a greater problem than before. These resistors would, therefore, have to be smaller than in the low-power amplifier and a value between 0.2 and 0.3 $\Omega$ for each of these resistors is reasonable. The quiescent current in $Tr_1$ is equal to the current in the current source which is 5 mA. Hence, taking the current gain of $Tr_1$ to be 100, the base current $I_b(Tr_1) = 5 \text{ mA}/100 = 50 \mu\text{A}$. This gives the current in $R_2$ as 50 $\mu\text{A}$ and hence $R_2 = \frac{(17.5-0.7)}{50 \mu\text{A}} = 336 \text{ k}\Omega$. This value may need to be adjusted to set the output at 17.5 V. Resistor $R_6$ is calculated from $R_6 = 0.7/5 \text{ mA} = 140 \Omega$. To allow about 3 mA through $D_3$ and $D_4$, $R_5 = (35-1.4)/3 \text{ mA} = 11.2 \text{ k}\Omega$. For a 20 Hz low-frequency response, $C_2$ is given by $C_2 = 1/2\pi \times 20 \times 8 = 995 \mu\text{F}$. A value of 1000 $\mu\text{F}$ is, therefore, chosen. The input impedance at the base of $Tr_1$ is approximately $h_{ie}$ for $Tr_1$ which is $h_{ie} = h_{fe}/40I_C = 100/(40 \times 5 \text{ mA}) = 500 \Omega$. The feedback reduces it further. Therefore, the minimum value of the input capacitor $C_1$ is given by $C_1 = 1/2\pi \times 20 \times 500 = 15.9 \mu\text{F}$. A value of at least 20 $\mu\text{F}$ is chosen. The presence of $R_1$ further reduces this value. Darlington $Tr_2$ and $Tr_3$ must be power transistors having a collector current rating of at least 1.6 A the peak load current, a collector-emitter voltage $BV_{CEO}$ of at least 35 V and power rating of one fifth the amplifier output power. Complimentary Darlington transistors TIP 121 and TIP126 (80 V, 5 A, 65 W) are suitable. Transistors $Tr_1$ and $Tr_4$ can be small-signal transistors but must have a breakdown voltage of greater than 35 V. MPSA05 and MPSA55 are adequate. The $V_{BE}$ multiplier must provide at least 4 $V_{BE}$ drops across $Tr_2$ and $Tr_3$. Let $I_{Ra} = 1 \text{ mA}$. Then $R_a(Tr_5) = 0.7 \text{ V}/1 \text{ mA} = 700 \Omega$.

Hence $1 + \frac{R_b}{R_a} = \frac{2.4}{0.7} = 3.4$, $\frac{R_a}{R_b} = 2.4$, $R_b = 2.4 \text{ k}\Omega$. A 5 k potentiometer can be used for $R_b$ to enable adjustment of the quiescent current in $Tr_2$.
and \( Tr_3 \). A 2N3904 transistor can be used. Resistor \( R_1 \) at the input sets the overall voltage gain of the power amplifier. For a voltage gain of 20, \( R_1 \approx R_2/10 = 16.8 \, k \) (see Chap. 7). Because of the moderate open-loop gain of the circuit, \( R_1 \) may have to be reduced somewhat in order to achieve the desired gain of 10. Under test, the circuit performed as expected delivering 15 V peak into an 8 \( \Omega \) load which is equivalent to 14 W. Resistor \( R_2 \) was adjusted to 496 \( k \) in order to set the DC output voltage at 17.5 V. The 5 k potentiometer was adjusted to set the bias current in the output stage at about 14 mA. Finally, the circuit gain was set at –20 by adjusting \( R_1 = 16 \, k \). The frequency response was measured at 100 Hz to 20 kHz.

An improved non-inverting version of the power amplifier in Fig. 9.14 is shown in Fig. 9.16. An additional common emitter amplifying stage \( Tr_6 \) is introduced in the circuit. This stage provides further gain and allows the application of voltage-series feedback at the emitter of \( Tr_6 \) via \( R_2, R_1, \) and \( C_1 \). The Zener regulator \( D_3, D_4 \) provides regulated bias for the base of \( Tr_6 \) through potential divider \( R_9 \) and \( R_{10} \). This configuration requires a compensation capacitor, \( C_4 \) whose value is given by \( C_5 = \frac{g_m}{2\pi f_c A_v} \) where \( g_m = 1/(r_e(Tr_6) + R_1) \).
Example 9.9  Design a 25 W power amplifier using the configuration in Fig. 9.16.

Solution  For maximum symmetrical output, the quiescent voltage at the output of the power amplifier is $V_{CC}/2$. For $P = 25$ W into 8 Ω, using
\[ V_{pk} = \sqrt{2PR_L}, \quad V_{pk} = \sqrt{2 \times 25 \times 8} = 20 \text{ V}. \]

In order to allow for transistor saturation losses, the peak voltage swing is set at \( 20 + 5 = 25 \) V. Hence \( V_{CC} = 2 \times 25 = 50 \text{ V}. \) The peak output current is given by \( I_{pk} = 20/8 = 2.5 \) A. Using a current gain of 1000 for each Darlington pair, the maximum output current results in maximum base currents for the Darlington of \( I_B(T_{r2,3}) \) given by \( I_b(T_{r2,3}) = 2.5 \text{ A}/1000 = 2.5 \text{ mA}. \) This current flows into the collector of \( T_r1 \) during negative-going half-cycles or is supplied from the constant current flowing out of the collector of \( T_{r4} \) during positive-going half-cycles. However, in order to ensure that \( T_{r4} \) can always supply the necessary current, the constant current is set at 5 mA which is twice the requirement for the base current to the Darlington pairs. Resistors \( R_3 \) and \( R_4 \) are chosen to maximize bias current stability in the output stage while minimizing power dissipation from signal current. Since higher output currents are involved, the power dissipation is a greater problem than before. These resistors would, therefore, have to be smaller than in the low-power amplifier and a value between 0.2 and 0.3 \( \Omega \) for each of these resistors is reasonable. The quiescent current in \( T_r1 \) is equal to the current in the current source which is 5 mA. Hence, taking the current gain of \( T_r1 \) to be 100, the base current \( I_b(T_{r1}) = 5 \text{ mA}/100 = 50 \mu\text{A}. \) Since this current is supplied by \( T_{r6} \), the quiescent current in this transistor is set at say 0.5 mA. Hence \( R_7 = 0.7/0.5 \text{ mA} = 1.4 \text{ k}. \) Resistor \( R_6 \) is calculated from \( R_6 = 0.7/5 \text{ mA} = 140 \Omega. \) To allow about 3 mA through diodes \( D_1 \) and \( D_2, \) \( R_5 = (50-1.4)/3 \text{ mA} = 16.2 \text{ k}. \) For a 20 Hz low-frequency response into the 8 \( \Omega \) load, \( C_2 \) is given by \( C_2 = 1/2\pi \times 20 \times 8 = 995 \mu\text{F}. \) A value of 1000 \( \mu\text{F} \) is, therefore, chosen. The \( V_{BE} \) multiplier must provide at least \( 4V_{BE} \) drops across \( T_{r2} \) and \( T_{r3}. \) Let \( I_{Ra} = 1 \text{ mA}. \) Then \( R_a(T_{r5}) = 0.7 \text{ V}/1 \text{ mA} = 700 \Omega. \) Hence \[ 1 + \frac{R_b}{R_a} = \frac{2.4}{0.7} = 3.4, \quad \frac{R_a}{R_b} = 2.4, \quad R_b = 1.7 \text{ k}. \]

A 5 k potentiometer for \( R_b \) can be used to allow adjustment of the quiescent current in the output stage. Resistor \( R_2 \) along with resistor \( R_1 \) provides feedback to the emitter of the input transistor \( T_{r6}. \) Let \( R_2 = 4.7 \text{ k} \) say.
Then the voltage at the emitter of $Tr_6$ is $V_E(Tr_6) = 25 - 0.5 \text{ mA} (4.7 \text{ k}) = 22.7 \text{ V}$. This sets the voltage at the base of $Tr_6$ at $V_B(Tr_6) = 22.7 - 0.7 = 22 \text{ V}$. Using a current of 0.25 mA through resistors $R_9$ and $R_{10}$ to ensure bias voltage stability for $Tr_6$, then $R_{10} = 22/0.25 \text{ mA} = 88 \text{ k}$. Using two 18 V Zener diodes for $D_3$ and $D_4$, the Zener regulator would provide 36 V. Hence $R_9 = (36 - 22)/0.25 \text{ mA} = 56 \text{ k}$. Allowing 2 mA into $D_3$ and $D_4$ for proper operation, then $R_8 = (50 - 36)/2 \text{ mA} = 7 \text{ k}$. The input impedance of the amplifier is less than $R_9 // R_{10}$ which is 56 k//88 k = 32 k. Therefore, the value of the input capacitor $C_3$ can be found using $C_3 = 1/2\pi \times 20 \times 32 \text{ k} = 0.25 \mu\text{F}$. A value of 1 \mu\text{F} is then chosen since the input impedance at the base of $Tr_6$ while high because of voltage-series feedback introduced by $R_2$ and $R_1$ reduces the overall input impedance below 32 k. The gain of the amplifier is given by $1 + R_2//R_1$. Since $R_2 = 4.7 \text{ k}$ then for a gain of 20, $R_1 = 247 \Omega$. A small filter capacitor $C_6$ of about 0.1 \mu\text{F} can be used to reduce the effect of long power supply leads, while $C_5 = 1 \mu\text{F}$ improves the regulation of the Zener diodes. For an adequate low-frequency response, capacitor $C_1$ must be chosen such that its reactance is equal to $R_1$ at 20 Hz. Thus $C_1 = 1/2 \times \pi \times 20 \times 247 = 32 \mu\text{F}$. Capacitor $C_4$ introduces Miller compensation for circuit stability. For $Tr_6$, $I_C = 0.5 \text{ mA}$ and hence $r_e(Tr_6) = 1/40I_C = 50 \Omega$. Therefore using $f_c = 500 \text{ kHz}$, $A_V = 20$ and $g_m = 1/(r_e(Tr_6) + R_1) = 1/(50 + 247) = 1/297$ in Eq. (9.37), the values for capacitor $C_4$ is given by $C_4 = g_m/(2\pi f_c A_V) = 1/297 \times 2\pi \times 5 \times 10^{-5} \times 20 = 54 \text{ pF}$.

Darlingtonss $Tr_2$ and $Tr_3$ must be power transistors having a collector current rating of at least 2.5 A the peak load current, a collector-emitter voltage $BV_{CEO}$ of at least 50 V and power rating of one fifth the amplifier output power. Transistors TIP142 and TIP147 (100 V, 10 A, 125 W) can be used. Transistors $Tr_1$ and $Tr_4$ can be small-signal transistors but must have $BV_{CEO}$ of greater than 50 V. MPSA06 and MPSA56 (80 V, 500 mA, 1.5 W) are adequate. These transistors can also be used for $Tr_5$ and $Tr_6$. A simple but useful modification of this circuit is the use of a
Cascode amplifier in the second stage. This arrangement removes distortion caused by early effect, and thereby enhances the overall harmonic distortion performance of the amplifier particularly at high frequencies.

9.7 High-Power Amplifier Design

In the power amplifiers considered thus far, neither the input nor the output stages permit direct coupling. An enhanced power amplifier circuit that overcomes these problems is shown in Fig. 9.17. It comprises three amplifying stages: the input stage made up of the differential amplifier $Tr_1$ and $Tr_2$, the intermediate common-emitter stage $Tr_3$ with current source load $Tr_4$ and the complimentary symmetry emitter follower output stage using Darlington pairs $Tr_5$ and $Tr_6$. In the differential amplifier input stage, two pnp transistors $Tr_1$ and $Tr_2$ are connected at their emitters with resistor $R_2$ supplying current to these emitters from a Zener-regulated supply fed from the supply rail. Each transistor is basically in a common-emitter mode with resistor $R_3$ in the collector of $Tr_1$. This first stage produces a modest voltage gain. A signal applied at the base of amplifier $Tr_1$ is amplified and passed via $R_3$ to the second stage $Tr_3$. The common-emitter amplifier second stage with active load $Tr_4$ provides most of the voltage gain.
The complimentary symmetry emitter follower output stage of Darlington pairs $Tr_5$ and $Tr_6$ provides a high-impedance load to the collector of $Tr_3$ and low-impedance output drive to the speaker as before. The use of high-gain Darlington pairs reduces the current demands on the second stage and thereby reduces the required bias current in $Tr_3$. Also, the increased input impedance of these Darlington transistors along with the active load results in a larger open-loop amplifier gain. The active load comprises transistor $Tr_4$ and the associated components, while $Tr_7$ is an amplified Zener that provides
output stage bias. The input resistor $R_1$ both supplies bias current to the base of $Tr_1$ and establishes a near-zero potential at the input of the amplifier.

This enables direct coupling at the input of the circuit. Resistors $R_{11}$ and $R_{12}$ introduce negative feedback around the amplifier. Capacitor $C_1$ is for input coupling, while $C_2$ enables the minimization of DC offset. This will be discussed in the actual design to follow. Capacitor $C_3$ provides Miller compensation. It ensures that the amplifier has only one dominant pole and, therefore, is stable when feedback is applied. Its value can be determined analytically or experimentally. Capacitor $C_4$ along with $R_{13}$ ensures stable amplifier operation into inductive loads. Inductor $L_1$ and resistor $R_{14}$ enable stable operation into capacitive loads.

In analyzing this circuit, we need to determine the open-loop gain, i.e., the gain before feedback is applied. In order to do so, the feedback resistors must be disconnected. As we have discussed in Chap. 8, there are rules which govern how this should be done. However, in this circuit their effect is minimal.

### 9.7.1 Input Stage

The gain $A_{V1}$ of the first stage $Tr_1$ with collector current $I_{C1}$ is given by

$$A_{V1} = -\frac{h_{fe}R_{L1}}{2h_{ie}} \approx -\frac{R_{L1}}{2r_e} \quad (9.25)$$

where

$$r_e = \frac{1}{40I_{C1}} \quad (9.26)$$

In the circuit of Fig. 9.17, the load $R_{L1}$ is resistor $R_3$ in parallel with the input impedance $h_{ie}$ to transistor $Tr_3$. Thus, the voltage gain of the input stage of Fig. 9.17 is given by

$$A_{V1} = -\frac{R_3//h_{ie3}}{2r_e} \quad (9.27)$$
where

\[ h_{ie3} = \frac{h_{fe}}{40I_{C3}} \]  

(9.28)

### 9.7.2 Intermediate Stage

The second stage of the amplifier consists of transistor \( Tr_3 \) in a common-emitter amplifier configuration with an active load realized using \( Tr_4 \). This stage amplifies the output from the differential amplifier stage and provides most of the voltage gain of the overall amplifier. The gain of the stage is given by

\[ I_1 = I_{R1} = 0.7/R_1 \]  

(9.29)

where \( I_{C3} \) is the current in transistor \( Tr_3 \) and \( R_{L3} \) is the load made up of the active load in parallel with the input impedance of the complimentary Darlington pairs. Since the Darlington pairs are in the emitter follower configuration, the input impedance is \( h_{fe(D)} \) where \( h_{fe(D)} \) is the current gain of the Darlington pair. Since the impedance of the active load is high, it follows that \( R_{L3} \approx h_{fe(D)} \).

### 9.7.3 Output Stage

The output stage of the amplifier consists of a complimentary emitter follower whose gain is approximately one. It presents a low output impedance and provides the amplifier with the ability to deliver current to the speaker load without loading down the amplifier and reducing the open-loop gain. The use of the Darlington pair gives the stage a high current gain of approximately the product of the current gain of each of the two transistors. For typical transistor gains, this value can be of the order of 1000–10,000.

The overall voltage gain \( A_V \) of the open-loop amplifier is the product of the open-loop gain of the three stages and is given by

\[ A_V = 40I_{C3}R_{L3} \cdot \frac{R_2//h_{ie3}}{2r_e} \]  

(9.30)
The closed-loop amplifier shown in Fig. 9.17 involves voltage-series negative feedback being applied as in the non-inverting operational amplifier. For a finite open-loop gain $A_V$, the closed-loop gain $A_{Vf}$ is given by

$$A_{Vf} = \left(1 + \frac{R_{12}}{R_{11}}\right)\left(\frac{1}{1 + 1/A_V\beta}\right)$$  \hspace{1cm} (9.31)

where

$$\beta = \frac{R_{11}}{R_{11} + R_{12}}$$  \hspace{1cm} (9.32)

If $A_{Vf} \gg 1$, the closed-loop gain Eq. (9.31) reduces to

$$A_{Vf} = 1 + \frac{R_{12}}{R_{11}}$$  \hspace{1cm} (9.33)

This is the well-known expression for the voltage gain of a non-inverting operational amplifier circuit. It is, therefore, desirable to have a large open-loop gain so that Eq. (9.33) applies. Assuming large open-loop gain, the effect of capacitor $C'$ in the transfer function can be found from

$$A_{Vf} = \frac{1+sC_2(R_{11}+R_{12})}{1+sC_2R_{11}}$$

which means that the circuit has a low-frequency pole at

$$V_{oc} = -h_{fe}I_bR_L.$$  \hspace{1cm} (9.34)

### 9.7.4 Compensation Capacitor

It was shown in Chap. 7 that Miller capacitor compensation succeeds in realizing a dominant pole system. The closed-loop system has a gain of $A_{Vf}$ and the closed-loop graph intersects the open-loop plot at frequency $f_c$. In order to determine the value of this capacitor, we note that at $f_c$

$$A_V = A = A_{V1} \times A_{V2} \approx \frac{R_{L1}}{2r_e} \times A_{V2}$$  \hspace{1cm} (9.35)
At $f_c$, $R_{L1} \rightarrow X_{CM}$ where $X_{CM}$ is the reactance of the effective Miller capacitance at the input of $Tr_3$ and is given by $X_{CM} = 1/2\pi f_c A_{V2} C_3$. Hence

$$A_V = \frac{X_{CM}}{2r_e} \times A_{V2} = g_M \times \frac{1}{2\pi f_c A_{V2} C_3} \times A_{V2} = \frac{g_M}{2\pi f_c C_3}$$

(9.36)

where $g_M = 1/2r_e$ is the transconductance of the input stage. From this, the value of capacitor $C_3$ is given by

$$C_3 = \frac{g_M}{2\pi f_c A_V}$$

(9.37)

**Example 9.10**  Design a power amplifier that delivers 100 W average power into an 8 $\Omega$ load using the configuration in Fig. 9.17.

**Solution**  In order to produce 100 W into 8 $\Omega$, the peak output voltage $V_{opk}$ is given by

$$\left(\frac{V_{opk}}{\sqrt{2}}\right)^2 = 100$$

where $R_{spk} = 8$ $\Omega$. This gives $V_{opk} = 40$ V.

The corresponding peak output current is $40/8 = 5$ A. Resistors $R_9$ and $R_{10}$ provide output stage quiescent current stability. However, since they are in the output current path there will be voltage losses across them, therefore, they cannot be too large. If we allow a voltage drop of 1 V peak, then $R_9$ and $R_{10}$ should be $1/5 = 0.2$ $\Omega$. On the positive half-cycle, this current flows through resistor $R_9$ resulting in a 1 V drop across $R_9$. This and the base-emitter voltages of Darlington $Tr_5$ sum to $40 + 1 + 1.4 = 42.4$ V. If we allow about 5 V across the active load in order that it is fully operational, then the positive supply voltage needs to be about 50 V. On the negative half-cycle, resistor $R_{10}$ and the base-emitter voltages of Darlington $Tr_6$ again sum to about 42.4 V. For symmetry, we choose a negative supply voltage of −50 V. This allows at least 7 V across $Tr_3$ during its operation. For good transistor operation, let the quiescent current in each transistor of the differential pair be 1 mA. The total current through $R_2$ is, therefore, 2 mA. This current is provided by the Zener diode $D_1$ which is selected to be about half of the
supply voltage. A Zener with voltage of 24 V is available. The base of \( Tr_1 \) is at an approximately zero potential, and hence \( R_2 \) is given by \( R_2 = (24-0.7)/2 \text{ mA} = 11.7 \text{ k}\Omega \). Resistor \( R_4 \) supplies current to the Zener of about 5 mA as well as the 2 mA to the differential pair. Hence \( R_4 = (50-24)/7 \text{ mA} = 3.7 \text{ k}\Omega \). The base-emitter voltage of \( Tr_3 \) appears across \( R_3 \) and, therefore, \( R_3 = 0.7/1 \text{ mA} = 700 \text{ \Omega} \). Resistor \( R_1 \) supplies base current to \( Tr_1 \). It should be low in order to minimize the voltage drop arising from the base current flow while high enough to provide a high input impedance to the circuit. A value of about 10 k or higher is a reasonable compromise. For a peak output voltage of 40 V, the peak output current is 40/8 = 5 A. Using Darlington current gain of 1000, the maximum peak base current of each Darlington is 5/1000 = 5 mA. Since this current is sourced from the collector current of \( Tr_3 \), we, therefore, choose a quiescent current of 10 mA for this transistor. The collector current of \( Tr_4 \) must also be set at 10 mA. This is accomplished by noting that the voltage across diode \( D_2 \) is dropped across \( R_5 \) through which the 10 mA also flows giving \( R_5 = 0.7/10 \text{ mA} = 70 \text{ \Omega} \). Resistor \( R_6 \) is chosen such that about 5 mA flows through diodes \( D_2 \) and \( D_3 \) to turn them fully on. Hence \( R_6 = (50-1.4)/5 \text{ mA} = 9.7 \text{ k}\Omega \). In order to minimize DC offset at the output, feedback resistor \( R_{12} \) is chosen to be the same value 10 k as the input resistor \( R_1 \). Resistor \( R_{11} \) then sets the closed-loop gain. A value of 520 \text{ \Omega} \) gives a closed-loop gain of 20. For the \( V_{BE} \) multiplier, the current in this stage is the 10 mA collector current of \( Tr_3 \). Because of the base-emitter voltage of \( Tr_7 \) across \( R_7 \), a value of 1 k results in a current through this resistor of 0.7/1 k = 0.7 mA. This is approximately seven times larger than the base current of \( Tr_7 \) which is 10 mA/100 = 0.1 mA. If we set \( R_8 = 1 \text{ k}\Omega \), then a 5 k potentiometer for \( VR_1 \) will produce a maximum voltage across \( Tr_7 \) of 0.7 mA \times (1 \text{ k} + 1 \text{ k} + 5 \text{ k}) = 4.9 V. This is more than the 2.8 V required to turn on the Darlington pairs. The minimum voltage across \( Tr_7 \) (corresponding to \( VR_1 = 0 \)) is 0.7 mA \times (3.3 \text{ k}) = 2.3 V. Therefore, the potentiometer can be used to set the bias current in the output stage to a value that minimizes crossover distortion. This value is likely to lie in the range 10–100 mA. The
capacitor $C_2$ influences the low-frequency performance of the amplifier. A value of 100 $\mu$F sets a pole at $f_p = 1/(2\pi100 \times 10^{-6} \times 520) = 3$ Hz.

The capacitor $C_1$ also influences low-frequency roll-off. Using the input resistance as 10 k (since feedback will increase the input impedance into $Tr_1$), a value of 10 $\mu$F for this capacitor will result in a pole at $f_p = 1/2\pi10 \times 10^{-6} \times 10,000 = 1.59$ Hz. Capacitor $C_3$ is determined using Eq. (9.37). The choice of frequency $f_c$ is critical. It must be chosen high enough such that adequate feedback is available at all frequencies of interest. However, setting this frequency too high will increase the risk of instability arising from increased phase shift around the feedback loop. For audio amplifiers, $f_c$ is likely to be in the range 200 kHz to 2 MHz using $f_c = 500$ kHz and $g_m = 1/2r_e = 1/50$, where $r_e = 1/40I_C$, we get $C_3 = \frac{1}{50} \times \frac{1}{2\pi5 \times 10^5 \times 20} = 318$ pF. The final value of $C_3$ can be experimentally determined by adjusting for minimum square wave overshoot.

Suggested transistors are as follows: Power Darlington MJ11021/MJ11022 (250 V, 15 A, 175 W); $Tr_3/Tr_4$ MJE340/MJE350 (300 V, 500 mA, 20 W); $Tr_1/Tr_2$ 2N5400 pnp (140 V, 600 mA, 625 mW).

This amplifier can be improved in several ways. The first improvement is to replace the resistor $R_2$ supplying current to the differential pair by a constant current source as shown in Fig. 9.18. The effect of this is to improve the ripple rejection capability of the amplifier so that power supply changes do not get into the amplifier via the emitters of $Tr_1$ and $Tr_2$. A second improvement is the inclusion of small resistors $R_e$ in the emitters of $Tr_1$ and $Tr_2$. These resistors reduce the distortion produced in this stage, increase the bandwidth, and improve the current equalization between the transistor pair. If this is done, the compensation capacitor can be reduced, and hence the amplifier slew rate increases. Note that $g_m$ becomes $g_m = 1/2(r_e + R_e)$. A third significant improvement is the utilization of a Cascode amplifier in place of $Tr_3$ as shown in Fig. 9.19. This reduces distortion arising from modulation of the collector-base junction capacitor of $Tr_3$ as a result of the large voltage swing occurring in the output stage. Finally,
the Darlington pairs in the output stage may be assembled using discrete transistors or may be replaced by power MOSFETS which have extremely high input impedance. A fully symmetrical design using these latter devices is the subject of the next section.

*Fig. 9.18* Introduction of constant current source
**Example 9.11** The amplifier circuit shown in Fig. 9.20 uses feedback pairs in the output stage and can deliver 60 W into 8 Ω. Analyze the circuit to determine the quiescent currents in the input and intermediate stages as well as the closed-loop gain. Investigate the purpose of the 100 μF capacitor connected between the output and the junction of the two 2.7 k resistors.
Solution  The voltage at the emitters of the input transistors is approximately +0.7 V. Noting that the other end of the 6.8 k resistor supplying current to these transistors is supplied by a 15 V Zener diode regulator, the current through the 6.8 k resistor is (15–0.7)/6.8 k = 2.1 mA. This is the total current flowing into the emitters of the two input transistors. The first of these transistors has a 680 Ω resistor in its collector circuit. This in turn is connected across the base-emitter junction of the intermediate stage. Hence the current through this resistor is 0.7/680 = 1 mA. Therefore, the current in $Tr_2$ is 2.1–1 = 1.1 mA. The current through $R_3$ is (35–15)/2.2 k = 9 mA. The current through the second stage transistor is (35–0.7)/(2.7 + 2.7) k = 6.4 mA. Finally, the closed-loop gain is 1 + 20 k/1 k = 21. The 100 μF capacitor
is used to bootstrap resistor $R_6$, thereby producing a quasi-constant current source. This makes more drive current available to drive the base of the feedback pair for positive output swing.

### 9.8 High-Power MOSFET Amplifier

A high-quality power amplifier may be designed using power MOSFETs instead of power transistors in the output stage. Power MOSFETs became available in the 1970s and enable the exploitation of the high input impedance of the field effect transistor while being able to handle significant power levels. They can be used to replace the Darlington Pairs in Fig. 9.17 in the output stage. These devices respond to very high frequencies and are more easily biased. Another advantage of these devices is their extremely high input impedance completely isolates the second stage transistor collector from the effects of the amplifier load. A completely symmetrical amplifier design using power MOSFETs is shown in Fig. 9.21. Note that four MOSFETs are used, two n-channel and two p-channel devices each pair sharing the load current on alternatively positive and negative signal cycles. Along with power, MOSFETs at the output, this circuit uses a complimentary symmetry differential amplifier at the input and complimentary Cascode intermediate voltage gain stages. The result is a fully symmetrical and very linear circuit that produces low levels of harmonic distortion. The dominant pole is set by the capacitance at the gate-drain junctions of the MOSFETs with all other poles at high frequencies.
Example 9.12  Design a power amplifier that delivers 150 W average power into an 8 \( \Omega \) load using the configuration in Fig. 9.21.

Solution  In order to produce 150 W into 8 \( \Omega \), the peak output voltage \( V_{opk} \) is given by

\[
\frac{V_{opk}}{\sqrt{2}} = 100
\]

where \( R_{spk} = 8 \Omega \). This gives \( V_{opk} = 49 \) V.

The corresponding peak output current is \( 49/8 = 6.13 \) A. Resistors \( R_{20} \) to \( R_{23} \) provide output stage quiescent current stability. As before, since they are in the output current path they cannot be large. Values of 0.22 \( \Omega \) will be used and, because the current is approximately shared, will result in a peak voltage drop of less than 1 V. On the peak positive half-cycle with maximum current flowing into the load, the voltage drop in \( R_{20} \) (or \( R_{21} \)) added to the gate-source FET voltage of 2 V gives the voltage at the collector of \( Tr_7 \) as \( 49 + 1 + 2 = 52 \) V. If we allow about 5 V
across the active load in order that it is fully operational, then the positive supply voltage needs to be about +60 V. Similarly, we choose a negative supply voltage of −60 V. The FET gate resistors $R_{16}$–$R_{19}$ are necessary for MOSFET stability and each needs to be about 220 Ω. Diodes $D_5$, $D_7$, $D_6$, and $D_8$ protect the gate source junctions from over-voltage with Zeners $D_5$ and $D_6$ limiting the voltage to 12 V.

Potentiometer $V_{R_1}$ is adjusted in order to set the FET bias current. Note that a $V_{be}$ multiplier is not necessary. Suitable power MOSFETs are 2SK1058/2SJ162 (160 V, 7 A, 100 W).

At the input, the complimentary symmetry differential amplifier has a reduced current flowing in the bias resistor $R_1$ since $Tr_1$ and $Tr_3$ approximately provide each other with the necessary base current. This resistor can, therefore, assume a higher value while still keeping the transistor bases at an approximately zero potential. Suitable transistors are 2N5551/2N5401 (160 V, 600 mA). We let $R_1 = R_{25}$ for minimum DC offset and set the value at 33 k. Hence with $R_{24} = 1$ k, the overall closed-loop gain is 34. This gives a sensitivity of about 1 V rms for full output into 8 Ω. The input transistors all have emitter degeneration resistors $R_2$ to $R_5$. These resistors balance the current in $Tr_1$–$Tr_2$ and $Tr_3$–$Tr_4$, improve the frequency response and reduce distortion. However, the gain of this stage is reduced. Values of 100 Ω represent a reasonable compromise. Diodes $D_1$ and $D_2$ provide regulated supplies for the currents into $Tr_1$–$Tr_2$ and $Tr_3$–$Tr_4$. If we set the currents in these transistors to be 0.5 mA, then using diodes $D_1$ and $D_2$ at 24 V, it follows that $R_9 = R_{10} = (24–0.7)/1$ mA = 23.3 k. $R_8$ and $R_{11}$ supply current to the Zener diodes. This current needs to be about 5 mA. Hence $R_8 = R_{11} = (60–24)/(5 + 1) = 6$ k. The cascode amplifiers $Tr_5$–$Tr_6$ and $Tr_8$–$Tr_7$ using MJE340/MJE350 high-voltage transistors for $Tr_6$ and $Tr_7$ must operate with enough current to charge the input (gate-drain) capacitance of the MOSFETS which varies with drain-source voltage. Using gate capacitance of 500 pF and a current of 15 mA, the slew rate will be $SR = \frac{2 \times 15 \text{ mA}}{500 \text{ pF}} = 60 \text{ V/μs}$. This is sufficient to avoid slewing distortion for peak output signals at 20 kHz which is $SR = 2\pi \times 49 \times 20$, 


Resistors $R_{12}$ and $R_{15}$ introduce local feedback in the cascode amplifiers, thereby improving linearity. A value for these resistors of 82 $\Omega$ results in a voltage drop across it of $15 \text{ mA} \times 82 = 1.23 \text{ V}$. Therefore, the voltage between the base of $Tr_5$ and the negative supply rail is $1.23 + 0.7 = 1.93 \text{ V}$. This is the voltage across resistor $R_7$ which, because it is carrying the $Tr_3$ collector current of 0.5 $\text{ mA}$, must be $R_7 = 1.93/0.5 \text{ mA} = 3.8 \text{ k}$. Resistor $R_6$ is calculated in a similar manner to give the same value. Diodes $D_3$ and $D_4$ set the voltage at the bases of $Tr_6$ and $Tr_7$. Their values are chosen to be 3.9 $\text{ V}$ in order to allow sufficient voltage across the cascode arrangement. Current for these diodes is delivered by resistors $R_{14}$ and $R_{13}$ which are given by $R_{13} = R_{14} = (60 - 3.9)/5 \text{ mA} = 11.2 \text{ k}$ where 5 $\text{ mA}$ is the value of this current. Capacitor $C_1$ is an input coupling capacitor whose value is set to ensure an adequate low-frequency response. Since the input impedance of the circuit is approximately $R_1 = 33 \text{ k}$, for a low-frequency cutoff of 20 Hz, $C_1 = 1/2\pi \times 20 \times 33,000 = 0.24 \mu\text{F}$. We chose a value of 1 $\mu\text{F}$. Capacitors $C_5$ and $C_6$ are filter capacitors chosen to reduce the ripple at the Zener diodes. A value of 10 $\mu\text{F}$ will give sufficiently low impedance at ripple frequency of 120 Hz from a bridge rectifier. Capacitors $C_7$ and $C_8$ perform a similar function and need to be about 100 $\mu\text{F}$. Capacitors $C_2$ and $C_3$ are connected as a non-polarized capacitor and minimize the dc offset at the output of the amplifier. This capacitor along with $R_{24}$ also influences the low-frequency cutoff frequency and is given by $C_T = 1/2\pi \times 20 \times 1000 = 8 \mu\text{F}$. A value of 100 $\mu\text{F}$ is chosen and, therefore, $C_2 = C_3 = 200 \mu\text{F}$.

9.9 IC Power Amplifiers

The power amplifiers discussed thus far all employ discrete components. An alternative approach to power amplification is the use of power ICs. These are specifically designed to deliver high voltages and currents, unlike low-power operational amplifier ICs. A few devices selected from the large number available are presented.
9.9.1 Low-Power IC Amplifier: LM386

The first example of a power amplifier IC is the LM386 from National Semiconductor shown in a typical application in Fig. 9.22. This device has been optimized such that it requires a minimum number of supplementary components and can deliver up to 1 W average power into an 8 Ω load. It operates from a single-ended power supply that can vary from 4 to 12 V. It can, therefore, be powered from three 1.5 V batteries, the 5 V supply from a computer, a 9 V battery, or a 12 V car battery. Internal circuitry provides bias for the IC such that the output terminal is at half of the supply voltage, thereby allowing for maximum symmetrical swing. The output terminal must, therefore, be coupled to the load through a capacitor $C$ resulting in a low-frequency cutoff frequency given by $f_L = 1/2\pi R_{load}C$. Even though the IC operates from a single-ended supply, the inputs are referenced to the ground. Direct coupling at the input is, therefore, possible. Overall negative feedback is applied within the package. The input signal is applied to the non-inverting input with the inverting input connected to the ground. The gain is 20 but can be adjusted using IC pins. The 10 kΩ potentiometer limits the input signal amplitude to the maximum rated value of ±0.4 V.

With a 9–12 V supply, the IC can deliver a 6 V peak-peak output which corresponds to about 0.5 W rms into 8 Ω.

Fig. 9.22 LM386 power amplifier
In order to increase the output power, two LM386 ICs can be operated in a bridge configuration shown in Fig. 9.23. Here, one IC is connected in the non-inverting configuration (signal applied to the non-inverting input with inverting input grounded), while the other is connected in the inverting configuration (signal applied to the inverting input with non-inverting input grounded). The load is connected across the IC outputs which are out of phase. Thus, while the output of one IC swings positive toward the supply voltage, the output of the other swings negative toward the ground.

![Bridge configuration](image)

**Fig. 9.23** Bridge configuration

### 9.9.2 USB-Powered Amplifier: LM4871

The LM4871 uses the bridge configuration in Fig. 9.23 in its internal structure to deliver 3 W into a 3 Ω load from a 5 V supply such as is available from a computer USB port. It requires few external components not including output coupling capacitor. It possesses thermal shutdown protection and is unity gain stable. The amplifier gain can be set externally and is intended primarily for the use in portable devices. Figure 9.24 shows it in a typical application.
Fig. 9.24  Power amplifier using the LM4871

9.9.3 Medium-Power IC Amplifier : LM3886
For higher output power levels than can be delivered by the LM386, the LM3886 shown in Fig. 9.25 is available. This is a high performance audio power amplifier that can deliver 56 W continuous power into an 8 Ω load with low harmonic distortion between 20 Hz and 20 kHz. It operates from ±10 to ±42 V and can supply up to 4 A. The device is fully protected against overtemperature, overcurrent, and voltage transients. It operates essentially as a power op-amp, and therefore, the gain is given by \( A_{Vf} = 1 + \frac{R_2}{R_1} \). The peak output voltage is about 5 V less than the supply voltage.
**Example 9.13** Configure the LM3886 to produce 50 W into 8 Ω with reasonable sensitivity.

**Solution** For 50 W into 8 Ω, the peak output voltage is given

\[ V_{opk} = \sqrt{50 \times 2 \times 8} = 28.3 \text{ V} \]

The peak output current is then

\[ I_{opk} = \frac{28.3}{8} = 3.54 \text{ A} \]

Therefore, the required supply voltage is given by \( \pm V_{CC} = 28.3 + 5 = \pm 33.3 \text{ V} \), where 5 V is the dropout from the IC. If the device is powered from an unregulated supply, then adequate allowance must be introduced such that the minimum supply voltage is 33.3 V. In order to produce the full output from an input of say 1 V, the amplifier gain must be

\[ \frac{28.3}{\sqrt{2}} = 20 \]

Therefore,

\[ 20 = 1 + \frac{R_f}{R_i} \]

If \( R_1 = 1 \text{ k} \) then \( R_2 = 19 \text{ k} \). Note that with readily available \( \pm 15 \text{ V} \) supplies, this IC can deliver 10 W into an 8 Ω load.
9.9.4 **High-Power IC Amplifier Driver: LME49811**

The LME49811 is a power IC driver from Texas Instruments that, working in conjunction with power output transistors, is able to deliver up to 500 W output into an 8 Ω load at extremely low levels of harmonic distortion. The basic system is shown in Fig. 9.26. It operates from ±20 V to ±100 V with the power output increasing with the supply voltage. The IC is used to deliver drive current (source and sink) to complimentary Darlington pairs $Tr_1$ and $Tr_2$ such as the MJ11021 and MJ11022 (250 V, 15 A, 175 W). Transistor $Tr_3$ is a $V_{BE}$ multiplier that sets the bias current in $Tr_1$ and $Tr_2$. The resistors $R_f$ and $R_i$ set the closed-loop gain at $A_V = 1 + R_f/R_i$. For stability, $A_{Vf}$ must be greater than about 20. The capacitor $C_C$ provides compensation and must be optimized experimentally. The IC driver has a shutdown mode and is thermally protected. Power supply decoupling of the IC using $C_3$ and $C_4$ is essential.
Example 9.14 Configure the LME49811 IC to produce 200 W into 8 Ω with a gain of 21.

Solution In order to produce 200 W into 8 Ω, the peak output voltage is given by \( V_{Opk} = \sqrt{2 \times 8 \times 200} = 56.6 \) V. The peak output current is then \( I_{Opk} = \frac{56.6}{8} = 7.1 \) A. The specifications for the LME49811 indicate that in order to deliver an output voltage of \( \pm 56.6 \) V, the supply voltage must be \( \pm 80 \) V. The components of the \( V_{BE} \) multiplier are determined as done previously. For a gain of 21, \( R_i \) is set to 1 k and hence \( R_f \) is set to 20 k. Resistor \( R_1 \) is also set at 20 k. From the datasheet, the shutdown
resistor \( R_M \) is calculated using \( R_M = (V_{\text{ref}} - 2.9)/I_{SD} \). With \( V_{\text{ref}} = 6.8 \) V and \( I_{SD} = 1.5 \) mA, \( R_M = 2.6 \) k. Capacitors, \( C_1 \) and \( C_2 \), are selected to be 10 \( \mu \)F for an adequate low-frequency response. The compensation capacitor \( C_c \) is set at a nominal value of 30 pF with the final value determined experimentally. The power supply pins to the IC must be decoupled with \( C_3 = C_4 = 0.1 \) \( \mu \)F capacitors. In order to deliver this level of power to the speaker, the Darlington output stage needs to comprise a parallel arrangement of four sets of complimentary Darlington pairs MJ11021/MJ11022 as shown in Fig. 9.27. Each pair will deliver a portion of the output load current with all four pairs being driven by the LME49811. Adequate heatsinking of these transistors, as well as the LME49811, is necessary for the successful operation of this high-power system.

![Fig. 9.27 Parallel combination of complimentary Darlington pairs](image)

**9.10 Amplifier Accessories**

A power amplifier is often used to drive inductive and capacitive loads such as loudspeakers and significant lengths of the connecting cable. If the amplifier is to remain stable under such conditions, appropriate networks need to be connected at the output of the power amplifier.
The two networks normally used are a shunt Zobel network for maintaining stability into inductive loads and a parallel-connected inductor and resistor in series with the output for preserving stability when driving capacitive loads.

A capacitive load connected to the output of a power amplifier can result in the amplifier going unstable. This occurs since the output resistance of the amplifier in conjunction with the capacitor form what is effectively a low-pass filter at the output of the amplifier. This network introduces a pole into the transfer function of the amplifier which causes phase shift that pushes the closed-loop system toward instability. In order to prevent this, an inductor is placed between the amplifier output and the capacitive load such that the capacitance is isolated from the amplifier. Its value is chosen such that the upper cutoff frequency created by the inductor working in conjunction with the lowest load resistance presented by the speaker load is above the highest frequency to be amplified. Additionally, a small resistor is placed in parallel with this inductor in order to provide damping. This network is referred to as a Thiele network. Typical values are 2 μH in parallel with a 1 Ω resistor of suitable wattage (See $L_1$ and $R_27$ in Fig. 9.21).

The voice coil of a loudspeaker presents an inductive load to a power amplifier that can excite instability at high frequencies as the inductive reactance increases. This problem can be resolved by placing a Zobel network across the speaker. This network comprises a resistor in series with a capacitor, and its effect is to cause the inductive speaker load to appear resistive across the frequency of operation of the amplifier. The resistor is usually in the range 4.7–10 Ω, while the capacitor is almost always 0.1 μF (See $R_{26}$ and $C_4$ in Fig. 9.21).

It may be necessary to provide protection for the output transistors in a power amplifier. This is to prevent transistor burnout due to current overload. A simple mechanism to achieve this is the circuit shown in Fig. 9.28. This is incorporated in the output stage of the amplifier. A large current flow through resistors $R_E$ produces a voltage drop that turns on transistors $Tr_a$ and $Tr_b$. These in turn reduce the drive current to the base of the output transistors and as a result limit the current in these devices.
9.10.1 **Heatsink Design**

In the class B amplifier, almost 25% of the input power from the power supply is converted into heat, most of which is dissipated in the output stage. As a result, during operation power amplifiers dissipate a large amount of heat in the power transistors. A characteristic of transistors is that as the temperature is increased, their power-handling capability
decreases. A graphical illustration of this is presented in Fig. 9.29. Here, the curve ABCD defines the safe operating area of the transistor. Portion AB represents the maximum current that the transistor can handle, portion CD is set by the maximum collector-emitter voltage of the transistor and portion BC is the hyperbola defined by $V_{CE} = P_D$ where $P_D$ is the transistor power rating at room temperature (25°C).

As the temperature of the case of the transistor and hence the collector junction temperature increases, the power rating of the transistor decreases. The result is that the hyperbola represented by curve BC moves toward the axes as shown, thereby decreasing the safe operating area of the transistor. The transistor is then said to be derated. A curve showing the transistor derating as a function of case temperature is shown in Fig. 9.30. In order to prevent this transistor derating, the dissipated heat must be conducted away such that the transistor junction temperature is kept low. To aid in heat conduction
away from the transistor, the device must be mounted on a piece of metal called a heatsink. This along with the metal case of the transistor provides a large surface area from which the heat can be radiated. This results in a lower transistor junction temperature as compared with the transistor operating without the heatsink. The heat path is from the transistor junction to the case, from the case to the heatsink and finally from the heatsink to the surrounding atmosphere.

![Typical derating curve for silicon power transistors](image)

**Fig. 9.30** Typical derating curve for silicon power transistors

Information regarding transistor derating is contained in the equation

\[
P_D(T) = P_D(T_o) - (T - T_o) \cdot DF
\]

where \(P_D(T)\) is the maximum power dissipation at temperature \(T\), \(T_o\) is the temperature above which derating begins with \(P_D(T_o)\) the maximum power dissipation rating of the transistor and \(DF\)
(Watts/degree of temperature) is the derating factor given in manufacturer specification sheet.

Example 9.15  Determine the maximum allowable dissipation at 100°C in a power transistor rated at 125 W at 25°C if derating occurs above this temperature by a derating factor of 0.5 W/°C.

Solution  Using Eq. (10.35), the maximum power dissipation for the transistor at 100°C is

\[ P_D(100\degree) = P_D(25\degree) - (100\degree - 25\degree) (0.5 W/\degree) = 125 W - 75\degree (0.5 W/\degree) = 87.5 W. \]

This means that at 100°C this 125 W power transistor can only dissipate 87.5 W.

In order to determine the heatsink required for a particular application, it is necessary to consider the thermal conditions associated with the transistor heatsink combination. In particular, the junction temperature for a heatsink mounted transistor is given by

\[ T_J = T_A + P_D (\theta_{JC} + \theta_{CS} + \theta_{SA}) \]  \hspace{1cm} (9.39)

where \( P_D \) is the power to be dissipated, \( T_J \) is the transistor junction temperature, \( T_A \) is the ambient temperature in the immediate vicinity of the transistor, \( \theta_{JC} \) (°C/W) is the transistor thermal resistance between junction and case, \( \theta_{CS} \) is the insulator thermal resistance between case and heatsink and \( \theta_{SA} \) is the heatsink thermal resistance between heatsink and atmosphere. \( \theta_{JC} \) is set by the transistor manufacturer, while \( \theta_{CS} \) is determined by the transistor mounting arrangements. If a good thermal compound is used between the transistor case and the heatsink, \( \theta_{CS} \approx 0.2\degree /W \). It is, however, often necessary to isolate the transistor case from the heatsink by introducing a mica wafer between them. This electrically isolates the transistor but raises the thermal resistance to typically \( \theta_{CS} \approx 2\degree /W \). The last parameter \( \theta_{SA} \) is the main heatsink specification and is determined using Eq. (9.39).

Example 9.16  In a power amplifier design, a power transistor is expected to dissipate 50 W. Using the transistor in the previous
example, determine the thermal resistance of the heatsink required for safe operation of this transistor. Use \( \theta_{JC} = 0.4^\circ\text{C/W} \) and \( \theta_{CS} \approx 2^\circ\text{C/W} \).

**Solution**  From the previous example, the transistor was able to dissipate 87.5 W at a junction temperature of 100°C. Thus, at this temperature, the transistor can safely dissipate 50 W. From Eq. (10.37), \( \theta_{SA} = (T_J - T_A)/P_D - \theta_{JC} - \theta_{CS} = (100-25)/50-0.4 - 0.2 = 0.9^\circ\text{C/W} \).

### 9.11 Applications

A variety of power amplifiers and associated systems are presented below.

**9.11.1 1.5 W Low-Power Amplifier**

The circuit shown in Fig. 9.31 is an improved non-inverting version of the low-power amplifier with bootstrapping in Fig. 9.13a and is similar to the configuration in Fig. 9.16 (improved medium power). An additional common-emitter amplifying stage \( \text{Tr}_4 \) is introduced in the circuit. This stage provides further gain and allows the application of voltage-series feedback at the emitter of \( \text{Tr}_4 \). The resistors \( R_1 \) and \( R_2 \) provide a fixed voltage for the base of \( \text{Tr}_4 \) and resistor \( R_8 \) and capacitor \( C_5 \) provide filtering. This configuration requires a compensation capacitor \( C_4 \) whose value is given by \( C_4 = \frac{8m}{2\pi f_c A_{Vf}} \) where

\[
g_m = \frac{1}{(r_e[\text{Tr}_4] + R_9)} \text{ and } A_{Vf} \text{ is the closed-loop gain of the amplifier.}
\]
For maximum symmetrical output, the quiescent voltage at the output of the power amplifier is $V_{CC}/2$. For $P = 1.5 \text{ W}$ into $8 \Omega$, using $V_{pk} = \sqrt{2PR_L}$, $V_{pk} = \sqrt{2 \times 1.5 \times 8} = 4.9 \text{ V}$. In order to allow for
transistor saturation losses, the peak voltage swing is set at 6 V, and therefore, \( V_{CC} = 2 \times 6 = 12 \text{ V} \). The peak output current is given by \( I_{pk} = 4.9/8 = 0.6 \text{ A} \). Using a current gain of 100 for each output transistor, the maximum output current results in maximum base currents for each given by \( I_b(Tr_{2,3}) = 0.6 \text{ A}/100 = 6 \text{ mA} \). This current flows into the collector of \( Tr_1 \) during negative-going half-cycles or is supplied by the bootstrapped resistor \( R_4 \) during positive-going half-cycles. In order to ensure that this current is always available, the collector current of \( Tr_1 \) is set at 12 mA which is twice the requirement for the base current to the output transistors. This gives \( R_4 + R_5 = 6 \text{ V}/12 \text{ mA} = 500 \text{ } \Omega \). We use \( R_4 = R_5 = 220 \text{ } \Omega \). Resistors \( R_6 \) and \( R_7 \) are chosen to maximize bias current stability in the output stage, while minimizing power dissipation from signal current. Since only moderate output currents are involved, the power dissipation is the less serious issue, and therefore, these resistors can be selected for bias stability. A value of about 1 Ω for each of these resistors is reasonable. Taking the current gain of \( Tr_1 \) to be 100, the base current \( I_b(Tr_1) = 12 \text{ mA}/100 = 120 \text{ μA} \). Since this current is supplied by \( Tr_4 \), the quiescent current in this transistor is set at say 0.5 mA. Hence \( R_3 = 0.7/0.5 \text{ mA} = 1.4 \text{ k} \). For a 20 Hz low-frequency response into the 8 Ω load, \( C_2 \) is given by \( C_2 = 1/2\pi \times 20 \times 8 = 995 \text{ μF} \). A value of 1000 μF is, therefore, chosen. The \( V_{BE} \) multiplier must provide at least \( 2V_{BE} = 1.4 \text{ V} \) drops across the base-emitter junctions of \( Tr_2 \) and \( Tr_3 \). Let \( I_{Ra} = 1 \text{ mA} \). Then \( R_a(Tr_3) = 0.7 \text{ V}/1 \text{ mA} = 700 \text{ } \Omega \). Hence \( 1 + \frac{R_b}{R_a} = \frac{1.4}{0.7} = 2. \)

\[
\frac{R_b}{R_a} = 1, R_b = 700 \text{ Ω} \]. A 2 k potentiometer can be used for \( R_b \) to allow adjustment of the quiescent current in the output stage. Resistor \( R_{10} \) along with resistor \( R_9 \) provides feedback to the emitter of the input transistor \( Tr_4 \). Let \( R_{10} = 2.7 \text{ k} \) say. Then the voltage at the emitter of \( Tr_4 \) is \( V_E(Tr_4) = 6–0.5 \text{ mA} (2.7 \text{ k}) = 4.7 \text{ V} \). This sets the voltage at the base of \( Tr_6 \) at \( V_B(Tr_4) = 4.7–0.7 = 4 \text{ V} \). Using a current \( I_R = 0.05 \text{ mA} \) through resistors \( R_8 – R_1 – R_2 \) which is one tenth of the collector current of \( Tr_4 \)
to ensure bias voltage stability for $Tr_4$, then $R_8 + R_1 + R_2 = 12 \text{ V}/0.05 \text{ mA} = 240 \text{ k}$ and $R_2 = 4/0.05 \text{ mA} = 80 \text{ k}$. Choosing $R_1 = 80 \text{ k}$ then $R_8 = 240 \text{ k} - 80 \text{ k} - 80 \text{ k} = 80 \text{ k}$. The input impedance of the amplifier is less than $R_1//R_2$ which is $80 \text{ k}//80 \text{ k} = 40 \text{ k}$. Therefore, the value of the input capacitor $C_1$ can be found using $C_1 = 1/2\pi \times 20 \times 40 \text{ k} = 0.2 \text{ \mu F}$. A value of 1 \mu F is then chosen since the input impedance at the base of $Tr_4$ while high because of voltage-series feedback introduced by $R_{10}$ and $R_9$ reduces the overall input impedance below 40 k. The gain of the amplifier is given by $1 + R_{10}/R_9$. Since $R_{10} = 2.7 \text{ k}$ then for a gain of 25, $R_9 = 112 \text{ \Omega}$. A filter capacitor $C_6$ of about 100 \mu F can be used to reduce the effect of long power supply leads, while $C_5 = 100 \text{ \mu F}$ forms a low-pass filter with $R_8$ to remove ripples from the supply going to the base of $Tr_4$. For an adequate low frequency response, capacitor $C_3$ must be chosen such that its reactance is equal to $R_9$ at 20 Hz. Thus $C_3 = 1/2 \times \pi \times 20 \times 112 = 71 \text{ \mu F}$. Choose $C_3 = 100 \text{ \mu F}$. Capacitor $C_4$ introduces Miller compensation for circuit stability and is determined using Eq. (9.37). For $Tr_4$, $I_C = 0.5 \text{ mA}$, and hence $r_e(Tr_4) = 1/40I_C = 50 \text{ \Omega}$. Therefore, using $f_c = 500 \text{ kHz}$, $A_{Vf} = 25$ and $g_m = 1/(r_e[Tr_4] + R_9) = 1/(50 + 112) = 1/162$ in Eq. (9.37), the value for capacitor $C_4$ is given by $C_4 = \frac{g_m}{2\pi f_c A_{Vf}} = \frac{1}{162 \times 2\pi \times 5 \times 10^{-5} \times 25} = 79 \text{ \text{ pF}}$.

Finally, bootstrapping capacitor $C_7$ must have a reactance at 20 Hz that is lower than the resistance of $R_4$. Hence $C_7 = 1/2 \times \pi \times 20 \times 220 = 36 \text{ \mu F}$. Choose $C_7 = 100 \text{ \mu F}$.

_Ideas for Exploration_: (i) Redesign the input stage of this circuit, using a differential amplifier to replace $Tr_4$; (ii) Employ a cascode amplifier in place of $Tr_1$.

### 9.11.2 50 W MOSFET Amplifier Using Bootstrapping

This circuit is that of a 50 W MOSFET amplifier using a differential input stage and a bootstrapped driver stage (Fig. 9.32). Each transistor in the differential pair has about 1 mA. For $P = 50 \text{ W}$ into 8 \Omega, using
In order to allow for transistor saturation losses, the supply is set at 35 V and, therefore, \( \pm V_{CC} = \pm 35 \) V. The MOSFETs being used are the IRF530 and the IRF9530 which together have input capacitance of 150 pF. The driver stage \( Tr_3 \) must have adequate current to drive the input capacitances of the MOSFETs. Using a current of 6 mA, the slew rate is \( SR = \frac{6 \text{ mA}}{150 \text{ pF}} = 40 \text{ V/\mu s} \) which will prevent slew rate limiting on audio signals. Let \( R_5 = R_6 \). Then \( R_5 + R_6 = 35 \text{ V/6 mA} = 5.8 \) k giving \( R_5 = R_6 = 2.9 \) k. For a current of 1 mA in \( Tr_1, R_2 = 0.7/1 \text{ mA} = 700 \) \( \Omega \). With 1 mA through \( Tr_2 \) also, then \( R_4 + R_3 = 35/2 \text{ mA} = 17.5 \) k. Let \( R_4 = 2.5 \) k then \( R_3 = 15 \) k. Let \( R_1 = R_8 = 47 \) k. Setting these resistors equal minimizes DC offset at the output of the amplifier. For a gain of 20, \( R_7 = 2.1 \) k. The capacitor values are calculated to give adequate low-frequency response as well as filtering of ripple.
Ideas for Exploration: (i) Replace the resistor $R_3$, $R_4$, and capacitor $C_5$ by a constant current source supplied from the positive supply rail; (ii) Employ a cascode amplifier in place of $Tr_3$. This will lower the distortion produced by the circuit, (iii) Redesign the system to deliver 100 W into 8 Ω using IRFP240 and IRFP9240 MOSFETS in the output stage.
9.11.3 Amplifier Clipping Indicator
The circuit in Fig. 9.33 gives an indication when clipping occurs in a power amplifier. It comprises a diode bridge connected to the output of the amplifier being monitored which ensures that signals of either polarity can be monitored. The signal drives two transistors connected as a silicon-controlled rectifier (see Chap. 14) such that if the voltage at the base-emitter junction of $Tr_1$ equals about 0.7 V, this transistor is turned on and thereby turns on $Tr_2$, the action of which further turns on $Tr_1$ latching both transistors fully on. They remain in this condition until the voltage across the arrangement goes to zero or the current through them goes to zero. When the transistors are turned on, current flows through the LED which then illuminates. Resistor $R_1$ limits the current through the LED to about 100 mA. Thus $R_1 = V_{pk}/100$ mA where $V_{pk}$ is the maximum peak output voltage of the amplifier. For an amplifier delivering output power $P$ into an 8 Ω speaker load, $V_{pk} = 4 \sqrt{P}$. Therefore, $R_1 = V_{pk}/100$ mA = $4 \sqrt{P}/0.1 = 40 \sqrt{P}$. For example, for $P = 100$ W, $R_1 = 40 \sqrt{100} = 400$ Ω. The potential divider formed by resistor $R_3$ and potentiometer $VR_1 = 1$ k sets the voltage to be applied to the base-emitter junction of $Tr_1$ (noting that $R_1$ is small). We allow for a 1 V drop across the LED and set the potentiometer at a value of say 700 Ω when triggering occurs for a given $V_{pk} = 4 \sqrt{P}$. Then
\[
\frac{4 \sqrt{P} - 1}{R_3 + 1000} = \frac{0.7}{700} \quad R_3 = 2000 \left( 2 \sqrt{P} - 1 \right)
\]
from which $R_3 = 2000 \left( 2 \sqrt{100} - 1 \right) = 38$ k. For example, for $P = 100$ W, $R_3 = 2000 \left( 2 \sqrt{100} - 1 \right) = 38$ k assists in turning on $Tr_2$. 
Ideas for Exploration: (i) Investigate the possibility of including a green LED in series with $R_3$ such that it illuminates when there is no clipping but goes off when clipping occurs since then the current through $R_3$ goes to zero.

9.11.4 Unity-Gain Buffer

The circuit in Fig. 9.34 uses two pairs of complementary transistors to realize a unity-gain buffer. The bases of $Tr_1$ and $Tr_2$ are connected and are at approximately zero potential. These transistors are biased using $R_1 = R_2 = 3.3 \, k$ resulting in transistor collector currents of

$$I_{c1} = I_{c2} = (15-0.7)/3.3k = 4.3 \, mA.$$  

The voltages at the emitters of $Tr_1$ and $Tr_2$ ($\pm V_{be}$) are applied to the bases of $Tr_3$ and $Tr_4$, respectively. The emitters of $Tr_3$ and $Tr_4$ are connected together via bias resistors $R_3 = R_4 = 3.3 \, \Omega$ with the signal output taken from the junction of these resistors. These resistors limit the quiescent current in these output transistors. Resistor $R_5 = 18 \, k$ in conjunction with potentiometer $VR_1 = 10 \, k$ enables the adjustment of the output offset voltage. Since all the transistors are in the common collector configuration, the circuit has a high input impedance and good frequency response. Also, because of the common collector output, the circuit is able to drive low-impedance loads. Small-signal complementary transistors such as the
2N3904 and 2N3906 or the 2N2222 and 2N2907 can be used to implement the circuit.

![Unity-gain buffer circuit](image)

**Fig. 9.34** Unity-gain buffer (a) with offset adjustment and (b) without offset adjustment

**Ideas for Exploration:** (i) Implement the circuit using the MPQ6502 quad package. In that case, resistors $R_3$ and $R_4$ may be eliminated (short-circuited) since the transistors in the package are matched. The offset components $V_{R_1}$ and $R_5$ may also be eliminated (open-circuited) (see Fig. 9.34b); (ii) Explore the circuit operation using a single-ended power supply.

### 9.11.5 Power Operational Amplifiers

A very simple method of realizing a power amplifier is to use an operational amplifier and boost the output current as shown in Fig. 9.35. The output of the operational amplifier drives a complimentary emitter follower with a resistor $R_3$ connected between the output of the
operational amplifier and the emitters of the two transistors. If the output current is less than $0.7 \, V/R_3$, then the transistors remain off, and the output current is supplied by the operational amplifier. As the current exceeds $0.7 \, V/R_3$, the voltage drop across $R_3$ exceeds $0.7 \, V$ and the transistors turn on $Tr_1$ for positive-going signals and $Tr_2$ for negative-going signals and supply the current. Crossover distortion is suppressed by the operation of resistor $R_3$ and the inclusion of the booster transistors in the feedback loop of the operational amplifier ensures that distortion introduced by these transistors is significantly reduced. For example, with $R_3 = 100 \, \Omega$ the limiting current is $0.7 \, V/100 = 7 \, mA$ above which the transistors take over. It is important to note that while the bulk of the output current is supplied by the transistors, base current to the transistors must be supplied by the operational amplifier. This limits the amount of current that can be delivered to about 1 A since with a transistor current gain of say 100, the base current demand for 1 A output is 10 mA which is the maximum current typically available from an operational amplifier. Further enhancement of the output current capacity can be achieved by the use of complimentary feedback pairs in place of the two transistors. The current gain for these pairs is better than 1000 in which case as much as 10 A can be delivered using this approach. In the system, $R_B = 100 \, k$ provides bias to the non-inverting input of the operational amplifier and $R_1$ and $R_2$ set the gain at $1 + R_2/R_1$. For a 741 operational amplifier operating from $\pm15 \, V$ supplies, the peak output voltage is about 12 V giving a power of
\[
P = \frac{(12/\sqrt{2})^2}{8} = 9 \, W
\]
into 8 \, $\Omega$ and 18 W into 4 \, $\Omega$. 
Another operational amplifier current booster circuit is shown in Fig. 9.36. The transistors are driven by current flowing into the power leads of the operational amplifier in response to a signal. One advantage of this circuit over the previous current booster is that $R_3$ and $R_4$ can be selected such that a quiescent current flows in the transistors. The result is that there is little or no crossover distortion.
Using a 741 op-amp, $R_3 = R_4 = 400 \, \Omega$ produced a quiescent current in the transistors of 20 mA. Setting $R_B = 100 \, k$, $R_2 = 9 \, k$ and $R_1 = 1 \, k$, a 1 V input resulted in a 10 V output. Like the first current booster circuit, enhancement of the output current capacity can be achieved by the use of complementary power Darlington pairs such as the MJ3001/MJ2501 (80 V, 10 A) or the TIP142/TIP147 (100 V, 10 A) in place of the two transistors. The current gain for these Darlington pairs can exceed 1000 enabling the circuit to deliver currents approaching 10 A. In the system, $R_B$ provides bias to the non-inverting input of the operational amplifier, and $R_1$ and $R_2$ set the gain at $1 + R_2/R_1$. Using this circuit, an OPA452 operational amplifier operating from ±35 V supply can deliver approximately 50 W into 8 Ω and 100 W into 4 Ω.

_Ideas for Exploration:_ (i) While both the operational amplifier and the complimentary emitter follower can be operated from the same bipolar supply, it is important that the supply is decoupled at the transistors and at the power pins to the operational amplifier. Also, separate ground connectors must be used for the speaker load and the
operational amplifier ground. This prevents “ground loops” from creating spurious results; (ii) Explore the use of the bridge configuration in order to increase the power output of the systems; (iii) Reconfigure this circuit to operate in the inverting configuration and examine its performance using simulation.

9.11.6 75 W Power Amplifier Using Feedback Pairs
This power amplifier in Fig. 9.37 utilizes complementary feedback pairs in the output stage. The design follows the procedures previously discussed. Resistors $R_{13} = 560 \, \Omega$ and $R_{14} = 560 \, \Omega$ provide current to $Tr_6$ and $Tr_7$ and also assist in the proper operation of the output transistors $Tr_5$ and $Tr_8$. For $P = 75 \, \text{W}$ into $8 \, \Omega$, using $V_{pk} = \sqrt{2PR_L}$,

$$V_{pk} = \sqrt{2 \times 75 \times 8} = 34.6 \, \text{V}.$$ 

Allowing for transistor saturation and other losses, the supply is selected to be $\pm V_{CC} = \pm 40 \, \text{V}$. 
Ideas for Exploration: (i) Replace the bootstrap arrangement in the collector of $Tr_3$ by a transistor constant current source; (ii) Introduce a transistor constant current source to supply the emitters of the differential pair $Tr_1$ and $Tr_2$. What improvement does this provide?

9.11.7 Research Project 1
This power amplifier is intended to deliver extremely high-power output. It must produce 250 W into 8 $\Omega$ or 500 W into 4 $\Omega$. The project requires the scaling up of the power MOSFET amplifier described in
Example 9.12 in order to produce these power levels. For $P = 250$ W into 8 $\Omega$, using $V_{pk} = \sqrt{2PR_L}$, $V_{pk} = \sqrt{2 \times 250 \times 8} = 63.2$ V. Allowing for transistor saturation and other losses, the supply is set at 75 V, and therefore, $\pm V_{CC} = \pm 75$ V. The number of MOSFETS in the output stage must at least be doubled compared to the 150 W circuit, therefore, giving eight devices: four n-channel and four p-channel. These can be Renesas 2SK2221 and 2SJ352 or Magnatec BUZ901 and BUZ906. This is a major project that should be undertaken with great care.

**Ideas for Exploration:** (i) Refer to the article “High-Power Audio Frequency Amplifier,” Elektor Electronics, May 1986, p60.

### 9.11.8 Research Project 2

Peter Walker and the Acoustical Manufacturing Company introduced the *current dumping amplifier* in 1975. It uses the system described in the op-amp power amplifier project in Fig. 9.35 where transistors are turned on to “dump” current into an external load. However, while the op-amp power amplifier uses negative feedback to reduce the distortion arising from the dumping action, the system developed by this company is claimed to cancel this distortion completely. The project requires the reader to implement the scheme in an amplifier and verify by an experiment that distortion cancelation does indeed occur. The basic system is shown in Fig. 9.38. It can be derived from the power op-amp circuit 1 of Fig. 9.35 by splitting resistor $R_3$ of that circuit into $R_3$ and $R_4$ and taking the output to the speaker load $R_L$ at the junction of these resistors. Note that as $R_4 \rightarrow 0$, the current dumping circuit reduces to the power op-amp circuit 1 of Fig. 9.35.
Using standard circuit analysis, for the system

\[ V_1 = A (V_i - \beta V_2) \] \hspace{1cm} (9.40)

where \( A \) is the gain of the low-power linear amplifier and \( \beta = R_1/(R_1 + R_2) \). The second equation is

\[ \frac{V_o}{R_L} = \frac{V_1 - V_o}{R_3} + \frac{V_2 - V_o}{R_4} \] \hspace{1cm} (9.41)

which reduces to

\[ \frac{V_o}{R_p} = \frac{V_1}{R_3} + \frac{V_2}{R_4} \] \hspace{1cm} (9.42)

where \( R_p = R_L//R_3//R_4 \). The third defining equation is

\[ V_2 = BV_1 \] \hspace{1cm} (9.43)

where \( B \) is the voltage gain of the current dumping transistors which is highly non-linear primarily as a result of crossover distortion.
Eliminating $V_1$ and $V_2$ from Eqs. (9.40), (9.42), and (9.43), we get

$$V_o = \frac{R_p}{R_3} \frac{A}{1 + \beta AB} \left( 1 + \frac{R_3}{R_4} B \right) V_i$$  \hspace{1cm} (9.44)

If the condition

$$\frac{R_3}{R_4} = \beta A$$  \hspace{1cm} (9.45)

is satisfied, then Eq. (9.44) reduces to

$$V_o = \frac{R_p}{R_3} A V_i$$  \hspace{1cm} (9.46)

The amplifier transfer function $A$ is frequency dependent and can be approximated as a pure integrator $A = \omega_T/s$ where $\omega_T = 2\pi f_T$ is the gain-bandwidth product of the amplifier and $s = j\omega$. In order to satisfy the condition Eq. (9.45), this frequency dependence can be counteracted by replacing resistor $R_4$ by an inductor whose impedance is given by $sL$.

Substituting these values into Eq. (9.45) gives

$$\frac{2\pi f_T}{s} \beta = \frac{R_3}{sL}$$

This reduces to

$$R_3 = 2\pi f_T \beta L$$

For example, for $f_T = 2$ MHz, $\beta = 0.4$ and $L = 2 \mu H$, then $R_3 = 2.5$ $\Omega$.

Thus, from Eq. (9.46), the output signal $V_o$ driving the speaker is independent of the non-linear dumper characteristic $B$ and depends only on the gain $A$ of the linear low-power amplifier. Therefore, the crossover distortion of transistors $Tr_1$ and $Tr_2$ is not present in the output signal.

(iii) Examine other distortion canceling schemes used by amplifier manufacturers or published in the audio engineering literature.

**9.11.9 Research Project 3**

This project involves the design of a *class D amplifier*. This is a class of amplifiers that operates by switching on and off the output to the external load. When on, the voltage across the switching device is low and when off, the current through the switching device is very low, therefore, there is little power loss in the switching devices and as a result such amplifiers have very high efficiencies (better than 90%). As a consequence, they require only small heatsink area since relatively low power is dissipated. The basic scheme is shown in Fig. 9.39. The input signal is compared with a triangular wave of a higher frequency of about 200 kHz using a comparator. The output of the comparator is a pulse width modulated waveform whose pulse widths vary according to the signal amplitude. This waveform then drives the push–pull MOSFET output stage, switching it fully on or fully off for each pulse. The output of this stage is applied to the loudspeaker through a low-pass LC filter to remove the unwanted switching components and recover the amplified analog signal.

*Fig. 9.39*  Class D amplifier

*Ideas for Exploration:* (i) Refer to International Rectifier Application Note AN-1071, “Class D Amplifier Basics” by Jun Honda and Jonathan Adams; (ii) Consider using the International Rectifier IRS2092 Class D Audio Amplifier Controller IC that contains the control and switching elements for driving the power MOSFETS.
9.11.10 Research Project 4

This project uses the improved crystal radio circuit in Fig. 2.72 of Chap. 2 and adds a power amplifier IC in order to drive a loudspeaker. The circuit is shown in Fig. 9.40 where the output of the common-emitter amplifier $Tr_1$ is used as the input to an LM386 low-power IC amplifier. The use of two amplification stages should enable a telescopic antenna to be used, instead of a long-wire antenna.

![Circuit Diagram](image)

*Fig. 9.40* Advanced Crystal Radio Using a Power Amplifier IC

*Ideas for Exploration:* (i) Check the signal strength with a telescopic antenna; (ii) Introduce the JFET radio frequency signal booster developed in Chap. 3 (Fig. 3.64a) in order to amplify the radio signal; (iii) Design and implement a radio frequency signal booster using a single-stage common-emitter amplifier similar to the amplifier based on $Tr_1$ in Fig. 9.40; (iv) Design a 9 V regulated DC supply in order to power the radio from the main supply (see Chap. 10).

9.11.11 Research Project 5

This project investigates the performance of an experimental power amplifier system that is developed using the power op-amp circuit of Fig. 9.36 and which can deliver higher output voltages than that circuit. The experimental circuit is shown in Fig. 9.41. Here, a 741 op-amp
drives transistors $Tr_3$ and $Tr_4$. In order to reduce loading on resistors $R_3$ and $R_4$, these transistors should be power Darlington pairs such as MJ1001 and MJ901 (80 V, 8 A, 90 W). The values of resistors $R_3$ and $R_4$ determine the quiescent current in $Tr_3$ and $Tr_4$. For Darlington pairs with a base-emitter voltage of 1.4V and using a quiescent current of 1.7mA for the 741; resistors $R_3$ and $R_4$ can be about 680Ω. The use of ±30V supplies allows the amplifier to deliver over 30W into an 8Ω speaker load. In order to enable the op-amp to operate from these high voltage supplies, transistors $Tr_1$ and $Tr_2$ are employed. Zener diodes $D_1$ and $D_2$ provide 15V at the base of these transistors which then deliver ±14.3V to the power supply terminals of the op-amp. The supply current to the op-amp drives resistors $R_3$ and $R_4$ via transistors $Tr_1$ and $Tr_2$. The output of the circuit is taken at the collectors of $Tr_3$ and $Tr_4$ which are connected. Resistors $R_6$ and $R_5$ enable the output $V_o$ of the amplifier system to be at a higher value than the op-amp is able to deliver. These resistor values, particularly that of $R_5$, would need to be sufficiently low in order that the current drawn from the op-amp be able to activate $Tr_3$ and $Tr_4$ via $R_3$ and $R_4$. The relationship is given by $V_o = V_{op}(1 + R_6/R_5)$ where $V_{op}$ is the output of the op-amp. Resistors $R_2$ and $R_1$ provide overall feedback and set the amplifier gain at $1 + R_2/R_1$. 
Ideas for Exploration: (i) Consider using small resistors in the emitters of $Tr_3$ and $Tr_4$ in order to stabilize the quiescent current in these transistors; (ii) Replace the Darlington pairs by power MOSFETS such as IRF9530 and IRF530 in which case resistors $R_3$ and $R_4$ would have to be re-calculated.

Problems
1. Using the configuration in Fig. 9.42 and a transistor with a current
gain of 50, design a low-power amplifier to deliver 60 mW into an 8 Ω load using a 6 V supply.

2. If the 8 Ω speaker in the above amplifier is replaced by a 15 Ω speaker, calculate the output power.

3. A power amplifier has an efficiency of 30% and delivers an output power of 15 W to a resistive load. Calculate the power dissipated and the DC input power to the amplifier.

4. A large signal amplifier delivers an output power of 25 W and consumes 75 W from the associated DC supply. Calculate its efficiency.

5. Using the configuration shown in Fig. 9.43, design a transformer-coupled amplifier delivering 1.5 W into 8 Ω and operating from a 16 V supply. Use a power Darlington with β = 2000.

6. Using the configuration shown in Fig. 9.44, design a transformer-coupled amplifier delivering 2 W into 8 Ω and operating from a 24 V supply. Use a power Darlington with β = 1000.

7. Explain the phenomenon of crossover distortion and the reason it occurs. Suggest one method of overcoming this problem.

8. Design a low-power amplifier using the topology of Fig. 9.12 and a 12 V supply.

9. For the amplifier circuit shown in Fig. 9.45, determine the quiescent current and the base voltage in transistor Tr3 if the output voltage is 4.5 V. Develop a design procedure for this configuration.

10. What would be the effect on amplifier performance of increasing the input and output capacitors? Discuss the use of a variable Zener circuit to adjust the output bias current.

11. Design a 500 mW amplifier using the circuit of Fig. 9.46. Introduce bootstrapping to improve the performance of this circuit.
12. Design a 5 W amplifier using the configuration of Fig. 9.47.

13. Compare the performances of the amplifiers designed in questions 11 and 12.

14. Identify the type of feedback that is used in the amplifier in Fig. 9.47 as well as the number of voltage gain stages.

15. Design a 20 W amplifier driving an 8 Ω speaker using the configuration in Fig. 9.16.

16. Design a 60 W amplifier driving a 4 Ω speaker using the configuration in Fig. 9.17. (i) Discuss the effect of including emitter resistors in the input stage; (ii) Design and introduce a constant current source in the differential amplifier stage and indicate how this improves amplifier performance; (iii) Design a short-circuit protection for the amplifier.

17. The power amplifier shown in Fig. 9.48 utilizes an output configuration referred to as quasi-complimentary symmetry since the two power transistors are of the same polarity. Analyze the circuit shown and investigate the operation of the output stage.

18. Design a 75 W power MOSFET amplifier using the circuit in Fig. 9.21.

19. In a power amplifier design a power transistor is expected to dissipate 75 W. Using a transistor that can dissipate 100 W at a junction temperature of 100°C determine the thermal resistance of the heatsink required for safe operation of this transistor. Use $\theta_{JC} = 0.4°C/W$ and $\theta_{CS} \approx 2°C/W$.

20. As a research project, modify the configuration in Fig. 9.48 to include another transistor stage at the input as in Fig. 9.16.

21. An audio power amplifier can be represented in a simplified
model as an amplifier $A_1$ with relatively low distortion $d_1$ driving an output stage $A_2$ with significant distortion $d_2$ (Fig. 9.49).

Positive feedback is applied around $A_1$ via $\beta_1$ and negative feedback is applied around the system through $\beta_2$. Show that when $A_1\beta_1 = 1$, the output is given by $V_o = \frac{V_i}{\beta_2} + \frac{d_1}{A_1\beta_2}$. This means that in the amplifier output signal $V_o$, the already low distortion $d_1$ is further reduced by the factor $A_1\beta_2$ and the major distortion $d_2$ completely vanishes!

Fig. 9.42  Circuit for Question 1
**Fig. 9.43** Circuit for Question 5

**Fig. 9.44** Circuit for Question 6
Fig. 9.45 Circuit diagram for Question 9
Fig. 9.46  Circuit for Question 11
Fig. 9.47 Diagram for Question 12
Fig. 9.48  Diagram for Question 17
Bibliography


Motorola Product Application Note AN-483B, Complementary Darlington Output Transistor in Audio Amplifiers, April 1974

[Crossref]


10. Power Supplies

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An electrical power source is essential for the operation of most electronic equipment. Some portable equipment such as radio receivers and pocket calculators may be battery operated, but most electronic equipment require an electrical supply. In this chapter, we examine the operation and design of linear power supplies that convert an AC voltage from the public mains supply into a stable DC voltage. At the end of the chapter, the student will be able to:

- Explain the operation of linear regulators.
- Design several forms of linear regulated power supplies.
- Utilize IC regulators in regulated power supplies.
- Design short-circuit protection circuits.

### 10.1 Basic System

A regulated power supply consists of several subsystems, a transformer, a rectifier, a filter and a voltage regulator, as shown in Fig. 10.1. The transformer converts the high AC mains voltage to a lower usable voltage while also providing isolation from the mains. The rectifier converts the low AC voltage from the transformer to a varying DC
voltage, while the filter removes the ripple from the rectified voltage, thereby converting it from high ripple content to low ripple content. Finally, the regulator converts the unregulated output of the filter to a regulated one where the DC voltage is very stable and ripple free. The power supply comprising only of transformer, rectifier and filter is referred to as an unregulated supply. When a regulator is added, the system is referred to as a regulated power supply.

![Diagram](image.png)

**Fig. 10.1** Basic power supply system

### 10.2 Rectification

The principle of rectification has been introduced in Chap. 1 where diode applications were discussed. In this chapter, more quantitative analysis is done so that design issues may be considered. The circuit shown in Fig. 10.2 is that of a half-wave rectifier with a transformer to reduce the mains voltage to a more desirable level. The diode permits current flow in one direction only. The voltage $V_S$ represents the secondary voltage of the transformer and is given by $V_S = V_m \sin \omega t$, where $\omega = 2\pi f$. For $f = 60$ Hz, $\omega = 377$ rad/s. The output waveform is shown in Fig. 10.3. Its average value is the ratio of the area under one cycle of the half-wave rectified voltage waveform and the waveform period $T = 1/60$ given by

$$ (10.1) $$
Fig. 10.2 Half-wave rectifier

\[ V_{AV} = \frac{T}{1/60} \left( \int V_m \sin 377t \, dt \right) = \frac{V_m}{\pi} \]

Note that the area under half of the output voltage cycle is zero. The supply output is comprised of two components: a DC component \( V_{DC} \).
which is essentially the average value of the output voltage, and an AC component $V_{AC}$ which determines the ripple content of the output voltage, i.e., $V_{AV} = V_{DC} + V_{AC}$. It is therefore desirable to reduce this ripple to a minimum.

The circuits shown below are full-wave rectifiers using a center-tapped transformer as shown in Fig. 10.4 and a bridge rectifier as shown in Fig. 10.5. The diodes conduct such that there is current flow in only one direction and both half-cycles of the waveform are utilized. The resulting output waveform is shown in Fig. 10.6. For this waveform, the average value increases to

$$
V_{AV} = \frac{\int_0^T V_m \sin 377t \, dt}{1/120} = \frac{2V_m}{\pi}
$$

(10.2)

where $T = 1/120$ since the waveform frequency is doubled. This value is twice as large as the value for the half-wave rectifier since both half-cycles are available in the output. The AC component still has a peak value of $V_m$. By definition, the effective or root mean square (rms) value of a periodic function of time is the square root of the ratio of the area under the square of one cycle of the waveform and the waveform period and for a sinusoidal waveform is given by

$$
V_{rms} = \sqrt{\frac{1}{T} \int_0^T V_m^2 \sin^2 377t \, dt}
$$

(10.3)
**Fig. 10.4** Full-wave rectifier using center-tapped transformer

**Fig. 10.5** Full-wave rectifier using a diode bridge

**Fig. 10.6** Output waveform of the full-wave rectifier
For a half-wave rectifier, Eq. (10.3) leads to \( V_{rms} = \frac{V_m}{2} \), while the value for a full-wave rectifier is the same as that for a sinusoidal waveform, i.e., \( V_{rms} = \frac{V_m}{\sqrt{2}} \).

### 10.3 Filtering

In order to convert the half- and full-wave rectifiers into viable supplies, the ripple component \( V_{AC} \) in the output needs to be reduced. This process is referred to as filtering, and one straightforward method of doing this is to connect a “reservoir” capacitor \( C \) across the output of the rectifier. If the capacitor is sufficiently large, it acts as a short circuit for the AC output voltage component, thereby removing it from the output signal. The resulting circuit consisting of transformer, rectifier and filter is called an unregulated supply.

The arrangement for the half-wave rectifier is shown in Fig. 10.7 with a load \( R_L \). As the transformer voltage that is applied to the diode rises, the diode conducts, and the capacitor is charged up to the peak voltage at point A in Fig. 10.8. When the transformer voltage falls such that the cathode voltage of the diode set by the capacitor is greater than the anode voltage set by the transformer, the diode turns off, and the output load is supplied by the capacitor which discharges through the load to point B in Fig. 10.8. The capacitor in effect prevents the output voltage from going to zero at any point in the cycle. The discharge rate depends on the value of the capacitor and the load current, and this voltage is exponential in form with time constant \( CR_L \) seconds. The instantaneous voltage across the capacitor and load is given by

\[
V_{DC} = \left( V_{pk} - V_D \right) e^{-t/CR_L}
\]

(10.4)

where \( V_D \) is the diode voltage drop. When the transformer voltage rises again above the capacitor voltage, the diode turns on the capacitor is recharged and the cycle is repeated. The resulting voltage waveform is shown in Fig. 10.8.
If the time constant $CR_L$ is chosen to be significantly larger than the period of the waveform, then the capacitor voltage will not fall significantly before being recharged through the diode, and therefore, the amplitude of the ripple voltage will be reduced. However, the conduction time $\Delta t_D$ of the diode is quite short compared with the period $T$ of the waveform as shown in Fig. 10.9. During this time, the current pulse delivered by the transformer and diode must supply the charge delivered to the load. Since $I = dQ/dt$ if $I_{DC}$ the load current is approximately constant, then the average current pulse $I_{pk}$ through the diode is given by

$$I_{pk} \Delta t_D = I_{DC} T \quad (10.5)$$

from which
Since $T \gg \Delta t_D$, the magnitude of the current pulse is quite large. Moreover because $\Delta t_D$ decreases as capacitor size increases, then the peak diode current increases. If the capacitor is too large, the diode peak current rating could be exceeded causing damage to the diode (and/or the transformer). Voltage and current waveforms are shown in Fig. 10.9. Because of the capacitor voltage, the diode is subjected to a maximum reverse voltage of $2V_s$, and therefore the diode PIV rating must be $PIV = 2V_s$.

The filtering of full-wave rectifiers, either that using the center-tapped transformer or the bridge rectifier version, can be similarly accomplished using a reservoir capacitor as shown in Figs. 10.10 and
Because of the availability of both cycles in the rectifier output, the capacitor is recharged twice as frequently as in the half-wave rectifier, and therefore the ripple content is approximately half of that in the half-wave rectifier.

![Full-wave rectifier with capacitive filter](image1)

**Fig. 10.10** Full-wave rectifier with capacitive filter

Also, since the capacitor discharge is reduced, the diode current flow during recharge is also reduced. The peak inverse voltage for the full-wave rectifier using the center-tapped transformer is $2V_s$, while that for the bridge rectifier is $V_s$. The output voltage and current waveforms for these circuits are shown in Fig. 10.11.

![Full-wave rectifier using diode bridge and capacitive filter](image2)

**Fig. 10.11** Full-wave rectifier using diode bridge and capacitive filter
10.4 Average DC Output Voltage

In order to calculate the peak-to-peak value of the output ripple and the average output voltage, certain approximations need to be made. Specifically, from Fig. 10.8 for the half-wave rectifier, the diode is off for most of the period T. During this time, the capacitor delivers a load current $I_{DC}$ and therefore discharges in the process. The decay is exponential but can be approximated as a linear decay. Also, the load current is assumed to be approximately constant during the discharge.

For a capacitor, the relationship $I = C dV/dt$ holds. This can be approximated by $I \approx C \Delta V / \Delta t$, where $\Delta V$ is a small change in capacitor voltage and $\Delta t$ is the associated small time interval over which this voltage change occurs. For the half-wave rectifier,

\begin{equation}
10.7
\end{equation}
where $\Delta V_R$ is the change in voltage of the reservoir capacitor and $T_H$ is the period of the half-wave rectified waveform. From this, $T_H \approx T = 1/f$ the peak-peak output ripple is given by

$$\Delta V_R = \frac{I_{DC}T}{C} = \frac{I_{DC}}{Cf}$$

(10.8)

where $f$ is the frequency of the input voltage. For a full-wave rectifier, the period $T_F$ of the rectified waveform is half that of the half-wave rectifier and therefore $T_F \approx T/2 = 1/2 f$. Hence for the full-wave rectifier, the peak-peak output ripple is given by

$$\Delta V_R = \frac{I_{DC}T}{C} = \frac{I_{DC}}{2Cf}$$

(10.9)

From this, the average DC output voltage is

$$V_{DC} = V_{pk} - \Delta V/2$$

(10.10)

**Example 10.1** Using the circuit in Fig. 10.7, design a half-wave unregulated power supply that can deliver 12 V DC at 1 A with less than 2.5 V peak-to-peak ripple.

**Solution** Since the peak transformer voltage is greater than the root mean square value by a factor of 1.414, it is reasonable to choose the transformer voltage $V_{rms}$ to be close to the required DC output voltage, i.e., $V_{rms} = 10$ V. Also, to prevent transformer heating, the transformer secondary current rating should be larger than the maximum load current by at least a factor of 1.5, i.e., $I_{rms} (s) = 1.5 I_{DC} (max) = 1.5$ A. Choose a diode with $I_{AV} \geq I_{DC} (max) = 1$ A and

$$PIV > 2V_{pk} = 24 \sqrt{2} = 33.6 \text{ V}.$$ Capacitor $C$ is given by

$$C = \frac{I_{DC}}{f \Delta V} = \frac{1}{60 \times 2.5} = 6666 \mu F.$$ A rough indication of the output voltage
under full-load conditions is given by \( V_{DC} = V_{pk} - \Delta V/2 = 14 - 2.5/2 \approx 13. \) The capacitor DC working voltage should be at least 10% higher than the peak voltage of the supply in order to provide a safety margin. The solution is shown in Fig. 10.13.

![Half-wave unregulated supply](image)

**Example 10.2**  Design a full-wave unregulated power supply delivering 15-V DC at 1 A with less than 1.5 V peak-to-peak ripple. Use a center-tapped transformer as in Fig. 10.10.

**Solution**  Since the peak transformer voltage is greater than the root mean square value by a factor of 1.414, we choose the transformer voltage \( V_{rms} \) to be close to the required DC output voltage, i.e., \( V_{rms} = 12 \) V. Also, to prevent transformer heating, the transformer secondary current rating should be larger than the maximum load current by at least a factor of 1.5, i.e., \( I_{rms} (s) = 1.5I_{DC} (max) = 1.5 \) A. Choose a diode with \( I_{AV} \geq I_{DC} (max) = 1 \) A and \( PIV > 2V_{pk} = 30 \sqrt{2} = 42.4 \) V.

Capacitor \( C \) is given by \( C = \frac{I_{DC}}{2f\Delta V} = \frac{1}{2 \times 60 \times 1.5} = 5555 \) \( \mu F \). A rough indication of the output voltage under full-load conditions is given by \( V_{DC} = V_{pk} - \Delta V/2 = 17 - 1.5/2 \approx 16. \) In both designs, diode voltage drops and transformer winding resistance reduce the output voltage. The solution is shown in Fig. 10.14.
Example 10.3  Repeat the design in Example 10.2 using a diode bridge as in Fig. 10.11.

Solution  We again choose the transformer voltage $V_{rms}$ to be close to the required DC output voltage, i.e., $V_{rms} = 12 \text{ V}$. Also, to prevent transformer heating, the transformer secondary current rating should be larger than the maximum load current by at least a factor of 1.5, i.e., $I_{rms} = 1.5 I_{DC \text{ (max)}} = 1.5 \text{ A}$. Choose a diode with $I_{AV} \geq I_{DC \text{ (max)}} = 1 \text{ A}$ and $PIV > V_{pk} = 15 \sqrt{2} = 21.2 \text{ V}$. Capacitor $C$ is given by

$$C = \frac{I_{DC}}{2f_{AV}} = \frac{1}{2 \times 60 \times 1.5} = 5555 \text{ \mu F}.$$ 

The diode voltage drops and transformer winding resistance reduce the output voltage. The solution is shown in Fig. 10.15.
10.5 Bipolar Unregulated Power Supplies
Many electronic devices, especially operational amplifiers, require both positive and negative supply voltages. These voltages are defined relative to a common ground terminal. Such a supply is referred to as a bipolar supply and is shown in Fig. 10.16. In this circuit, a center-tapped transformer is used to drive four diodes with the center tap serving as the common ground. Diodes $D_1$ and $D_2$ provide positive full-wave rectification and make terminal 1 positive with respect to the center tap, while diodes $D_3$ and $D_4$ provide negative full-wave rectification and make terminal 2 negative relative to the center tap. Capacitors $C_1$ and $C_2$, respectively, filter the positive and negative voltages. It is possible to realize a bipolar unregulated supply using a single winding transformer. This elegant circuit is shown in Fig. 10.17. Each section is effectively a half-wave rectifier and therefore would in general produce twice as much ripple as the circuit of Fig. 10.16. However, it does not require a center-tapped transformer, and this is its main advantage. Moreover, this circuit can function as a voltage doubler (as seen in the Zener diode example of Fig. 1.69 in Chap. 1) by moving the ground to either the $+V$ or the $-V$ terminal.

![Bipolar unregulated power supply](image)

*Fig. 10.16* Bipolar unregulated power supply
10.5.1 Power Supplies for Class B Power Amplifiers

These unregulated power supplies are suitable for supplying power to the class B power amplifiers in Chap. 9. For these cases, since the output transistors conduct on alternative half-cycles, the power supply delivers current on alternative half-cycles as well. Therefore from Eq. (10.1), the average current \( I_{av} \) demanded by these amplifiers is \( I_{av} = I_{pk}/\pi \) where \( I_{pk} \) is the peak output current of the amplifier. Therefore in the design of unregulated power supplies for these amplifiers, the value of current used in the calculation of the filter capacitor is \( I_{av} \).

Example 10.4  Design a full-wave unregulated power supply delivering 50V DC as required by the 25 W medium power amplifier of Fig. 9.16 in Chap. 9. Use a diode bridge system as in Fig. 10.15.

Solution  Since the peak transformer voltage is greater than the root mean square value by a factor of 1.414, in order to achieve the 50 V requirement we choose the transformer voltage \( V_{rms} \) to be \( V_{rms} = 40 \text{ V} \). The peak voltage is then \( 40 \sqrt{2} = 56.7 \text{ V} \). The peak current demand of the amplifier is \( I_{pk} = 2.5 \text{ A} \) and hence the average current to be delivered by the power supply is \( I_{av} = 2.5A/\pi = 0.8 \text{ A} \). The circuit will be designed to deliver 1 A. Choose a diode with \( I_{AV} \geq I_{DC(max)} = 1 \text{ A} \) and \( PIV > V_{pk} = 40 \sqrt{2} = 56.6 \text{ V} \). Allowing a 3 V peak-to-peak ripple in the
supply voltage, capacitor $C$ is given by

$$C = \frac{I_{av}}{2f\Delta V} = \frac{1}{2 \times 60 \times 3} = 2777 \ \mu F.$$

This power supply can also be implemented using a center-tapped transformer of output 80 V (40-0-40) as in Fig. 10.14.

**Example 10.5** Using the circuit in Fig. 10.13, design a half-wave unregulated power supply that can deliver 35-V DC as required by the 10 W power amplifier in Example 9.8 of Chap. 9.

**Solution** Since the peak transformer voltage is greater than the root mean square value by a factor of 1.414, in order to achieve the 35 V requirement we choose the transformer voltage $V_{rms}$ to be $V_{rms} = 28$ V. This results in a peak supply voltage of $40 \sqrt{2} = 56.7$ V. The peak current demand of the amplifier is $I_{pk} = 1.6$ A and hence the average current to be delivered by the power supply is $I_{av} = 1.6A/\pi = 0.5$ A. The circuit will be designed to deliver 1 A. Choose a diode with $I_{AV} \geq I_{DC}(\text{max}) = 1$ A and $PIV > 2V_{pk} = 56 \sqrt{2} = 79$ V. Allowing a 4 V peak-to-peak ripple in the supply voltage, capacitor $C$ is given by

$$C = \frac{I_{av}}{f\Delta V} = \frac{1}{60 \times 4} = 4166 \ \mu F.$$

**Example 10.6** Design a full-wave unregulated bipolar power supply delivering ±50V DC at 5 A peak current with less than 5 V peak-to-peak ripple to supply the 100 W power amplifier in Example 9.10 of Chap. 9.

**Solution** The full-wave rectifier system shown in Fig. 10.16 is used. In order to produce ±50 V, an 80 V center-tapped transformer (40-0-40) is used. When rectified the peak output at each supply will be $40 \sqrt{2} = 56.6$ V. Designing for a maximum peak-to-peak ripple is 3 V and allowing for diode voltage drop and transformer resistance will give an average output voltage of about ±50 VDC. The transformer current rating is chosen as 4 A which is sufficient to deliver the 5 A peak current requirement into 8 Ω. The average current demand from the positive and negative supplies is $5/\pi = 1.6$ A and hence using a 2 A demand, the
filter capacitors are given by \[ C = \frac{I}{2f\Delta V} = \frac{2A}{2 \times 60 \times 3} = 5555 \ \mu F. \] Use \( C = 5000 \ \mu F \) with 75 VDC working voltage. A diode bridge with PIV 200 V and 5 A rating is used to provide the rectification. The circuit is shown in Fig. 10.18.

![Diagram](image)

**Fig. 10.18** Bipolar Unregulated Supply for Example 10.6

**Example 10.7** Design a half-wave unregulated bipolar power supply delivering ±35 V DC at 3.5 A peak current with less than 4 V peak-to-peak ripple to supply the 50 W MOSFET power amplifier in Fig. 9.32 of Chap. 9.

**Solution** The half-wave system shown in Fig. 10.17 is used. In order to produce ±35 V, a 60 V center tap transformer is used. When rectified the peak output on each supply will be \( 40 \sqrt{2} = 56.6 \) V. The maximum peak-to-peak ripple is 4 V, and allowing for diode voltage drop and transformer resistance will give an average output voltage of about ±35 VDC. The transformer current rating is chosen as 3 A which is sufficient to deliver the 3.5 A peak current requirement into 8 \( \Omega \). The average current demand is \( 3.5 A/\pi = 1.1 A \). The filter capacitors are given by \[ C = \frac{I}{f\Delta V} = \frac{1.1A}{60 \times 4} = 4583 \ \mu F. \] Use \( C = 5000 \ \mu F \) with 75 VDC working.
voltage. A diode bridge with PIV 100 V and 4 A rating is used to provide the rectification.

### 10.6 Voltage Multipliers

It is possible to produce a high DC voltage using a low-voltage transformer. This can be done using a combination of diodes and capacitors along with the transformer. Such circuits rely on capacitor charge storage and are therefore not able to deliver high currents. In the circuit of Fig. 10.19, when the AC input is negative-going such that diode $D_1$ is forward-biased, capacitor $C_1$ is charged up to the peak transformer voltage $\sqrt{2}V_s$ with the polarity shown. During this time $D_2$ is reverse-biased. When the transformer input reverses and is positive going, $D_1$ is reverse-biased, but $D_2$ is now forward-biased allowing capacitor $C_2$ to charge up to the sum of the transformer voltage $\sqrt{2}V_s$ and the voltage $\sqrt{2}V_s$ on $C_1$, both of which are in series. After a few cycles, capacitor $C_2$ charges up to $2\sqrt{2}V_s$ making this circuit a voltage doubler. When a load is connected, however, $C_2$ will be constantly discharging, and therefore, the output voltage will in general be less than $2\sqrt{2}V_s$ and will have high ripple content. Increasing the size of the capacitors will reduce but not eliminate the problem.

![Voltage doubler circuit](image)

**Fig. 10.19** Voltage doubler
The principle of the voltage doubler may be extended to voltage tripling, quadrupling and beyond. In the voltage tripler circuit of Fig. 10.20, during the half-cycle when terminal A is positive relative to terminal B, diode $D_1$ turns on, and $C_1$ is charged to $\sqrt{2}V_s$. When the transformer voltage reverses such that terminal B is positive relative to terminal A, diode $D_2$ conducts and the transformer voltage in series with the voltage across $C_1$ together charge capacitor $C_2$ to $2\sqrt{2}V_s$. When A is again positive relative to B, diode $D_3$ conducts, and the series combination of the transformer voltage and the voltage across capacitor $C_2$ charges capacitor $C_3$ to $2\sqrt{2}V_s$. After a few cycles, the output voltage across $C_3$ rises to approximately $2\sqrt{2}V_s$.

![Fig. 10.20 Voltage tripler](image)

Any number of multiplications of the basic input voltage is realized in the multiplier circuit of Fig. 10.21. The peak transformer secondary voltage $\sqrt{2}V_s$ is multiplied by the number of cascaded stages resulting in an output voltage at terminal 1 of $2\sqrt{2}V_s$ relative to terminal A where $n$ corresponds to the number of diodes in the circuit path. As can be seen from the circuit, $n$ is always an even number. If point B is grounded instead of A, then the output is taken at terminal 2 and is still
but now \( n \) is an odd number. Thus, any multiplication of \( 2 \sqrt{2} V_s \)
is possible using this circuit. The diode and capacitor voltage ratings must be twice the transformer output voltage \( \sqrt{2} V_s \). Again, the capacitor values and diode current ratings depend on the output current.

![General voltage multiplier](image)

**Fig. 10.21** General voltage multiplier

### 10.7 Voltage Regulators

Unregulated power supplies have certain undesirable characteristics. Firstly, the DC output voltage decreases, and the AC ripple increases as load current increases. Secondly, the output voltage changes significantly in response to a changing input voltage resulting from changing line voltage. These disadvantages can be minimized by adding a voltage regulator to the unregulated supply. The resulting supply is called a regulated power supply. The function of the regulator is therefore to maintain a constant output voltage under conditions of changing load current and changing line voltage. There are two types of voltage regulators: (a) the shunt regulator in which a control element is in parallel (shunt) with the load and (b) the series regulator in which a control element is in series with the load.

In a **shunt regulator**, the regulating device is placed in parallel with the load and works in conjunction with a resistor in series with the load and the unregulated supply. The regulator operates by varying the current through the control element depending on the load current. This results in a varying voltage drop across the series resistor such that the load voltage remains constant. One example of a shunt regulator is the Zener diode regulator which was introduced in Chap. 1. In a **series**
regulator, the regulating device is placed in series with the load and the unregulated supply, and the voltage across the control element is adjusted so that the load voltage remains constant. Examples of these types of regulators will be discussed in this chapter.

### 10.7.1 Ripple and Regulation

The performance of a voltage regulator can be specified by several parameters. One of these gives an indication of the ripple content of the DC output. The output of a rectifier contains considerable ripple, which would have to be reduced by the regulator in order to make the DC voltage useable. The quality of the resulting output may be expressed using percent ripple $R$ which is defined as

$$ R = \frac{\text{Ripple voltage (rms)}}{\text{Average or DC output voltage}} \times 100\% \quad (10.11) $$

**Example 10.8** An unregulated voltage supply delivering current to a load has a DC output voltage of 15 V and a ripple voltage of 0.75 V $\text{rms}$. Calculate the percent ripple.

**Solution** Using Eq. (10.11), the percent ripple is given by

$$ R = \frac{0.75}{15} \times 100 = 5\%. $$

This parameter is however difficult to calculate because of the difficulty in determining the $\text{rms}$ ripple voltage in the output. A ripple measure that is more easily evaluated is the ripple factor $r$ given by

$$ r = \frac{\text{Peak to peak ripple in output voltage}}{\text{Average or DC output voltage}} \quad (10.12) $$

**Example 10.9** An unregulated voltage supply has a DC output voltage of 20 V and peak-to-peak ripple voltage of 2 V. Calculate the ripple factor.

**Solution** Using Eq. (10.12), the ripple factor is given by

$$ r = \frac{2}{20} = 0.1. $$

The peak-to-peak output voltage ripple involved in this specification is easily determined using an oscilloscope. Both percent ripple and ripple
Another factor of importance in a power supply is load regulation which specifies the change in the DC output voltage arising from changing load current. This factor is given by

\[
\text{Load regulation} = \frac{V_{DC \; \text{(no load)}} - V_{DC \; \text{(full load)}}}{V_{DC \; \text{(full load)}}} \times 100\%
\]  

(10.13)

where \(V_{DC \; \text{(no load)}}\) is the average value of the output voltage when the external load resistance is removed and \(V_{DC \; \text{(full load)}}\) is the average value of the output voltage when the external load resistance is at a minimum. In practical circuits, diode resistance and transformer winding resistance will result in voltage drops that cause the output voltage to be reduced with increasing load current. It is desirable to reduce this drop and thereby have a low load regulation.

**Example 10.10** A DC voltage supply delivers 30 V when unloaded and 27 V when delivering its full load current. Calculate the load regulation for this supply.

**Solution** Using Eq. (10.13), the load regulation is given by

\[\frac{30 - 27}{27} \times 100 = 11.1\%\]

**Line regulation** specifies the change in the DC output voltage resulting from a change in the line or input voltage. It is a measure of effectiveness of the regulation (output voltage stability) in the presence of changing input voltage. It is given by

\[
\text{Line regulation} = \frac{\Delta V_{out}}{\Delta V_{in}} \times 100\%
\]

(10.14)

where \(\Delta V_{out}\) is the change in the output voltage of the regulator and \(\Delta V_{in}\) is the associated change in the input voltage to the regulator with constant load. Ideally, both line and load regulation should be zero, and in practice, the values are less than 0.01\% for good regulators. The ratio \(\Delta V_{out}/\Delta V_{in}\) is sometimes referred to as stability factor.
Example 10.11  A DC voltage supply delivers 50 V while delivering current to a load. If the output voltage increases by 0.5 V for an input voltage change of 3 V, calculate the line regulation for this supply.

Solution  Using Eq. (10.14), the line regulation is given by 

$$\frac{0.5}{3} \times 100 = 3.3\%$$

10.7.2 Zener Diode Regulator

As discussed in Chap. 1, the Zener diode is essentially a semiconductor diode designed to operate in the reverse-biased region. In the forward-biased region, the device operates as a normal diode, while in the reverse bias region, it again operates like a diode for voltages less than the breakdown voltage. For voltages exceeding the breakdown (Zener) voltage, the Zener diode conducts and operates along that part of the $I/V$ characteristic having a steep slope. Providing the current is prevented from rising too high, the voltage across the Zener in this condition is approximately constant at the breakdown or Zener voltage, and the dynamic resistance $r_d$ is quite low, ranging from a few ohms to about 50 Ω. In this region, the voltage across the Zener is approximately constant, and when operated here, the device provides a constant voltage output.

The current through the Zener in this region is limited by the power rating $P_D$ of the diode and must be operated such that $V_z I_z < P_D$. If $I_z(\text{max}) = P_D/V_z$ is exceeded, the diode will be destroyed. Also, $I_z$ must not fall below the minimum value $I_z(\text{min})$; otherwise, the Zener voltage will fall. This corresponds to the knee of the curve in Fig. 10.22. Zener diodes are available in voltages ranging from about 2.4 V to about 200 V. The power ratings range from about 1/4 W to over 100 W.
The Zener diode operates as an effective voltage regulator. The basic system is shown in Fig. 10.23. A (varying) voltage $V_i$ is applied to the Zener diode through a resistor $R$ that limits the current. The voltage $V_Z$ across the Zener is then applied to a load $R_L$. If $V_i$ increases, say, more current flows through the Zener but based on its characteristic, $V_Z$ stays approximately constant. Similarly, if $V_i$ decreases, the current though the Zener drops but again $V_Z$ remains constant. Thus, the voltage $V_Z$ is approximately constant despite changes in the input voltage or load current. The load $R_L$ therefore sees a regulated (constant) voltage providing $I_{z_{min}} \leq I_z \leq I_{z_{max}}$. This design of a Zener-regulated power supply involves the determination of $R$. In order to do so, the minimum
and maximum values of $V_i$ as well as the maximum value of $I_L$ must be known. When $I_L$ is at maximum corresponding to minimum $R_L$, and $V_i$ at a minimum, the value of $R$ must be such that $I_z \geq I_{z\text{min}}$.

![Zener diode regulator](image)

**Fig. 10.23** Zener diode regulator

Thus,

$$\frac{V_{i\text{min}} - V_Z}{R} - I_{L\text{max}} \geq I_{z\text{min}}$$  \hspace{1cm} (10.15)

i.e.

$$I_D = I_o \left( \frac{V_D}{e^{mV_T}} - 1 \right)$$  \hspace{1cm} (10.16)

When $V_i$ rises and $I_L$ goes to zero (load removed), the current through the Zener is at its maximum, and the required power rating $P_D$ of the diode must satisfy

$$P_D > V_Z \frac{V_{i\text{max}} - V_Z}{R}$$  \hspace{1cm} (10.17)

Zener-regulated power supplies are useful for low-power applications involving less than a few watts since under the condition where no load current is being supplied, the Zener must accommodate the full load current.

In order to determine the ripple at the output of the Zener diode regulator, the dynamic resistance of the Zener must be considered. The dynamic resistance is the reciprocal of the slope of the diode
characteristic in the operating region. It is an indication of the resistance of the diode to small voltage and current changes. The value is typically in the range 5–50 Ω. The actual circuit under small-signal conditions is equivalent to that shown Fig. 10.24. For input ripple voltage $v_i$, the output ripple $v_R$ is given by

$$v_R = v_i \frac{r_d//R_L}{r_d//R_L} = v_i \frac{r_d}{R+R_L}$$

(10.18)

where $r_d \ll R_L$. Hence to minimize $v_R$, $R$ should be as large as possible, for example, by using a large resistor or a constant current diode. Hence in (10.16), equality is used with $I_{z\min}$ set at a value determined by the specification sheet. If the load is variable and $V_i$ is fixed, then $V_{imin} = V_i$. If $V_i$ is variable and the load is fixed, then at no time will current flowing through $R$ all flow into the Zener since some current will always be flowing into the load. Hence (10.17) becomes

$$P_D > V_Z \left( \frac{V_{i\max} - V_Z}{R} - I_L \right)$$

(10.19)

Fig. 10.24 Equivalent circuit of Zener diode regulator

This circuit has the advantage of short-circuit protection provided by the presence of resistor $R$ which will act to limit excessive current to the load.

Example 10.12 A voltage from an unregulated supply varies between a minimum value of 16 V and a maximum value of 20 V. Using this
unregulated supply, design a Zener-regulated supply that delivers 10-V DC with a current capacity of 10 mA.

**Solution** The basic circuit is shown in Fig. 10.23. The first step is to choose a 10-V Zener in order to deliver the required output voltage. The power rating will be determined later. To determine $R$ we consider the case where Zener current is at a minimum. This occurs when the input voltage is at a minimum, in this case 16 V, and the load current is at a maximum at 10 mA. We determine from diode specifications the minimum diode current for proper Zener operation. Assume a value of 5 mA. The voltage across $R$ is $(16 - 10) V$ and the current through $R$ is $(10 + 5) mA$. $R$ is therefore given by $R = \frac{(16-10)}{(10+5)} \times 10^3 = 400 \ \Omega$. Note that if the load were suddenly removed, then the current through D would rise to 15 mA when the input voltage is at 16 V. To determine the diode power rating, we calculate the maximum current through the diode. This occurs when the unregulated input voltage is at a maximum of 20 V and the load current is at a minimum (zero) corresponding to a removal of the load. The voltage across $R$ is then $(20 - 10) = 10 V$, and hence, the current $I_D$ through $D$ is given by $I_D = \frac{10}{400} = 25 \ mA$. This current flows through $R$, and hence the required Zener power rating $P_D$ is given by $P_D = I_D \cdot V_D = 25 \ mA \times 10 \ V = 0.25 \ W$. We choose a 1/2 W diode to provide a safety margin and for longer diode life. In this design, the input ripple voltage is $(20 - 16) = 4 \ V$ pk-to-pk. Hence, assuming $r_d = 10 \ \Omega$, the output ripple voltage is $v_R = \frac{10}{400+10} \times 4 = 0.1 \ V$. The ripple factor $r$ is then $A_V = \frac{-9}{0.4+0.025} = -21$. The circuit is shown in Fig. 10.25.
10.7.3 Simple Series Transistor Regulator

One method of improving the current capacity of the Zener regulator is the use of a transistor in the emitter follower configuration. A simple single transistor regulator of this type is shown in Fig. 10.26. It utilizes the Zener diode regulator and an npn transistor connected as an emitter follower. The transistor collector is supplied from the unregulated voltage source. Thus, the Zener voltage is provided at the transistor emitter giving an output of \( V_o = V_z - 0.7 \) volts. The transistor effectively increases the load current capacity of the Zener by a factor of the transistor current gain. Alternatively, since the transistor base current is significantly less than the load current \( I_B \ll I_L \) for large transistor current gain, the changes in base current with large changes in load current are small. Therefore, the Zener current does not change by very much. Hence the output voltage is quite stable for large load current changes. The circuit output impedance is given by

\[
Z_O = \frac{r_d + h_{ie}}{1 + h_{fe}} \tag{10.20}
\]
The voltage $V_i$ must always be larger than $V_z$ (by a few volts) to ensure that the transistor is properly biased. In order to determine the ripple at the output with a load $R_L$, consider the equivalent circuit of the regulator shown in Fig. 10.27. Then

$$\frac{v_R}{R_L} = (v_i - v_R) h_{oe} + \left(1 + h_{fe}\right) i_b$$

(10.21)

$$i_b = \frac{-v_R}{h_{ie}}$$

(10.22)

giving

$$\frac{v_R}{v_i} = \frac{h_{oe}}{1 + h_{fe} + h_{oe}} \frac{1}{1 + \frac{h_{oe}}{r_e} + \frac{h_{oe}}{R_L}}$$

$$= \frac{1}{1 + \frac{r_{oe}}{r_e} \left(1 + \frac{1}{R_L}\right)}$$

(10.23)

where $r_{oe} = \frac{1}{h_{oe}}$ and $r_e = \frac{h_{ie}}{1 + h_{fe}}$. Now $r_{oe} \left(\frac{1}{R_L} + \frac{1}{r_e}\right) \gg 1$. Hence,
\[
\frac{v_R}{v_i} = \frac{R_L/\!\!/r_e}{r_{oe}}
\]

\(r_{oe}\) is of the order 10^5 \(\Omega\) and \(r_e\) is of the order 10^2 \(\Omega\), hence \(\frac{v_R}{v_i} \approx 10^{-3}\).

Thus, the ratio is quite small indicating that the ripple output of the emitter follower regulator is quite low.

Fig. 10.27 Equivalent circuit of single transistor regulator

Example 10.13  Design a single transistor regulated supply using a Zener diode capable of delivering 12 V at 100 mA. Use a half-wave rectifier to drive the regulator.

Solution  For a 12-V output, in order to allow for sufficient voltage across the transistor, we choose a transformer with secondary voltage \(V_S\) of 15 V. This gives a peak output voltage of \(12\sqrt{2} = 17\) V. If we set a maximum peak-to-peak ripple of the unregulated supply of 1 V, then using (10.8), the required capacitor \(C\) is given by

\[
C = \frac{I_{DC}}{\Delta V_{Rf}} = \frac{0.1}{1\times60} = 1667 \ \mu F.
\]

In order to realize a 12-V output, we choose a Zener having a voltage \(V_Z = 12 + 0.7 = 12.7\) V. The closest available voltage is 13 V. Let the current through the Zener be 5 mA
chosen for good Zener operation. A transistor with a current gain of 50 when delivering the full current of 100 mA will have a base current of 100 mA/50 = 2 mA. This must be supplied by the Zener. Then from (10.16),

\[ R = \frac{(V_S \text{ (min)} - V_Z)}{(2 + 5)} \text{ mA} = \frac{(15\sqrt{2} - 1 - 13)}{(2 + 5)} \text{ mA} = 1 \text{ k}\Omega \]

Note that the minimum voltage drop across the transistor is \( V_S \text{ (min)} - V_O = 25 - 1.5 - 15 = 9 \text{ V} \). This circuit can be modified to deliver higher currents by using a Darlington pair instead of a single transistor. In such a case, the design proceeds as before but using the gain of the Darlington pair.

**Example 10.14**  Design a regulated supply using a Darlington pair and a Zener diode that delivers 15 V at 1 A. Use a full-wave rectifier to drive the regulator.

**Solution**  For a 15-V output, in order to allow for sufficient voltage across the transistor, we choose a transformer with secondary voltage \( V_S \) of say 18 V. This gives a peak output voltage of \( \sqrt{2} \times 18 = 17 \text{ V} \). If we set a maximum peak-to-peak ripple of the unregulated supply of 1.5 V, then using (10.8), the required capacitor \( C \) is given by

\[ C = \frac{I_{DC}}{\Delta V_{RF}} = \frac{1 \text{ A}}{1.5 \times 120} = 5555 \text{ \mu F} \]

In order to realize a 15-V output, we choose a Zener diode having a voltage \( V_Z = 15 + 1.4 = 16.4 \text{ V} \). The closest available voltage is 16 V. Let the current through the Zener be 5 mA chosen for good Zener operation. A Darlington pair with a current gain of 1000 when delivering the full current of 1 A will have a base current of \( 1A/1000 = 1 \text{ mA} \). This must be supplied by the Zener. Then,

\[ R = \frac{(V_S \text{ (min)} - V_Z)}{(1 + 5) \text{ mA}} = \frac{(18\sqrt{2} - 1.5 - 16)}{(1 + 5) \text{ mA}} = 1.3 \text{ k}\Omega \]

Note that the minimum voltage drop across the transistor is \( V_S \text{ (min)} - V_O = 25 - 1.5 - 15 = 9 \text{ V} \). The full circuit is shown in Fig. 10.28.
Fig. 10.28 Regulated power supply using Darlington pair

This configuration utilizing a Darlington transistor is especially well-suited for introducing a variable voltage output. This is because the high input impedance of the Darlington allows the employment of a potentiometer as shown in Fig. 10.29. The loading on the potentiometer is minimal, and accurate voltage variation can be realized.

Fig. 10.29 Transistor regulator with variable output voltage

Short-circuit protection of the basic single transistor regulator can be realized by the introduction of a fuse at the output. Electronic short-circuit protection is easily realized as shown in Fig. 10.30. The protection circuit comprises $Tr_2$ and $R_X$. When there is a current overload and the protection transistor $Tr_2$ turns on, the base current to the pass transistor is limited, and the Zener voltage falls. This circuit is
simple and works very well. For example, to limit current to 100 mA, \(R_X = 0.7 \text{ V/0.1 A} = 7 \Omega\). The \(V-I\) characteristic for the circuit with electronic protection is shown in Fig. 10.31.

![Transistor regulator with electronic protection](image)

**Fig. 10.30** Transistor regulator with electronic protection
This circuit has the disadvantage of causing a slight change in the regulated output voltage as current flows through $R_X$. This problem can be overcome by placing the protection transistor in the position shown in Fig. 10.32. In this position the regulated output is unaffected by the voltage drop across $R_X$.

![Diagram](image)

**Fig. 10.32** Changed position for protection transistor

The second transistor introduced to provide electronic protection can provide that protection in a different manner as shown in Fig. 10.33. The introduced transistor is a pnp transistor along with resistor $R_2$ and signal diode $D_2$. The collector current $I_{C1}$ of $Tr_1$ flows out of the base of $Tr_2$ into $R_2$. This current results in a collector current $I_{C2}$ in $Tr_2$ which flows through diode $D_2$ also into $R_2$. The current flowing in $R_2$ is
therefore made up of the collector currents of the two transistors and is
given by \( (V_Z - 0.7)/R_2 \). As load current increases, the current through \( D_2 \)
decreases with a consequent fall in the voltage across \( D_2 \). Eventually \( D_2 \) turns off and all of the current through \( R_2 \) is supplied by \( Tr_1 \). This results in a maximum current through \( Tr_2 \) into the load given by
\[
I_{L(max)} = h_{fe2}(V_Z - 0.7)/R_2
\]
where \( h_{fe2} \) is the current gain of \( Tr_2 \). The circuit now converts from a constant voltage source to a constant current source, and as a result any further decrease in load resistance results in a fall in the output voltage. This may be described as a constant current characteristic and is similar to that in Fig. 10.31. For example for a Zener voltage of 12 V, for a maximum current of 250 mA we have \( R_2 = 50 \times (12 - 0.7)/0.25A = 2.2k \) where \( h_{fe2} = 50 \) for \( Tr_2 \) is used.

![Transistor regulator with alternative electronic protection](image)

**Fig. 10.33** Transistor regulator with alternative electronic protection

Under short-circuit conditions, the maximum current \( I_{L(max)} \) continues to flow into through the short circuit. It is possible to reduce this short-circuit current by the introduction of another signal diode \( D_3 \) as shown in Fig. 10.34. When the maximum output current flows and the regulator is in the constant current mode, as load resistance
decreases, diode $D_2$ becomes reverse-biased, and the additional diode $D_3$ becomes forward-biased. This causes current to flow from resistor $R_1$ through $D_3$ into the load. This reduces the current into the Zener diode, thereby causing the Zener diode voltage to fall. The result is decrease in both the output voltage and load current. Under short-circuit conditions, the load current will be reduced to near zero with zero output voltage. This is the *fold-back* characteristic (Fig. 10.35).

*Fig. 10.34* Transistor regulator with enhanced electronic protection
A further improvement in the protection scheme is possible by the replacement of diode $D_3$ by another pnp transistor $Tr_3$ as shown in Fig. 10.36. When the maximum output current flows and the regulator is in the constant current mode, as load resistance decreases, diode $D_2$ becomes reverse-biased, and the base–emitter junction of $Tr_3$ becomes forward-biased. This causes current to flow from resistor $R_1$ into the emitter of $Tr_3$ and out through the collector into resistor $R_2$. This has two effects: (i) it reduces the current into the Zener diode, thereby causing the Zener diode voltage to fall, and (ii) it reduces the collector current through $Tr_1$ and hence the maximum current available from $Tr_2$. The result is a rapid switch off of the supply when the maximum load current is exceeded. This may be referred to as a switch-off characteristic. In order to reset the supply after the overload condition is removed, the connection from the collector of $Tr_3$ to $R_2$ must be interrupted. This can be done with a normally closed push-button switch in the collector circuit of $Tr_3$. 

![Fig. 10.35 Fold-back characteristic](image-url)
In the single transistor voltage regulator, while the output ripple is low, there are still variations in the output voltage arising from the $V_{BE}/I_C$ characteristic of the transistor. Thus, as load current increases, $V_{BE}$ increases, and hence $V_o = V_z - V_{BE}$ decreases. In order to reduce the magnitude of this change, feedback can be used to sense the change and effect a correction at the output. The basic elements of a series feedback regulator circuit are shown in Fig. 10.37. It consists of an error amplifier, a sampling circuit, a voltage reference and a series element. During operation, the sampling circuit $R_2R_1$ samples the regulator output voltage and sends it to the error amplifier. This amplifier compares the sample with a reference voltage and generates a signal proportional to the difference. This error signal is used to drive the series pass element, which varies the output voltage such that the error is reduced and the output voltage regulated.
Considering the basic feedback system, the voltage across the series element is \((V_i - V_o)\), while the input voltage to the error amplifier is \((\beta V_o - V_{REF})\) where

\[
\beta = \frac{R_1}{R_1 + R_2}
\]  

The output voltage across the series element may be viewed as an amplified version of the input voltage, i.e.,

\[
V_i - V_o = A (\beta V_o - V_{REF})
\]  

where \(A\) is the gain of the error amplifier. Consider changes in the input and output voltages resulting in

\[
\Delta V_i - \Delta V_o = A (\beta \Delta V_o - \Delta V_{REF})
\]  

Since \(V_{REF}\) is constant, then

\[
\Delta V_i = (1 + A\beta) \Delta V_o
\]  

\[
\Delta V_o = \Delta V_i / (1 + A\beta)
\]  

Hence,

\[
\frac{\Delta V_o}{\Delta V_i} = \frac{1}{1 + A\beta}
\]
which is the stability factor. The ripple voltage component of the output is also reduced by a factor \((1 + A\beta)\). It follows that the higher the loop gain \(A\beta\), the better the regulator performance.

### 10.7.4.1 Voltage Regulator Using Discrete Transistors

A transistor regulator circuit utilizing feedback is shown in Fig. 10.38. Transistor \(Tr_2\) is the series pass transistor, and transistor \(Tr_1\) is the error amplifier. The overall system operates according to the block diagram in Fig. 10.37. The regulator in Fig. 10.38 accepts an unregulated DC input voltage \(V_i\) and delivers a regulated DC output voltage \(V_o\). It operates by sampling the output voltage \(V_o\) via \(R_1\) and \(R_2\) and comparing the sampled voltage which appears at the base of \(Tr_1\) with a reference voltage \(V_Z\) set at the emitter of \(Tr_1\) by the Zener diode \(D\). The resulting error voltage across the base–emitter junction of \(Tr_1\) establishes a current in \(R_3\) that sets the output voltage \(V_o\). If \(V_o\) increases, the sampled voltage and hence the voltage at the base of \(Tr_2\) increase. Since the emitter voltage of \(Tr_1\) is held fixed by the Zener, the base–emitter voltage increases. This further turns on \(Tr_1\), increasing its collector current. The resulting increased voltage drop across \(R_3\) lowers the collector voltage of \(Tr_1\), which then lowers the output voltage \(V_o\) by the emitter follower action of \(Tr_2\). If the output voltage decreases, then the base–emitter voltage of \(Tr_1\) is reduced, thereby reducing its collector current. The voltage at the collector of \(Tr_1\) increases which then increases the output voltage \(V_o\). The capacitor \(C\) provides filtering action for the output of the associated rectifier.
Fig. 10.38  Regulator using discrete transistors

The design procedure involves first choosing a current to be passed into the Zener through \( R_4 \). Let this value be \( I_z \). Then \( R_4 \) must be calculated to enable this current to flow when \( V_i \) is at its minimum. Hence,

\[
R_4 = \frac{V_{i\text{min}} - V_z}{I_z}
\]

where \( V_{i\text{min}} = V_z \sqrt{2} - \Delta V \) and \( \Delta V \) is the peak-to-peak ripple voltage at the input to the regulator. Resistor \( R_3 \) is calculated by noting that it must supply collector current \( I_{C1} \) to \( Tr_1 \) as well as base current \( I_{B2} \) to \( Tr_2 \). It must do so under worst-case conditions, i.e., when \( V_i \) is a minimum and \( I_{B2} \) is a maximum. Noting that the voltage at the collector of \( Tr_1 \) is \( V_{out} + V_{BE} \), then

\[
R_3 = \frac{V_{i\text{min}} - (V_{out} + V_{BE})}{I_{B2}(\text{max}) + I_{C1}}
\]

where
In order to determine $R_1$ and $R_2$, we note that $V_B(Tr_1) = V_Z + V_{BE}$. Assuming that the base current of $Tr_1$ does not load the $R_2, R_1$ potential divider, it follows that

$$\frac{V_Z + V_{BE}}{R_1} = \frac{V_{out}}{R_2 + R_1}$$

(10.34)

giving

$$V_{out} = \left(1 + \frac{R_2}{R_1}\right)(V_Z + V_{BE})$$

(10.35)

To prevent loading, choose current $I(R_2, R_1)$ through $R_2$ and $R_1$ such that $I(R_2, R_1) \geq 10I_B(Tr_1)$.

**Example 10.15** Design a regulated supply using the topology in Fig. 10.38 rated at 9 V and 100 mA. Power for the regulator must come from an unregulated supply using a full-wave bridge rectifier and a 12-V transformer having a ripple voltage of 1 V peak-to-peak at maximum load current. Use transistors with current gain of 100.

**Solution** For $V_o = 9$, choose an intermediate value of Zener diode voltage of say 5.6 V (why?). Let the minimum current through the Zener be 5 mA for good Zener performance. Also, choose $I_{C1} = 1$ mA as a reasonable operating current for $Tr_1$. Hence,

$$R_4 = \frac{V_{i(min)}-V_z}{5 \text{ mA}} = \frac{12 \sqrt{2}-1-5.6}{5 \text{ mA}} = 2 \text{ k}.$$  

Also,

$$R_3 = \frac{V_{i(min)}-(9+0.7)}{I_L/ h_{fe} + I_C(Tr_1)} = \frac{12 \sqrt{2}-1-9.7}{100 \text{ mA}/100+1 \text{ mA}} = 3.2\text{k}.$$  

The current flowing through $R_2$ and $R_1$ must be at least ten times the base current of $Tr_2$. The base current $I_{B1}$ of $Tr_1$ is approximately $1 \text{ mA}/100 = 10 \mu\text{A}$. Hence,

$$f_D = 1 = \frac{1}{2\pi R_A(C_A + C_C)}, R_1 + R_2 \leq 90 \text{k}$$

and

$$V_o = (V_Z + 0.7)\left(1 + \frac{R_2}{R_1}\right)$$

and
Thus for $R_1 = 10 \, \text{k}\Omega$, $R_2 = 4.3 \, \text{k}\Omega$ and note that for these values $R_1 + R_2 \leq 90 \, \text{k}\Omega$ as required. Finally,

$$C = \frac{I_{L,\text{max}}}{120\Delta V} = \frac{100}{120 \times 1} = 833 \, \mu\text{F}.$$ 

There are several ways to improve the performance of this circuit. A great improvement can be realized by supplying the Zener from the regulated output instead of the unregulated input by connecting resistor $R_4$ to the regulated output. This reduces the ripple across the Zener diode and hence at the output. A second improvement is to place a capacitor across the Zener diode, again reducing the ripple. The value of this capacitor is that value that has an impedance comparable to or lower than the dynamic resistance of the Zener. A third method of performance improvement is to replace $R_4$ by a constant current source. An excellent method of implementing this scheme is the use of the constant current diode made using a JFET. This is a two-terminal device made, for example, by Siliconix that can simply replace the resistor feeding the Zener. Finally, a small capacitor placed across the circuit output removes output noise and reduces the supply impedance at high frequencies. In order to handle a large load current, a second transistor $Tr_3$ can be used along with $Tr_2$ in a Darlington arrangement as shown in Fig. 10.39. This reduces the pass transistor base current demand that may otherwise cause resistor $R_3$ to be too low in value and thereby result in too large a standing current in the error transistor $Tr_1$. The calculation would now involve the combined transistor current gain $h_{fe2} h_{fe3}$. Further ripple reduction can be achieved by applying bootstrapping to the load resistor $R_3$ of the error transistor $Tr_1$. This increases the error transistor gain which increases the applied feedback.
Example 10.16  Using the circuit shown in Fig. 10.39, design a + 20 V, 1.5 A regulator that is driven by an unregulated supply having 2V peak-peak input ripple. Use a 22 V transformer and a bridge rectifier to provide the unregulated input. Assume the power transistor has a gain of 25 and the other transistors have gains of 150. Justify all design steps.

Solution  Choose $V_Z = 10$ V for good feedback and reasonable value of $R_4$, i.e., not too low. Choose a Zener current for good Zener operation say 5 mA. The minimum unregulated input voltage is

$V_i \text{(min)} = 22 \sqrt{2} - 2 = 29.1$ V. Hence, $R_4 = \frac{20-10}{5 \text{ mA}} = \frac{10}{5 \text{ mA}} = 2$ kΩ.

Let $I_C(Tr_1) = 1$ mA for good transistor operation. Then,

$R_3 = \frac{29.1-(20+1.4)}{1.5 \text{ A}/(150\times25)+1 \text{ mA}} = \frac{7.7}{1.4 \text{ mA}} = 5.5$ kΩ. In order that the base of $Tr_1$ does not load the voltage divider $R_2, R_1$,

$\frac{V_o}{R_1+R_2} > 10 \times \frac{1 \text{ mA}}{150} \approx 66 \mu$A, i.e., $R_1 + R_2 < \frac{V_o}{66 \mu$A} = \frac{20}{66 \mu$A} \approx 300$ kΩ.

Now $\frac{V_Z+0.7}{R_1} = \frac{V_o}{R_1+R_2}$, i.e., $\frac{10.7}{R_1} = \frac{20}{R_1+R_2}$ from which $\frac{R_2}{R_1} = 0.87$. For $R_1 = 10$
$k, R_2 = 8.7 \text{k}$. Note $R_1 + R_2 < 300 \text{k}$. Since the unregulated input is from a full-wave rectifier, 
\[ C = \frac{I}{2\Delta V_f} = \frac{1.5}{2 \times 2 \times 60} = 6250 \ \mu\text{F}. \]

**Example 10.17** Introduce bootstrapping of resistor $R_3$ in Example 10.16, and add a suitable filter capacitor across the Zener diode as shown in Fig. 10.40.

![Fig. 10.40](image)

**Solution** In order to apply bootstrapping to $R_3$, this resistor is split into two resistors. The exact values are not critical, and they can be made equal. Hence, $R_3$ is split into $R_{3a} = 2.2 \text{k}$ and $R_{3b} = 2.2 \text{k}$. A capacitor $C_3$ is chosen to have a value such that its reactance at the ripple frequency is lower than $R_{3a}$. Hence, 
\[ C_3 = \frac{1}{(2\pi f R_{3a})} = \frac{1}{(2 \times \pi \times 120 \times 2.2 \times 10^3)} = 0.6 \ \mu\text{F}. \]

A value of 10 $\mu$F is chosen. Choose $C_2 = 100 \ \mu\text{F}$ with a reactance of 13 $\Omega$ at 120 Hz.

A particularly useful version of this transistor series regulator that can be adapted to a wide range of output voltages and currents is shown in Fig. 10.41. The Zener diode is moved from between the emitter of $Tr_1$
and ground and connected between the base of \( Tr_1 \) and the regulated output. Resistor \( R_1 \) across the base–emitter junction of \( Tr_1 \) establishes a near constant current in the Zener diode of \( 0.7/R_1 \). The output voltage is \( V_o = (V_Z + 0.7) \), and this arrangement constitutes 100% negative feedback as compared with the original system. As before, \( Tr_2 \) could be either a single transistor or a Darlington pair for higher currents. Resistor \( R_2 \) provides protection for \( Tr_1 \) in the event of component failure. The application of bootstrapping to resistor \( R_3 \) will increase the amount of available feedback and hence improve the performance of the power supply.

![Diagram](image)

**Fig. 10.41** Alternative transistor feedback regulator

**Example 10.18** Using the configuration in Fig. 10.41, design a + 15 V, 100 mA regulator that is driven by an unregulated supply having 1.5-V peak-peak input ripple. Use a 20-V transformer and a half-wave rectifier to provide the unregulated input.

**Solution** For \( V_o = 16 \) V, choose a value of Zener diode with a voltage that is close to the desired voltage. Thus, a diode with \( V_Z = 15 \) V will result in a regulator voltage of 15.7 V. Let the minimum current through the Zener be 5 mA for good Zener performance. Then \( R_1 = 0.7/5 \) mA = 140 \( \Omega \). Also, choose \( I_{C1} = 1 \) mA as a reasonable operating current.
Hence, 
\[ R_3 = \frac{V_f\text{(min)} - (15 + 0.7)}{I_L / h_{fe} + I_C(T_{r1})} = \frac{20 \sqrt{2} - 1.5 - 15.7}{100 \text{ mA} / 100 + 1 \text{ mA}} = 5k5. \]

In order to provide some protection to \( T_{r1} \), let \( R_2 = 47 \Omega \). Finally, 
\[ C_1 = \frac{I_{L\text{max}}}{60\Delta V} = \frac{100 \text{ mA}}{60 \times 1.5} = 1111 \text{ } \mu\text{F}. \] Capacitor \( C_2 = 1 \mu\text{F} \) provides further filtering of the regulated output voltage.

**Example 10.19**  Introduce bootstrapping of resistor \( R_3 \) in Example 10.18.

**Solution**  In order to apply bootstrapping to \( R_3 \), this resistor is split into two resistors as shown in Fig. 10.42. The exact values are not critical and equal values will do. Hence, \( R_3 \) is split into \( R_{3a} = 2.2 \text{ k} \) and \( R_{3b} = 2.2 \text{ k} \). A capacitor \( C_3 \) is chosen to have a value such that its reactance at the ripple frequency is lower than \( R_{3b} \). Hence, 
\[ C_3 = \frac{1}{(2\pi f R_{3a})} = \frac{1}{(2 \times \pi \times 60 \times 2.2 \times 10^3)} = 1.2 \text{ } \mu\text{F}. \] A value of 10 \( \mu\text{F} \) is chosen.

**Fig. 10.42**  Alternative feedback regulator with bootstrapping

**Example 10.20**  Using the basic configuration in Fig. 10.41, design a +12 V, 5 A regulator that is driven by an unregulated supply having 5V
peak-peak input ripple. Use an 18 V transformer and a full-wave rectifier to provide the unregulated input.

**Solution**  Because of the large current requirement, a power Darlington such as the MJ3000 having $\beta = 1000$ is used. For $V_o = 12$ V, choose a value of Zener diode with a voltage that is close to the desired voltage. Thus, a diode with $V_Z = 11$ V will result in a regulator voltage of 11.7 V. Let the minimum current through the Zener be 5 mA for good Zener performance. Then $R_1 = 0.7/5$ mA = 140 $\Omega$. Also, choose $I_{C1} = 1$ mA as a reasonable operating current. Hence,

$$R_3 = \frac{V_i(\text{min})-(11+0.7)}{I_t/hfe+I_C(Tr_1)} = \frac{18\sqrt{2}-2-11.7}{(5/10^3)\times10^3 \text{ mA}+1 \text{ mA}} = 2 \text{ k}$$.  

In order to provide some protection to $Tr_1$, let $R_2 = 47 \Omega$. Finally,

$$C_1 = \frac{I_{t,\text{max}}}{2\times60\Delta V} = \frac{5 \text{ A}}{2\times60\times5} = 8,333 \mu\text{F}$$. Capacitor $C_2 = 1 \mu\text{F}$ provides further filtering of the regulated output voltage. The circuit is shown in Fig. 10.43.

**Fig. 10.43** Transistor voltage regulator for Example 10.20

### 10.7.4.2 Op-Amp Series Regulator

In order to further improve the regulator performance, the loop gain $A\beta$ needs to be increased. A simple method of doing this is to replace the transistor error amplifier by an operational amplifier which has a much
higher open-loop gain. This is shown in Fig. 10.44. The operational amplifier compares the reference voltage of the Zener with the feedback voltage sampled by resistors $R_1$ and $R_2$. Using basic op-amp theory,

$$V_o = V_Z \left(1 + \frac{R_2}{R_1}\right)$$  \hspace{1cm} (10.36)

![Op-amp series regulator](image)

**Fig. 10.44** Op-amp series regulator

Note that the op-amp must be supplied from the unregulated supply. (Why?) Similar to the improved transistor case, the circuit can be improved by supplying the Zener diode from the regulated output (Fig. 10.45). All the other improvement techniques (except bootstrapping) are applicable here. The current limiting techniques are also applicable.
**Example 10.21** Using the circuit shown in Fig. 10.46, design a +15 V, 2 A regulator that is driven by an unregulated supply having 2 V peak-peak input ripple. Use a 20 V transformer and a full-wave rectifier to provide the unregulated input. Assume the power transistor has a gain of 150.

![Fig. 10.46 Op-amp voltage regulator with Darlington pair](image)

**Solution** Choose \( V_Z = 7.5 \) V. Set \( I_Z = 5 \) mA for good Zener operation. Hence, \( R_3 = (15 - 7.5)/5 \) mA = 1.5 kΩ. From (10.36),

\[
7.5 \left( 1 + \frac{R_2}{R_1} \right) = 15
\]

Hence, \( R_1 = 10 \) kΩ = \( R_2 \). \( C = \frac{I}{2f\Delta V} = \frac{2A}{2 \times 60 \times 3} = 5.555 \) µF.

**10.7.4.3 Variable Output Voltage**

The basic feedback voltage regulator can be modified to produce a variable output voltage. In such a situation since the regulated output will now be variable, the Zener diode which provides the reference voltage will have to be supplied from the unregulated input voltage and not the regulated output if its current supply is to be maintained.

In the case of the transistor feedback regulator, one approach is shown in Fig. 10.47. Here the Zener diode is supplied from the unregulated voltage through a constant current diode to minimize ripple across the Zener diode. Additionally, a large filter capacitor is placed in
parallel with the Zener diode to further reduce ripple. The variable output voltage is produced by varying the feedback through adjustment of $VR_1$ in Fig. 10.47 which replaced feedback resistor $R_2$.

![Variable transistor voltage regulator](image)

**Fig. 10.47** Variable transistor voltage regulator

The minimum voltage is $V_Z$, while the maximum voltage must be at least three volts less than the minimum unregulated voltage in order to ensure that the pass transistor is properly biased. Thus,

$$(V_Z + V_{BE})(1 + \frac{VR_1}{R_1}) = (V_{min}(unreg) - 3)$$

is the design equation.

With respect to the op-amp feedback regulator, one simple approach to achieving variable regulated voltage is shown in Fig. 10.48. Here again the Zener diode is supplied from the unregulated voltage through a constant current diode to minimize ripple, and a large filter capacitor $C_1$ is placed in parallel with the Zener diode. The variable output voltage is produced by varying the reference voltage through adjustment of $VR_1$ in Fig. 10.48. This approach has the advantage that the feedback around the system is unaltered, thereby maintaining the system characteristics as the voltage is varied. It is important to note that the output of this system cannot go to zero because of saturation voltage loss within the op-amp. Once again, the maximum voltage must be set at about 3 V below the minimum unregulated voltage.
**10.7.5 Protection Circuits**

In this linear regulator, if the output is short circuited to ground, the pass transistor will be immediately destroyed by excessive current flow. Various protection schemes can be used to prevent this. One circuit that can be used is a current limiting circuit shown in Fig. 10.49. Transistor $Tr_3$ and $R_5$ are introduced such that the load current flows through $R_5$ and thereby develops a voltage across the base–emitter junction of $Tr_3$. For a sufficiently large load current this voltage exceeds the turn-on voltage of the transistor (0.7 V). $Tr_3$ therefore turns on and diverts base current away from the base of $Tr_1$, thereby limiting the load current. The design equations are simple: Let the maximum load current be $I_{L(max)}$. Then at turn on $I_{L(max)}R_5 = 0.7$ V giving

$$R_5 = \frac{0.7}{I_{L(max)}}$$  \hspace{1cm} (10.37)
This current limiting circuit at switch-on converts the regulator from a constant voltage output to a constant current output as shown in Fig. 10.50. Hence during its operation, as the external load resistance $R_L$ decreases, the constant current $I_{L(max)}$ develops a voltage across $R_L$ given by

$$V_o = I_{L(max)} R_L$$  \hspace{1cm} (10.38)
Therefore, as $R_L$ goes to zero, so does the output voltage.

For the circuit in Fig. 10.49 in the presence of a short circuit, a significant current $I_{L(max)}$ flows into a short circuit. This can result in heating from residual circuit resistance. It is therefore desirable that the load current $I_{L(max)}$ be also reduced. In the fold-back limiting circuit shown in Fig. 10.51, reduction of both the output voltage and load current in an overload condition is achieved. The fold-back action shown in Fig. 10.52 is introduced by the potential divider $R_6$ and $R_7$. The base of $Tr_3$ is connected to the junction of these resistors. Transistor $Tr_3$ is turned on when the voltage $V_x$ at the base of $Tr_3$ is 0.7 V higher than the output voltage $V_o$. Initially, with no load current $I_L$, $V_y$ is equal to $V_o$, and $V_x$ is lower than $V_y$ making $V_x$ less than $V_o$. $Tr_3$ is therefore off. As the load current increases, $V_y = V_o + I_L R_5$ increases, and hence $V_x$ also increases. Eventually when $V_x - V_o = 0.7 V$, $Tr_3$ turns on, thereby diverting current from $Tr_1$ and hence limiting $I_L$. The circuit is now in the constant current mode. As the load resistor $R_L$ is reduced further, $V_o$ decreases. But because of the potential divider $R_6$ and $R_7$, $V_x$ decreases by a smaller amount, and therefore to maintain $V_x - V_o = 0.7$, $I_L R_5$ must decrease, i.e., $I_L$ must fall. The design equations are the following: At turn-on,

$$0.7 = V_x - V_o = V_y - V_o = \rho (V_o + I_L R_5) - V_o$$  \hspace{1cm} (10.39)

where

$$\beta = \frac{R_1}{R_1 + R_2}$$  \hspace{1cm} (10.40)
Fig. 10.51 Transistor regulator with fold-back protection

Fig. 10.52 Fold-back characteristic

This gives

\[ 0.7 = (\rho - 1) V_o + \rho I_L R_5 \]  \hspace{1cm} (10.41)

Suppose \( V_o = 12 \text{ V} \) and \( I_L(\text{max}) = 1 \text{ A} \); then for \( R_5 = 1 \Omega \),
\[ \rho = \frac{0.7 + 12}{12 + 1} = \frac{12.7}{13} = 0.9692. \] For \( R_L = 0, \ V_o = 0 \) and hence
From this, \( R_7 = 10 \text{k}\Omega \) and \( R_6 = 317 \Omega \).

Protection for the op-amp regulator follows similar principles as seen in Fig. 10.53. Here transistor \( Tr_2 \) is used to introduce electronic short-circuit protection as in the discrete transistor case. When load current flows such that the voltage drop across \( R_4 \) equals 0.7 V, then \( Tr_2 \) turns on and draws current away from the pass transistor \( Tr_1 \), thereby limiting the load current drawn from the supply. Resistor \( R_5 \) ensures that the output voltage of the op-amp decreases as current through \( Tr_2 \) increases, thereby reducing the output voltage of the regulated supply.

![Opamp regulator with electronic protection](image)

**Fig. 10.53** Op-amp regulator with electronic protection

### 10.7.6 IC Voltage Regulators

Instead of building regulators using transistors and operational amplifiers, IC voltage regulators that greatly simplify the process are available. These ICs contain all the elements of the basic block including reference voltage, error amplifier, series pass device and overload protection circuitry. They provide excellent voltage regulation in three basic formats, fixed positive voltage, fixed negative voltage, and adjustable output voltages. The overall power supply consists of an unregulated supply providing the input voltage to the IC regulator. A wide range of output voltages and currents are available. The design of a fully regulated power supply using an IC regulator is quite straightforward.
### 10.7.6.1 Three-Terminal Voltage Regulator
The simplest of the IC regulators is probably the three-terminal device shown in Fig. 10.54. An unregulated voltage is supplied to the input terminal, a regulated output is available at the output terminal, and the third terminal is grounded. Both positive and negative voltage devices are available.

![Three-terminal IC regulator](image)

**Fig. 10.54** Three-terminal IC regulator

### 10.7.6.2 Fixed Positive Voltage Regulators
Fixed positive voltages are available in the 7800 series of regulators. The voltages range from 5 to 24 V as shown in Table 10.1. As an example, the 7815 IC regulator is shown in Fig. 10.55. The output voltage is +15 V. A positive rectified input voltage is supplied at $V_i$ with capacitor $C_1$ providing filtering (reservoir capacitor). The output is filtered by capacitor $C_2$ which is a smaller capacitor, designed to remove mostly high-frequency noise. The ground terminal is connected to ground. If the supply transformer has an output voltage of $V_s$ rms, then the peak voltage into the regulator is $\sqrt{2}V_s$, and the minimum voltage is

$$V_{mn} = \sqrt{2}V_s - \Delta V$$

where $\Delta V$ is the peak-to-peak ripple.

**Table 10.1** 7800 series positive voltage regulators

<table>
<thead>
<tr>
<th>IC</th>
<th>Output voltage (V)</th>
<th>Minimum input voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>7805</td>
<td>+5</td>
<td>7.3</td>
</tr>
</tbody>
</table>
Based on the maximum load current $I_{L_{\text{max}}}$, the reservoir capacitor $C_1$ is given by

$$C_1 = \frac{I_{L_{\text{max}}}}{2f\Delta V} \quad (10.42)$$

Note that the minimum value of the unregulated input voltage must exceed the minimum input voltage specification for the regulator. Some specifications include the following:

Output Voltage: Regulated Output Voltage
Line Regulation: Typically, 0.1%
Load Regulation: Typically, 0.1%
Current Limit: The maximum current that flows at the output of the regulator into a short circuit.

---

**Fig. 10.55** Three-terminal positive fixed voltage regulator

<table>
<thead>
<tr>
<th>IC</th>
<th>Output voltage (V)</th>
<th>Minimum input voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>7806</td>
<td>+6</td>
<td>8.3</td>
</tr>
<tr>
<td>7808</td>
<td>+8</td>
<td>10.5</td>
</tr>
<tr>
<td>7810</td>
<td>+10</td>
<td>12.5</td>
</tr>
<tr>
<td>7812</td>
<td>+12</td>
<td>14.6</td>
</tr>
<tr>
<td>7815</td>
<td>+15</td>
<td>17.7</td>
</tr>
<tr>
<td>7818</td>
<td>+18</td>
<td>21.0</td>
</tr>
<tr>
<td>7824</td>
<td>+24</td>
<td>27.1</td>
</tr>
</tbody>
</table>
Drop Out Voltage: This is the minimum voltage across the input and output terminal of the regulator that must be maintained if regulating action is to be sustained.
Ripple-Rejection Ratio: Ratio in dB of input ripple to output ripple.
Output Resistance: The DC output resistance of the regulator.

10.7.6.3 Fixed Negative Voltage Regulators
Similar to the 7800 series positive voltage regulators, the 7900 series provides negative regulated voltages. Similar specifications apply with the list of available voltages shown in Table 10.2. The connection of a – 5 V regulator is shown in Fig. 10.56.

Table 10.2 7900 series negative voltage regulators

<table>
<thead>
<tr>
<th>IC No.</th>
<th>Output voltage (V)</th>
<th>Minimum input voltage (V_i)</th>
</tr>
</thead>
<tbody>
<tr>
<td>7905</td>
<td>-5</td>
<td>-7.3</td>
</tr>
<tr>
<td>7906</td>
<td>-6</td>
<td>-8.4</td>
</tr>
<tr>
<td>7908</td>
<td>-8</td>
<td>-10.5</td>
</tr>
<tr>
<td>7909</td>
<td>-9</td>
<td>-11.5</td>
</tr>
<tr>
<td>7912</td>
<td>-12</td>
<td>-14.6</td>
</tr>
<tr>
<td>7915</td>
<td>-15</td>
<td>-17.7</td>
</tr>
<tr>
<td>7918</td>
<td>-18</td>
<td>-20.8</td>
</tr>
<tr>
<td>7924</td>
<td>-24</td>
<td>-27.1</td>
</tr>
</tbody>
</table>

Fig. 10.56 Three-terminal negative fixed voltage regulator
10.7.6.4 Adjustable Voltage Regulators

Adjustable voltage regulators allow the user to change the output voltage of the regulator to a desired level. The LM317 is an example of such a regulator. The circuit connection is shown in Fig. 10.57. The output voltage $V_o$ is given by

$$V_o = V_{ref} \left(1 + \frac{R_2}{R_1}\right) + I_{adj}R_2$$  \hspace{1cm} (10.43)

where $R_1 = 240 \, \Omega$ and $R_2 = 5 \, k$ is a potentiometer. Typical values are $V_{ref} = 1.25 \, V$ and $I_{adj} = 100 \, \mu A$. With these values, the output voltage can be adjusted over the range 1.25 V when $R_2 = 0$ to about 27 V when $R_2 = 5$ k. Capacitor $C_1 = 0.1 \, \mu F$ works in conjunction with the main power supply filter capacitor to provide improved filtering.

![Fig. 10.57 Adjustable IC voltage regulator](image)

The corresponding adjustable negative regulator is the LM337. These devices are able to provide output current of up to 1.5 A with an adjustable voltage range from 1.25 to 37 V. For the safe operation of this regulator protection diodes are required and the reader is referred to the device datasheet. A typical application for a supply that can be
varied from 1.25 to 14 V is shown in Fig. 10.58. Here $R_1 = 240 \, \Omega$ and $R_2 = 2.5 \, k$ is a potentiometer. Capacitor $C_2 = 10 \, \mu F$ improves ripple rejection. Capacitor $C_3 = 1 \, \mu F$ improves transient response of the supply. Diodes $D_1$ and $D_2$ provide protection to the IC against capacitor discharge.

Example 10.22    Design a variable voltage regulated power supply using the LM1084 adjustable regulator IC.

Solution    The LM1084 regulator IC is a low drop-out voltage regulator that can deliver 5 A at a positive voltage. It has the same pin-out configuration as the LM317. It is available with fixed output voltages of 3.3, 5.0, and 12.0 V as well as variable output. The device is current limited and thermally protected and can deliver 5 A at a line regulation of 0.015% and line regulation of 0.1%. A typical application as a variable voltage regulator is shown in Fig. 10.59. For this circuit the output voltage is given by $V_{DC} = 1.25 \left(1 + \frac{R_2}{R_1}\right)$. The unregulated part of the supply follows the established design procedure. It utilizes a BR34 bridge rectifier which contains four diodes with PIV of 400 V and current rating 3A. Resistor $R_1$ is set at 220 \, \Omega and $R_2$ is a potentiometer. Using $R_2 = 2.5 \, k$, then the output voltage varies from 1.25 V to
\[ V_{DC} = 1.25 \left(1 + \frac{2500}{220}\right) = 15.5 \text{ V} \]. Resistor \( R_3 = 1.5 \text{ k} \) and the red LED provide indication that the supply is on and also enable discharge of capacitor \( C_1 = 3300 \mu\text{F} \) when the supply is turned off. A small capacitor \( C_2 = 10 \mu\text{F} \) at the output removes any high-frequency noise from the supply.

Fig. 10.59  Variable regulator using the LM1084 IC

The corresponding negative voltage regulator using the LM337 regulator IC is shown in Fig. 10.60.

Fig. 10.60  Adjustable negative voltage regulated power supply using the LM337 IC regulator

10.7.7  Simple Approach to Regulated Power Supplies
The TL431A integrated circuit is a three-terminal device that operates essentially as a programmable Zener diode whose effective voltage $V_Z$ can be varied from 2.5 to 36 V using two external resistors $R_1$ and $R_2$ as shown in Fig. 1.70 of Chap. 1. The Zener voltage is determined by $V_Z = \left(1 + \frac{R_1}{R_2}\right)V_{ref}$ where $V_{ref} = 2.5$ V. The Zener current range is 1–100 mA, the typical dynamic resistance is 0.22 Ω, and the temperature coefficient is a low 0.4% at room temperature. It was used in Chap. 1 in Zener-regulated power supplies. The versatility of the TL431A is based on it containing both a variable reference voltage and an error amplifier that enables the application of corrective feedback. In this application, its performance is enhanced by the introduction of a pass transistor $Tr_1$ (Darlington) to boost the current capacity, thereby implementing the basic series regulator of Fig. 10.37. The simple system is shown in Fig. 10.61 where the transistor is within the feedback loop of the TL431A and therefore the output voltage is given by $V_o = \left(1 + \frac{R_2}{R_1}\right)2.5$ V.

Resistor $R_2 = R_{2a} + VR$ comprises fixed resistor $R_{2a}$ and variable resistor $VR$, thereby allowing easy variation of the output voltage. It can be adapted to a wide range of applications and power supply requirements at a very low cost.

![Fig. 10.61 Simple regulated power supply](image)
Example 10.23  Using the configuration in Fig. 10.61 and a bridge rectifier, design a regulated supply delivering 20 V at a current of 2 A.

Solution  A 24-V transformer is used to ensure adequate voltage drop across the pass transistor. Allowing a 2 V drop in the voltage across the reservoir capacitor \( C_1 \), the capacitor value is given by

\[
C_1 = \frac{2A}{(2 \times 2 \times 60)} = 8333 \mu F.
\]

The MJ3001 Darlington pair has a current gain of 1000. Hence for a maximum current of 2 A, the base current is \( 2A/1000 = 2 \) mA. The minimum value of the input voltage is 

\[
24\sqrt{2} - 2 = 32 \text{ V}.
\]

Allowing a current of 10 mA into the TL431A Zener gives \( R_3 = (32 - 20)/10 \text{ mA} = 1.2 \) k. For a 20V output, 

\[
20 = (1 + R_2/R_1) \times 2.5.
\]

Using \( R_1 = 2 \) k, then \( R_2 = 14 \) k. Capacitor \( C_2 = 100 \mu F \) reduces ripple across the Zener, and \( C_3 = 1 \mu F \) removes any high-frequency noise and residual ripple.

10.8 Applications

In this section, several regulated power supply designs are presented.

10.8.1 Variable Voltage Regulated Supply

We here explore the design of a variable voltage regulated power supply using the basic op-amp configuration of Fig. 10.44. The system must be adjustable down to zero and up to about 15 V and must have adjustable current limiting from about 100 mA to 1 A. In order to secure a 15V output from a regulator, a 30V center-tapped transformer rated at twice the required current is used. This would enable the design of a full-wave rectifier using two rectifying diodes that provides sufficient voltage to ensure pass transistor operation. One system topology is shown in Fig. 10.62. In order to achieve variable output, the Zener diode \( D_4 \) is supplied from the unregulated input through a constant current diode \( D_6 \) for improved ripple reduction. The Zener voltage supplies a potentiometer \( VR_1 \) which in turn supplies a variable reference voltage to the reference input of the op-amp. In order that zero output voltage be possible, the negative supply terminal of the op-amp cannot go to zero (why?) but must be taken to a negative voltage. A negative voltage of \(-6.8 \) V is
furnished by Zener diode $D_5$ which is powered via $R_3$ by the half-wave rectifier $D_3 - C_2$. The total voltage between the power supply terminals of the op-amp is $15 \sqrt{2} + 6.8 = 28 \text{ V}$ which is less than the maximum rated supply voltage of $2 \times 22 = 44 \text{ V}$ for the LM741. A Darlington pair comprising $Tr_1$ and $Tr_2$ is used and can be made up using a 2N3053 and a 2N3055, respectively, or a MJ3000 power Darlington. Potentiometer $VR_2$ permits variation of the current limit. $Tr_3$ can be a small-signal transistor 2N3904. Rectifying diodes $D_1$ and $D_2$ must have PIV ratings of better than $2 \times 15 \times \sqrt{2} = 42 \text{ V}$ and current rating higher than 1 A.

The 1N5401 diode is rated at 100 V and 3 A and can be used. Since $I = 1 \text{ A}$ and $f = 60 \text{ Hz}$, in order to realize a peak-to-peak ripple voltage of about 2.5 V, capacitor $C_1$ must be $C_1 = \frac{I}{2f \Delta V} = \frac{1}{2 \times 60 \times 2.5} = 3333 \mu \text{F}$. The negative supply to the op-amp must deliver at least 2 mA to the op-amp. Hence using $I = 0.002 \text{ A}$ and $f = 60 \text{ Hz}$, in order to realize a pk-to-pk ripple voltage of about 2.5 V, capacitor $C_2$ must be $V_{B1} = \frac{47}{153+47} \times 20 = 4.7 \text{ V}$. Use $C_2 = 100 \mu \text{F}$. Diode $D_3$ can be an 1N4002 with PIV = 100 V and current rating of 1 A. Resistor $R_3$ must supply the Zener and the op-amp with current. Allowing 10 mA through $D_5$ in order to accomplish this, then $R_3 = \left(15 \sqrt{2} - 6.8\right)/10 \text{ mA} = 1.4 \text{ k}$. A 5.6 V Zener is used for the reference Zener $D_4$. This value will be amplified by the op-amp to produce the desired output voltage. $VR_1$ is a 10 k potentiometer to provide the voltage variation. Capacitor $C_3$ should have a reactance that is comparable to the dynamic resistance of the Zener which is of the order of tens of ohms. A 10 \mu F capacitor has a reactance at $f = 120 \text{ Hz}$ of $1/2\pi 120 \times 10 = 133 \Omega$ which is acceptable. The constant current diode $D_6$ is a Siliconix J509 which supplies about 3 mA to $D_4$. The high impedance of $D_6$ and the low impedance of $D_4$ in parallel with $C_3$ ensure that the ripple content at the noninverting input at the op-amp is very low. A choice of $R_1 = 10 \text{ k}$ and $R_2 = 18 \text{ k}$ means that the
maximum output of the system is \( 5.6 \left(1 + \frac{18}{10}\right) = 15.7 \) V just above the desired output voltage level of 15. Resistor \( R_5 \) sets the maximum current of say 1.1 A and is given by \( R_5 = 0.7/1.1 \) A = 0.6 \( \Omega \). The 10-\( \Omega \) potentiometer \( VR_2 \) allows variation of the current limit to a minimum value of \( I_{\text{min}} = 0.7/10.6 = 66 \) mA. The resistor \( R_4 = 330 \) \( \Omega \) assists in lowering the output voltage during a current overload condition. Finally, capacitor \( C_4 = 0.01 \mu\text{F} \) is intended to reduce high-frequency noise at the output of the power supply.

Fig. 10.62 Variable voltage regulated power supply

Ideas for Exploration: (i) Re-design the system to deliver a higher voltage using the OPA452 (80 V, 50 mA) operational amplifier to replace the LM741. (ii) Utilize the LM338A regulator IC in the design of a variable regulated power supply.

10.8.2 Variable Power Supply with Zener Stabilization
This regulated supply utilizing a 741 op-amp includes variable output voltage from 5 to 20 V at 1 A while supplying the Zener from the regulated output. This is achieved by varying the resistance supplying the 3.9-V Zener while also varying the applied feedback. The circuit is shown in Fig. 10.63. The essence of the approach is to vary both the amount of feedback and the value of the resistor supplying the Zener. This latter action will ensure that as the output voltage changes, the
current through the Zener will remain approximately constant. Because of the saturation loss of the op-amp, the output is not allowed to fall below 5 V. With an input unregulated voltage of 30 V, the maximum voltage is 20 V. The output of the Zener is passed through a low-pass filter \( R_4 - C_2 \) to reduce any noise, and a capacitor \( C_3 \) is implemented across the output also for purposes of filtering. Both can be about 10 µF. A Darlington pair comprising a 2N3053 medium power transistor and a 2N3055 power transistor or an MJ3000 is used as the series device.

**Fig. 10.63** Variable power supply with Zener stabilization

_Ideas for Exploration:_ (i) Re-design the system to deliver a higher voltage using the OPA452 (80 V, 50 mA) operational amplifier to replace the 741.

### 10.8.3 Discrete Voltage Regulator

This Zener diode regulator in Fig. 10.64 enhanced by an emitter follower enables the adjustment of the Zener voltage to compensate for the voltage drop caused by emitter follower action. The follower is really a feedback pair with modest gain where the second transistor is a pnp Darlington pair such as the MJ2501. Thus, with a 15 V Zener, the voltage that would be available at the output of \( Tr_2 \) would be 14.3 V because of the \( V_{BE} \) drop. Thus if \( R_1 = 12 \, k \) and \( R_2 = 600 \, \Omega \), then

\[
V_o = (1 + 600/12000) \times 14.3 = 15 \, V
\]

The JFET is connected as a constant
current diode supplying the Zener diode. Capacitor $C_1 = 10 \, \mu\text{F}$ provides filtering for the Zener.

![Discrete voltage regulator](image)

**Fig. 10.64** Discrete voltage regulator

**Ideas for Exploration:** (i) Re-design the system to provide a negative voltage with respect to ground. (ii) Explore the introduction of short-circuit protection.

### 10.8.4 Bipolar Zener

The circuit in Fig. 10.65 is essentially two complimentary feedback pairs connected as $V_{BE}$ multipliers with voltage adjustment by a single resistor. Since variable resistor $R_v$ is across the base–emitter junctions of $Tr_1$ and $Tr_2$, it follows that the current $I$ through $R_v$ is $I = \frac{1.4V}{R_v}$.

Therefore, the positive Zener voltage with respect to the zero potential is $V_Z = IR_1 + 0.7 = 1.4R_1/R_v + 0.7$, and the negative Zener voltage with respect to the zero reference is $-V_Z = -(IR_1 + 0.7) = -(1.4R_1/R_v + 0.7)$. Thus, a symmetrical supply is available with easy adjustment using $R_v$. Variable resistor $R_v$ should comprise a variable component $R_{V_0}$ and a
fixed component $R_b$ such that $R_V$ has a minimum value $R_V = R_b$. For example, let $R_1 = 6.8 \, k$, $R_{Vd} = 10 \, k$ and $R_b = 1 \, k$. Then noting that $R_{V_{\text{max}}} = (10 \, k + 1 \, k) = 11 \, k$ and $R_{V_{\text{min}}} = 1 \, k$, then $V_{Z_{\text{min}}} = (1.4 \times 6.8 \, k/11 \, k) + 0.7 = 1.6 \, V$ and $V_{Z_{\text{max}}} = (1.4 \times 6.8 \, k/1 \, k) + 0.7 = 10.2 \, V$. This means that the bipolar Zener voltages are variable from $\pm 1.6 \, V$ to $\pm 10.2 \, V$ using $R_V$.

![Bipolar Zener Circuit](image)

**Fig. 10.65** Bipolar Zener

*Ideas for Exploration*: (i) Use this configuration to design an adjustable Zener-regulated bipolar power supply.

### 10.8.5 Simple Feedback Power Supply
This feedback regulator delivers 6 V at 100 mA from a 12 V supply. It does not use a reference voltage Zener but instead uses the error transistor base–emitter junction as the reference voltage. The circuit is shown in Fig. 10.66. The defining equation is \( \frac{0.7}{R_1} = \frac{V_o}{R_1 + R_2} \) where \( V_o \) is the regulated output voltage and \( R_1 = R_{1a} + VR_1 \). For \( V_o = 6 \) V, if \( R_2 = 4.7 \) k then \( R_1 = 620 \) Ω. A good approach is to set \( R_{1a} = 470 \) Ω and potentiometer \( VR_1 = 1 \) k in series with \( R_{1a} \) in order to adjust the output voltage to the desired voltage. A load current of 100 mA produces a base current requirement in \( Tr_1 \) of 100 mA/50 = 2 mA where \( \beta = 50 \) is used. With a collector current in \( Tr_2 \) of 2 mA, then \( R_3 = (12 - 6 - 0.7)/(2 \) mA + 2 mA) = 1.3 k. This circuit can be adapted to accommodate other unregulated input voltages for a variety of applications. If an unregulated supply is used, \( R_3 \) can be bootstrapped to realize a higher gain in \( Tr_2 \) and therefore greater ripple-reducing feedback. \( R_4 = 1 \) k provides about 5 mA to the LED to indicate the on-condition.

**Fig. 10.66** Simple feedback power supply

*Ideas for Exploration:* (i) Add electronic protection to this circuit. (ii) Use this configuration to design an adjustable Zener-regulated bipolar power supply. (iii) Use a 20V transformer and an unregulated half-wave
rectifier to supply the circuit. (iv) Replace $Tr_1$ by a Darlington pair so that the base current for $Tr_1$ required from $R_3$ is reduced.

10.8.6 High-Current Variable Power Supply Using OPA549 Power Op-Amp

The OPA549 is a high-voltage, high-current operational amplifier that can be used as a variable regulated power supply. It is simply connected as an amplifier with a gain of 10 with DC at the input and the amplified DC at the output. The op-amp is powered from a 30 V unregulated supply. This is shown in Fig. 10.67, where a variable DC voltage of 0.1 V to 2.5 V at the non-inverting input results in a regulated output of 1 V to 25 V at a maximum current of 8 A. Current limit is set by resistor $R_{CL} = \left( \frac{75}{I_{LM}} - 7.5 \right)$ kΩ where $I_{LM}$ is the current limit in amperes. For example, for a current limit of 3 A, $R_{CL} = \left( \frac{75}{3} - 7.5 \right) k = 17.5 k$.

![Regulated power supply using OPA549 power op-amp](image)

Fig. 10.67 Regulated power supply using OPA549 power op-amp

Idea for Exploration: (i) Re-design the system to deliver a negative voltage relative to ground.
10.8.7 Dual Tracking Power Supply

This project involves the design of the dual tracking power supply shown in Fig. 10.68. It has one positive and one negative output of equal voltage. The positive voltage is adjustable from 0 to 20 V, and the negative supply automatically tracks the positive voltage. The supply can deliver up to 1 A. The basic system for each voltage polarity is essentially the op-amp system discussed earlier in this chapter with certain modifications. A 24V transformer is used to supply each regulator. A low-cost high-voltage replacement for the 741 op-amp is used: It is the OPA452. This op-amp operates from up to ±40 V, can deliver 50 mA, has a GBP of 1.8 MHz and is unity-gain stable. The pass transistors are MJ3001 and MJ2501 complementary power Darlington which are 80 V, 10 A, 150 W devices with $\beta = 1000$. These ensure that the current drawn from each op-amp is no more than $1 \text{A}/1000 = 1 \text{mA}$. The feedback components $R_2 = 15 \text{k}$ and $R_1 = 5.1 \text{k}$ for the positive regulator set the gain at 4. Hence a 0 to 5 V at the noninverting input will produce 0 to 20 V at the output. The input reference voltage is supplied by the 5 V Zener and potentiometer $VR_1 = 5 \text{k}$. On the negative side, the noninverting input of the op-amp is connected to ground and the inverting input connected to the junction of equal resistors $R_3 = R_4 = 10 \text{k}$ which are connected between the positive and negative supplies. Hence as the positive voltage changes in response to the changing potentiometer, the negative output will track it as the feedback ensures that the inverting potential is held at zero potential as is the noninverting terminal. Resistor $R_5 = 5.6 \text{k}$ passes about 5 mA into the Zener diode $D_3$. Allowing a 2 V peak-to-peak ripple voltage, capacitor $C_1$ and $C_2$ are given by $C_1 = C_2 = 1 \text{A}/2 \times 60 = 8333 \mu \text{F}$. Capacitor $C_3$ is set at $C_3 = 100 \mu \text{F}$ to ensure low ripple across the reference Zener. $C_4 = C_5 = 1 \mu \text{F}$ are placed at the outputs to provide further filtering.
Ideas for Exploration: (i) Replace $R_5$ by a constant current diode to improve performance. (ii) Introduce electronic protection. (iii) Modify the system to allow for switching between tracking and independent voltage adjustment of the two supplies.

10.8.8 Precision Voltage Divider

This project involves the development of a precision voltage divider circuit that converts 30 V into ±15 V with current boosting for powering operational amplifiers. The circuit is shown in Fig. 10.69 and uses the op-amp current booster circuit discussed in Chap. 9, Fig. 9.34 where resistors $R_1$ and $R_2$ set the voltage ratio at the output. Feedback via $R_4$ ensures that the ratio set by $R_1$ and $R_2$ is maintained as current is drawn from the output. A 741 is suitable for this application. This system can be used to split other voltages such as that from a 9 V battery to produce ±4.5 V in order to operate a low-voltage op-amp from the battery.
Ideas for Exploration: (i) Examine whether resistor $R_3$ is necessary in this application. (ii) Use an OPA452 to produce higher dual voltages.

10.8.9 Bipolar Adjustable Regulated Power Supply

The circuit in Fig. 10.70 provides an adjustable bipolar power supply. It uses the LM317 and the LM337 regulator ICs used previously. The former provides a variable positive voltage supply while the latter provides a variable negative voltage supply. These ICs can both deliver 1.5 A with output given by $V_{DC} \approx \pm 1.25(1 + R_2/R_1)$. Using $R_1 = 220 \, \Omega$ and potentiometer $R_2 = 5k$, then the minimum output voltage is

$$V_{DC} = \pm 1.25 \, V \text{ for } R_2 = 0 \text{ and } V_{DC} = \pm 1.25(1 + 5000/220) \approx \pm 30 \, V.$$ A 50V center-tapped transformer 2A current rating is used to power the system. This gives peak output voltage $\pm 25 \sqrt{2} \approx \pm 35 \, V$. Allowing 2 V peak-to-peak ripple then the filter capacitor values are given by $C_1 = C_2 = 1.5/2 \times 60 \times 2 = 4167 \, \mu F$. Use $C_1 = C_2 = 5000 \, \mu F$. Small capacitors $C_3 = C_4 = 1 \, \mu F$ at the output provide additional filtering to remove noise. Diodes $D_1$ to $D_4$ can be 1N5402 which have ratings of 3 A and PIV of 200 V.
Ideas for Exploration: (i) Modify the system to introduce tracking such that adjustment of the voltage of one supply, say the positive side, is automatically tracked by the voltage of the negative supply. One approach to accomplishing this is that used in Fig. 10.68.

10.8.10 Variable Voltage Regulated Supply Using LM338
The power supply circuit in Fig. 10.71 uses the LM338 regulator IC. This IC can deliver 5 A over a voltage range from 1.2 to 32 V and needs only two resistors to set the output voltage. The device is current limited and thermally protected and has excellent load and line regulation characteristics. The output voltage for this circuit is given by

$$V_{DC} = 1.25 \left(1 + \frac{R_2}{R_1}\right)$$

The unregulated part of the supply follows the established design procedure. It utilizes a BR34 bridge rectifier which contains four diodes. Resistor $R_1$ is set at 220 Ω and $R_2$ is a potentiometer. Using $R_2 = 2k$ enables the output voltage to vary from 1.25 V to

$$V_{DC} = 1.25 \left(1 + \frac{2000 \text{ to } 2200}{220}\right) = 12.6 \text{ V}$$

Resistor $R_3 = 1k$ and the red LED indicate when the supply is on and also enable discharge of capacitor $C_1 = 5000 \mu F$ when the supply is turned off. A small capacitor
$C_2 = 10 \mu F$ at the output removes any high-frequency noise from the supply.

![Variable regulator using the LM338 IC](image)

**Fig. 10.71** Variable regulator using the LM338 IC

*Ideas for Exploration:* (i) Investigate the measurement of line and load regulation for this power supply.

### 10.8.11 Research Project 1

The transistor feedback regulator in Fig. 10.72 considered previously was enhanced by bootstrapping resistor $R_3$. Another approach to performance enhancement is the use of a constant current diode in place of the resistor $R_3$. In the existing circuit, ripples from the unregulated supply will cause variation in the current in $R_3$ which must be accommodated by the error transistor. This therefore shows up in the regulated output. With a constant current diode instead of resistor $R_3$, there will be significantly reduced variation in the current resulting from ripples in the unregulated supply and hence reduced ripple in the regulated output. The project requirement is to design the regulator using a constant current diode instead of resistor $R_3$. The current considerations are the same as before in that current through the CCD must supply both the collector current of the error transistor and the base current of the pass transistor.
Ideas for Exploration: (i) Simulate this system and that using bootstrapping and compare the load regulation and line regulation performances of the two systems; (ii) Add short-circuit protection; (iii) Explore the idea that if the CCD current is sufficiently large say 10 mA, then resistor $R_4$ may not be necessary as sufficient current may be available through $Tr_1$; (iv) In the event that $R_4$ is omitted, convert the system into a variable voltage regulator.

10.8.12 Research Project 2

This project shown in Fig. 10.73 requires the design of a high-current fixed-voltage regulator using the 7812 voltage regulator IC. This IC can deliver 12 V at about 1 A but has its current rating boosted by the use of three parallel-connected power transistors ($Tr_1, Tr_2, Tr_3$) such as $MJ2955$. The current into the regulator $I_{reg}$ is made up of current $I_{R1}$ through $R_1$ and the base current $I_B$ of the three power transistors such that $P_D \geq V_Z I_{Z\text{max}}$. Since the voltage across $R_1$ is $V_{BE}$, then

$$R_1 = \frac{V_{BE}}{I_{R1}} = \frac{V_{BE}}{\left(I_{reg} - I_B\right)}$$

where $I_B = I_C/\beta$ and $I_C$ is the transistor collector current. Let the current provided by the collector of the each
transistor be 5A. Then the total current delivered by the transisotrs is $I_C = 15$ A. For $I_{reg} = 1$ A and assuming $\beta = 20$, it follows that

$$R_1 = 0.7 / \left(1A - \frac{15A}{20}\right) = 2.8 \, \Omega.$$  

Resistors $R_2, R_3, R_4$ which are set to about 0.1 $\Omega$ ensure that the current into the emitters of the three transisotrs is divided equally such that each carries about 5A. The total current available from the supply is $I_C + I_{reg} = 15A + 1A = 16$ A. A

15 V transformer with a current rating of 16 A is selected. This gives a peak voltage of $15 \sqrt{2} = 21.2$ V. Allowing for a minimum of 4 V across the regulator IC and for transformer resistance voltage drop with an output voltage of 12 V, the peak-to-peak ripple into the regulator IC can be about 5 V. Hence capacitor $C_1 = \frac{15A}{2 \times 60 \times 5} = 25,000 \, \mu F$. Capacitor $C_2 = 100 \, \mu F$ assists with filtering into the regulator and capacitor $C_3 = 1 \, \mu F$ provides filtering at the output. The diode bridge must be rated at 16 A and a 16 A fuse should be included at the output. The transistors and diode bridge should be mounted on heatsinks.

*Fig. 10.73*  High-current fixed-voltage regulator
**Ideas for Exploration:** (i) Re-design the system using a 7805 voltage regulator in order to provide a high-current 5 V regulated power supply; (ii) Use the 7912 to design a negative voltage supply to compliment the positive voltage supply in Fig. 10.73. Use three parallel-connected 2N3055 npn power transistors.

### 10.8.13 Research Project 3

This project examines a *regulated power supply* configuration that is slightly different from those already considered. The basic circuit is shown in Fig. 10.74, where a 15 V, 1 A transformer drives a bridge rectifier and is filtered by capacitor $C_1 = 1000 \mu F$. This results in an unregulated voltage of about 20 V. This voltage is applied to the 13 V Zener diode in series with current setting resistor $R_1$. Setting $R_1 = 1 \, k$ results in a Zener diode current of $(20 - 13)/1 \, k = 7 \, mA$. The stabilized voltage produced by the Zener is applied to a voltage divider string of resistors $R_2 = 2.7 \, k, R_3 = 820 \, \Omega, R_4 = 1.5 \, k$ and $R_5 = 1.5 \, k$. This (in conjunction with the output transistor) provides four reference voltages: 4.5, 6, 9, and 12 V. The voltage at the positive terminal is the zero reference, and that on the negative terminal is the variable voltage. This is different from the previous regulators where the positive rail is usually the variable one. Transistors $Tr_2$ and $Tr_3$ form a pnp feedback pair, and $Tr_1$ provides short-circuit protection. With $R_6 = 1.5 \, \Omega$, load currents in excess of about 450 mA causes $Tr_1$ to turn on and limit the current to the base of the feedback pair, thereby converting the supply from a constant voltage supply into a constant current supply. Under short-circuit conditions, the full unregulated supply voltage is across $Tr_2$ and with 450 mA flowing through the device, some 10 W of power would be dissipated in this device. It must therefore be mounted on a suitable heat sink. Capacitor $C_2 = 100 \mu F$ provides additional filtering at the output, and resistor $R_7 = 1 \, k$ discharges this capacitor when the supply is turned off.
Ideas for Exploration: (i) Introduce an LED in series with $R_7$ to indicate the ON condition. (ii) Convert the regulated supply into a fully variable supply by replacing the resistor string by a potentiometer of value about 10 k. The wiper of the potentiometer then goes to the base of $Tr_3$. (iii) Introduce fold-back current limiting to this circuit.

10.8.14 Research Project 4
In this research project, a *high-current variable-voltage* regulator using the LM317 regulator IC is designed to deliver a variable voltage from 1.25 to 15 V at a current of 20 A. The circuit is shown in Fig. 10.75. Here four 2N3055 power transistors ($Tr_1$, $Tr_2$, $Tr_3$, $Tr_4$) are used to boost the current capacity of the LM317. The transistors are connected in parallel in the emitter follower configuration. Resistors $R_3 = 0.47 \, \Omega$ are placed in the emitter of each transistor in order to distribute the current load such that each transistor carries about 5A resulting in a total output current of 20A. The base of the parallel arrangement is driven by the output of the LM317 which is connected as a variable voltage regulator. With $R_1 = 220\Omega$ and $R_2 = 2.5k$ the output is variable from 1.25 to about 15 V. This IC is able to provide the required current to the transistor bases of $20A/20 = 1A$ using $\beta = 20$. Note that there will be a voltage loss of 0.7 V across the base-emitter junctions of the transistors which will increase as the load current is increased because of the emitter resistors $R_3$. The
transformer used is rated at 18 V, 20 A and the diode bridge should also be rated at not less than 30 A. Allowing a peak-to-peak ripple of 5 V, the filter capacitor $C_1$ is given by $C_1 = \frac{20}{2 \times 60 \times 5} = 33,333 \ \mu F$. This capacitor can be realized by using three 10,000µF capacitors connected in parallel. The LED $D_1$ in conjunction with $R_4 = 2.2k$ provides ON indication as well as discharges the filter capacitors when the system is off. Capacitor $C_2 = 10 \ \mu F$ provides additional filtering at the output of the IC regulator. A 20 A fuse should be introduced at the output for protection against current overload.

![High-current variable-voltage regulator](image)

*Fig. 10.75* High-current variable-voltage regulator

*Ideas for Exploration*: (i) Use the LM337 to design a negative voltage supply to compliment the positive voltage supply in Fig. 10.75. Use four parallel-connected MJ2955 pnp power transistors.

**10.8.15 Research Project 5**
This research project involves the investigation of a \textit{switch-mode power supply}. Such a supply converts one voltage level to another by switching devices on and off at high frequency and using energy storage devices such as an inductor and/or a capacitor. Its main advantage over the linear regulators discussed in this chapter is its high efficiency which is better than 90\%. One class of switch-mode power supply is the step down or \textit{buck converter} shown in Fig. 10.76. The operation can be divided into two phases: a charge phase and a discharge phase. In the charge phase, the switch $S$ is closed, and energy is stored in the inductor $L$. In the discharge phase, the switch is open, and the energy stored in the inductor is transferred to the output capacitor $C$ and load through the diode $D$. The capacitor maintains the load voltage during the charging phase of the inductor which is central to the energy transfer process. Since there is no build-up of current in the inductor, it follows that the change in inductor current $\Delta I_L$ during the charging phase must be equal to the change in inductor current $\Delta I_D$ during the discharge phase, i.e., $|\Delta I_L| = |\Delta I_D|$. From this it can be shown that the relation between the input voltage $V_i$ and the output voltage $V_o$ is given by $V_o = DV_i$ where $D = T_{ON}/T_S$, $T_{ON}$ is the on-time of the switch and $T_S$ is the switching period. Since $D < 1$, then $V_o < V_i$ which represents a reduction of the input voltage as generally occurs with the series regulators discussed in this chapter.

![Step-down buck converter](image)

\textit{Fig. 10.76} Step-down buck converter

A simple implementation of this system is shown in Fig. 10.77. A variable duty cycle square wave is generated by the 555 timer, and this
is used to switch on and off a p-channel MOSFET IRF4905. Potentiometer $VR_1 = 10 \, k$ varies the duty cycle of the square wave and hence the output voltage. The output voltage in this circuit varies with changing load since no feedback is present. An improved circuit is shown in Fig. 10.78. It uses a Texas Instruments LM2576HV-ADJ integrated circuit that contains the pulse generation and switching circuitry necessary to realize a buck converter. Importantly, it contains feedback circuitry that changes the pulse width and thereby maintains a constant output voltage. Potentiometer $VR_1 = 50 \, k$ varies the amount of feedback and hence the output voltage. This version of the IC enables a variable output voltage from 1.2 to 50 V at 3 A.

![Buck converter using 555 timer](image)

**Fig. 10.77** Buck converter using 555 timer
Ideas for Exploration: (i) Investigate the operation of a boost converter that increases the voltage supplied to the system.

Problems
1. Describe the operation of a full-wave rectifier and derive the expression for the average and rms output voltages.
2. Explain how the inclusion of a filter capacitor reduces the ripple in the output voltage and derive an expression for the peak-to-peak value of this ripple voltage.
3. Design an unregulated power supply to deliver 15 V at 1 A. Use a 15-V transformer with a bridge rectifier and allow for a maximum ripple voltage of 1.5 V peak-to-peak.
4. Re-design the circuit of Question 3 using a half-wave rectifier.
5. A voltage from an unregulated supply varies between a minimum value of 12 V and a maximum value of 18 V. Using this unregulated supply, design a Zener-regulated supply that delivers 9 V DC with a current capacity of 15 mA.
6. Design a single transistor regulated supply using a Zener diode capable of delivering 15 V at 120 mA. Use a half-wave rectifier to drive the regulator. Show how this circuit can be equipped with short-circuit protection.
7. Design a regulated supply using a Darlington pair and a Zener diode that delivers 9 V at 1.5 A. Use a full-wave rectifier to drive the regulator.
8. Explain the operation of the regulator shown in Fig. 10.79. Using this circuit, design a regulated supply to deliver 9 V at 0.5 A.
9. Explain the operation of the regulator circuit shown in Fig. 10.80, describing the circuit corrective action for unwanted increases or decreases in output voltage.
describing the circuit corrective action for unwanted increases or decreases in the output and giving an indication of the action of capacitor C.

10. Using the circuit shown in Fig. 10.80, design a +16 V, 1.2 A regulator that is driven by an unregulated supply having 2-V peak-peak input ripple. Use a 20-V transformer and a bridge rectifier to provide the unregulated input. Assume the power transistor has a gain of 20 and the other transistors have gains of 125. Justify all your design steps.

11. Show how electronic protection can be added to this circuit and describe its operation.

12. Introduce bootstrapping of resistor $R_3$ in the design of Problem 10 and describe the effect of this bootstrapping.

13. Using the circuit shown in Fig. 10.81, design a +16 V, 1.2 A regulator that is driven by an unregulated supply having 2-V peak-peak input ripple. Use a 20-V transformer and a bridge rectifier to provide the unregulated input. Assume the power transistor has a gain of 20 and the other transistors have gains of 125. Justify all your design steps.

14. Design a regulated supply using the basic topology in Fig. 10.82 rated at 10 V and 150 mA. Power for the regulator must come from an unregulated supply using a half-wave bridge rectifier and a 12-V transformer having a ripple voltage of 1.5-V peak-to-peak at maximum load current. Use a pass transistor with current gain of 150. Include short-circuit protection in your design.

15. Using the circuit shown in Fig. 10.83, design a +20 V, 1.5 A regulator that is driven by an unregulated supply having 2.5-V peak-peak input ripple. Use a 30-V transformer and a full-wave rectifier to provide the unregulated input. Assume the power transistor has a gain of 50 and the other transistor has a gain of 150. Justify all design steps.

16. Discuss the manner in which output voltage variation can be
17. Design a 9V regulator using the 7809 regulator IC.

18. Design a single transistor regulator to power a small radio from the mains supply. The required voltage is 6 V and the maximum current demand is 50 mA.

19. How can a constant current diode be used to improve the performance of a regulated power supply?

20. Indicate other methods of improving the performance of a regulator.

21. Design a + 12 V regulated supply using regulator IC from the 7800 series.

22. Design a ± 15 V regulated bipolar supply using regulator ICs from 7800 and 7900 series.

23. Using the circuit of Fig. 10.60, design a variable voltage regulated supply that can deliver 0–9 V at 100 mA. Design a variable voltage bench power supply using a Darlington pair and the topology of Fig. 10.84.

24. Outline the operation of a switch-mode buck regulator.
**Fig. 10.79** Circuit for Question 8

**Fig. 10.80** Circuit for Question 9
**Fig. 10.81** Circuit for Question 13

**Fig. 10.82** Circuit for Question 14
Fig. 10.83  Circuit for Question 15

Fig. 10.84  Circuit for Question 24

**Bibliography**


A filter is an electrical network that passes signals within a specified band of frequencies while attenuating those signals that fall outside of this band. Passive filters utilize passive components, namely, resistors, capacitors, and inductors, while active filters contain passive as well as active components such as transistors and operational amplifiers. Passive filters have the advantage of not requiring an external power supply as do active filters. However, they often utilize inductors, which tend to be bulky and costly, whereas active filters utilize mainly resistors and capacitors. Additionally, active filters can produce signal gain and generally have high input and low output impedances, which allow simple cascading of systems with little or no interaction between stages. This chapter discusses the principles of active filter operation and treats with several types and configurations of active filters. At the end of the chapter, the student will be able to:

- Understand the principles of operation of the basic types of filters.
- Explain the operation of a range of active filters.
- Design a range of active filters.
11.1 Introduction to Filters

There are five basic types of filters: low-pass, high-pass, band-pass, band-stop (or notch), and all-pass filters. A low-pass filter passes signals with constant amplitude from DC up to a frequency $f_c$ referred to as the cut-off frequency. The signal output above $f_c$ is attenuated. This is shown in Fig. 11.1, where the magnitude of the output voltage of the ideal (solid line) and practical (dashed line) responses is plotted against the frequency. The ideal response shows the pass-band, the range of transmitted frequencies, the stop-band, the range of attenuated frequencies, and the cut-off or break frequency $f_c$. In the practical response, $f_c$ is the frequency at which the magnitude of the output voltage falls to 0.707 of its low-frequency value, which is −3 dB. Here, $f_c = 1$ Hz for the normalized response.

![Fig. 11.1 Low-pass filter response](image)

A high-pass filter attenuates signals from DC up to a frequency $f_c$ while passing all signals with constant amplitude above $f_c$. The normalized response is shown in Fig. 11.2, where the ideal and practical responses with pass-band and stop-band are indicated. A band-pass filter passes a band of frequencies, while frequencies outside
of that band are attenuated. This is shown in Fig. 11.3, where the ideal and practical responses are indicated. A band-stop filter stops a band of frequencies while passing all frequencies outside that band. It performs in a manner that is exactly opposite to the band-pass filter. The band-stop response is shown in Fig. 11.4 with ideal and practical responses. Finally, an all-pass filter passes all frequencies with a constant amplitude output but with a changing phase. This is shown in Fig. 11.5.

![High-pass filter response](image-url)
Fig. 11.3  Band-pass filter response

Fig. 11.4  Band-stop filter response
11.2 Basic First-Order Low-Pass Filter

We first consider a low pass filter of the simplest kind shown in Fig. 11.6a. It is a noninverting low-pass active filter using an RC network feeding into a unity-gain operational amplifier. A resistor $R_{os}$ is sometimes included in the feedback loop of the op-amp in order to minimize DC offset at the output, as shown in Fig. 11.6b. For the circuit, we have

$$A_f = \frac{V_o}{V_i} = \frac{1/sC}{R + 1/sC} = \frac{1}{1 + j\omega RC} = \frac{1}{1 + jf/f_c} \tag{11.1}$$

where

$$f_c = 1/2\pi RC. \tag{11.2}$$
Note that for \( f \ll f_c \), \( |A_f| \rightarrow 1 \), and for \( f \gg f_c \), \( |A_f| \rightarrow 0 \). The frequency response plot for this circuit is shown in Fig. 11.7, which is clearly a low-pass response. The frequency \( f_c = 1/2\pi RC \) is the cut-off frequency. The system has one pole at \( f = f_c \) and is, therefore, first-order. At this frequency, the filter transfer function becomes

\[
A_f(f_c) = \frac{1}{1 + jf_c/f_c} = \frac{1}{1 + j}.
\]

(11.3)
This reduces to
\[ A_f(f_c) = \frac{1}{\sqrt{2} \angle 45^\circ} = 0.707 \angle -45^\circ. \]  \hspace{1cm} (11.4)

Hence
\[ |A_f|_{f_c} = \frac{1}{\sqrt{2}} = 0.707 \]  \hspace{1cm} (11.5)

with
\[ |A_f|_{f_c} \text{ (dB)} = 20 \log 0.707 = -3 \text{ dB}. \]  \hspace{1cm} (11.6)

The signal phase is
\[ \angle A_f(f_c) = -45^\circ. \]  \hspace{1cm} (11.7)

Equation (11.2) is used to design the filter.

**Example 11.1**  Design a low-pass noninverting filter with unity gain and a break frequency of 1 kHz.

**Solution**  Choose \( C = 0.01 \) \( \mu \)F. Then, from Eq. (11.2),
\[ R = \frac{1}{2\pi} \times 10^3 \times 0.01 \times 10^{-6} = 16 \text{ k}. \]  If low DC offset is required, then \( R_{os} = R = 16 \text{ k}. \)

**11.2.1 Low-Pass Filter with Gain**

The low-pass filter with gain is achieved by reducing the feedback around the op-amp, as shown in Fig. 11.8. The transfer function is given by
\[ \frac{V_o}{V_i} = \frac{k}{1 + jf/f_c} \]  \hspace{1cm} (11.8)

where \( f_c = 1/2\pi RC \) is the break frequency and \( k = 1 + \frac{R_2}{R_1} \) is the low-frequency gain. For low DC offset, \( R = R_2/R_1 \).
An alternative configuration for a first-order low-pass filter is shown in Fig. 11.9a. It is an inverting amplifier configuration with a capacitor $C$ across the feedback resistor $R_2$. From Fig. 11.9a, we have

\[
\frac{V_i}{R_1} = \frac{-V_o}{R_2/1/sC} = -V_o \frac{R_2}{1 + sCR_2}
\]

which yields

\[
A_f = -\frac{R_2}{R_1} \frac{1}{1 + sCR_2} = \frac{-k}{1 + jf/f_c}
\]

where $f_c = 1/2\pi R_2 C$ is the break frequency and $k = R_2/R_1$ is the low-frequency gain. For reduced DC offset, a resistor $R_{os} = R_1/\parallel R_2$ can be inserted between the noninverting terminal and ground, as shown in Fig. 11.9b.
Example 11.2  Design a first-order noninverting low-pass filter with a gain of 10 and a cut-off frequency of 5 kHz using Fig. 11.8.

Solution  Choose $C = 0.01 \mu F$. Then, from $f_c = 1/2\pi RC$, resistor $R$ is found to be $R = 1/(2 \times \pi \times 5 \times 10^3 \times 0.01 \times 10^{-6}) = 3.2 \, k$. Since $1 + R_2/R_1 = 10$, for $R_1 = 1 \, k$, then $R_2 = 9 \, k$. The solution is shown in Fig. 11.10.
**Design Procedure**

In preparation for the discussion on higher order filters and their realization, we wish to develop a more ordered procedure for designing first-order filters. Thus, the basic first-order system can be written as

\[
A(s) = \frac{A_o}{1 + a_1 (s/\omega_c)}
\]  

(11.11)

where \( A_o = k \) is the low-frequency gain, \( \omega_c = 2\pi f_c \) is the cut-off frequency, and here \( a_1 = 1 \). For higher order filters considered later, the condition \( a_1 \neq 1 \) will arise.

For the first-order noninverting low-pass filter, the transfer function is given by

\[
A_f(s) = \frac{1 + \frac{R_2}{R_1}}{1 + RC s}.
\]  

(11.12)

Comparing coefficients in (11.11) and (11.12) gives

\[
A_o = 1 + \frac{R_2}{R_1}
\]  

(11.13)

\[
a_1/2\pi f_c = RC.
\]  

(11.14)

The design steps are as follows:

1. Select \( C \) usually between 100 pF and 1 \( \mu \)F.
2. Set the coefficient \( a_1 = 1 \).
3. Determine \( R \) using \( R = a_1/2\pi f_c C \).
4. Select \( R_1 \) and find \( R_2 \) using \( R_2 = R_1 (A_o - 1) \).

For the first-order **inverting** low-pass filter, the basic first-order system can be written as

(11.15)
The transfer function for the actual system is given by

\[ A(s) = -\frac{A_o}{1 + a_1 (s/\omega_c)}. \]

Comparing coefficients in (11.15) and (11.16) gives

\[ A_o = \frac{R_2}{R_1} \quad (11.17) \]

\[ a_1/2\pi f_c = R_2C. \quad (11.18) \]

The design steps are as follows:

1. Select \( C \) usually between 100 pF and 1 \( \mu \)F.
2. Set the coefficient \( a_1 = 1 \).
3. Determine \( R_2 \) using \( R_2 = a_1/2\pi f_c C. \)
4. Determine \( R_1 \) using \( R_1 = R_2/A_o. \)

### 11.3 Low-Pass Second-Order Filter

It is possible to cascade two first-order low-pass filters with the same cut-off frequency \( f_c \) each with \(-20 \text{ dB/dec} \) roll-off rate low-pass second-order filter to get a second-order filter with a roll-off rate of \(-40 \text{ dB/dec} \). This is shown in Fig. 11.11. Such an approach has several disadvantages. The first is that the cut-off frequency of the overall filter is lower than the cut-off frequency \( f_c \) of the individual first-order filters. The result is that the pass-band gain begins to fall well before the cut-off frequency \( f_c \). Second, the transition from the pass-band to the stop-band lacks sharpness as is desired in a filter. Third, it can be shown that
the phase response is not linear with the effect that signal distortion results. A low-pass filter can be optimized to meet at least one of the following three requirements: (i) maximum flatness in the pass-band; (ii) maximum sharpness in the transition from pass-band to stop-band; and (iii) linear phase response.

In order to allow optimization of a filter, the transfer function of the filter must contain complex poles and, hence, for a second-order filter, must take the following form:

\[
A(s) = \frac{A_o}{(1 + a_1 (s/\omega_c) + b_1(s/\omega_c)^2)}
\]  

where \(A_o\) is the low-frequency gain in the pass-band and \(a_1\) and \(b_1\) are positive real filter coefficients. These coefficients define the location of the complex poles of the filter and thereby determine the characteristics of the filter transfer function. The angular frequency \(\omega_c = 2\pi f_c\) represents the cut-off frequency of the filter. This transfer function can be normalized by setting \(\omega_c = 1\) giving

\[
(11.20)
\]
Several filter types are available: (i) **Butterworth** response, with maximum pass-band flatness; (ii) **Chebyshev** response, with sharpened transition from pass-band to stop-band; (iii) **Bessel** response, with linearized phase response within the pass-band; (iv) **inverse Chebyshev** response, having flat pass-band and ripples in the stop-band; and (v) **Elliptic (Cauer)** response, which is an optimal approximation to the ideal low-pass filter with ripples in the pass-band and the stop-band. These filter responses occur for second- and higher order and not for first-order where complex poles are not possible, and therefore all filter types have identical responses for a first-order low-pass filter [corresponding to \( a_1 = 1 \) in (11.11)]. Only the Butterworth, Chebyshev, and Bessel filters are considered in this chapter.

The amplitude responses of first-, second-, and third-order **Butterworth** low-pass filters using the normalized characteristic are shown in Fig. 11.12. The filter provides maximum flatness in the pass-band, and as the order increases, the pass-band flatness occurs for higher frequencies before the break frequency. This type of filter is, therefore, ideal for audio systems, where high-frequency noise needs to be removed with maximum pass-band flatness in order to preserve signal quality. The **Chebyshev** low-pass filter provides increased roll-off rate as compared with the Butterworth filter. The price paid for this is constant amplitude ripples in the pass-band. The amplitude of these ripples for a filter of given order may be varied by changing the filter coefficients; the higher the ripple amplitude, the steeper the roll-off rate. The **Bessel** low-pass filters have a linear phase response as compared with the Butterworth and the Chebyshev filters resulting in constant group delay. The pass-band gain, however, is not at flat as the Butterworth though it is flatter than the Chebyshev and the roll-off rate is less than both the Chebyshev and the Butterworth. A graphical comparison of these three filter responses is presented in Fig. 11.13.
The second-order low-pass filter transfer function (11.19) can be realized around a single active device using two topologies: the Sallen–Key and the multiple feedback (MFB).
11.3.1 Sallen–Key or Voltage-Controlled Voltage Source (VCVS) Topology

The circuit shown in Fig. 11.14 is one implementation of a second-order low-pass filter referred to as the Sallen–Key or VCVS topology. Using Kirchhoff’s current law (KCL), the node equations at junctions $A$ and $B$ are

\[
\frac{V_i - V_A}{R_1} = \frac{V_A - V_B}{R_2} + (V_A - V_o) sC_2
\]  \hspace{1cm} (11.21)

\[
\frac{V_A - V_B}{R_2} = V_B sC_1
\]  \hspace{1cm} (11.22)

where $V_B = V_o$. Eliminating $V_A$ and $V_B$ yields

\[
A_f = \frac{V_o}{V_i} = \frac{1}{1 + sC_1 (R_1 + R_2) + s^2 R_1 R_2 C_1 C_2}.
\]  \hspace{1cm} (11.23)

Comparing coefficients for (11.23) and (11.19) yields

\[
A_o = 1
\]  \hspace{1cm} (11.24)

\[
a_1/\omega_c = C_1 (R_1 + R_2)
\]  \hspace{1cm} (11.25)

(b)
\[
\frac{b_1}{\omega_c^2} = R_1 R_2 C_1 C_2.
\]

From (11.25), we have
\[
R_2 = \frac{a_1}{\omega_c C_1} - R_1
\]  \hspace{1cm} (11.27)
and hence
\[
\frac{b_1}{\omega_c^2} = R_1 C_1 C_2 \left(\frac{a_1}{\omega_c C_1} - R_1\right).
\]  \hspace{1cm} (11.28)

After manipulation, this leads to a quadratic equation in \(R_1\) given by
\[
\omega_c^2 C_1 C_2 R_1^2 - \omega_c a_1 C_2 R_1 + b_1 = 0.
\]  \hspace{1cm} (11.29)
Solving for \(R_1\), we get
\[
R_1 = \frac{a_1 C_2 + \sqrt{a_1^2 C_2^2 - 4b_1 C_1 C_2}}{4\pi f_c C_1 C_2}
\]  \hspace{1cm} (11.30)
where the positive sign from the square root is taken and
\[
C_2 \geq 4b_1 C_1 / a_1^2.
\]  \hspace{1cm} (11.31)

Substituting (11.30) for \(R_1\) into (11.27) gives
\[
R_2 = \frac{a_1 C_2 - \sqrt{a_1^2 C_2^2 - 4b_1 C_1 C_2}}{4\pi f_c C_1 C_2},
\]  \hspace{1cm} (11.32)

We can now state a design procedure for a specific cut-off frequency:

**Design Procedure**

1. Select \(C_1\) usually between 100 pF and 1 \(\mu\)F.
2. For the specific type of filter (Butterworth, Chebyshev, and Bessel) and the specific filter requirements, obtain the coefficients \(a_1\) and \(b_1\) from the relevant table.
3. Determine \(C_2\) using \(C_2 \geq 4b_1 C_1 / a_1^2\).
Find $R_1$ and $R_2$ using
\[ R_1 = \frac{a_1 + \sqrt{a_1^2 - 4b_1C_1/C_2}}{4\pi f_c C_1} \]

5. Determine $R_{os} = R_1 + R_2$ for minimum offset voltage.

**Example 11.3**  Design a VCVS second-order unity-gain low-pass Butterworth filter with a cut-off frequency of 10 kHz.

**Solution**  For this case, $f_c = 10$ kHz. Select $C_1 = 0.001 \mu F$. For second-order Butterworth, \( a_1 = \sqrt{2}, b_1 = 1 \). Then \( C_2 \geq \frac{(4 \times 1 \times 0.01 \times 10^{-6})}{\sqrt{2}} \)

Select $C_2 = 0.05 \mu F$. Hence $R_1 = \frac{1.4142 + \sqrt{2 - \frac{(4 \times 1 \times 0.01 \times 10^{-6})}{0.05 \times 10^{-6}}}}{4\pi \times 10 \times 0.01 \times 10^{-6}} = 2 \ \Omega$ and $R_2 = \frac{1.4142 + \sqrt{2 - \frac{(4 \times 1 \times 0.01 \times 10^{-6})}{0.05 \times 10^{-6}}}}{4\pi \times 10 \times 0.01 \times 10^{-6}} = 254 \ \Omega$. Finally, for minimum offset,

\[ R_{os} = 2000 + 254 = 2254 \ \Omega. \]

Based on the design Eqs. (11.30) and (11.32), the resistor and capacitor values can be scaled in order to get more appropriate values. Specifically, $R_1, R_2 \rightarrow \alpha R_1, \alpha R_2$, where $\alpha$ may be referred to as an impedance scaling factor, and $C_1, C_2 \rightarrow C_1/\alpha, C_2/\alpha$ will leave the filter characteristics unaffected. This can be seen by simply substituting $\alpha R_1, \alpha R_2$ and $C_1/\alpha, C_2/\alpha$ into (11.30) and (11.32) that the equations are unchanged. Also, the system can be designed for gain, as shown in Fig. 11.15, where

\[ k = 1 + R_b/R_a. \]  \hspace{1cm} (11.33)
The process of developing the associated design procedure follows that used for the unity-gain case.

**Example 11.4**  Develop a design procedure for the VCVS Butterworth second-order low-pass filter with gain for the special case when $R_1 = R_2$ and $C_1 = C_2$.

**Solution**  Using nodal analysis, the transfer function for the filter with gain is given by

$$A_f = \frac{V_o}{V_i} = \frac{k}{1 + s(C_1R_1 + C_1R_2 + C_2R_1 - kC_2R_1) + s^2R_1R_2C_1C_2}.$$  \hfill (11.34)

For the case where $R_1 = R_2 = R$ and $C_1 = C_2 = C$, (11.34) reduces to

$$A_f = \frac{V_o}{V_i} = \frac{k}{1 + s(3 - k)CR + s^2R^2C^2}.$$  \hfill (11.35)

Comparing coefficients with (11.19)

$$A(s) = \frac{A_o}{\left(1 + a_1(s/\omega_c) + b_1(s/\omega_c)^2\right)}$$  \hfill (11.36)

yields
For a Butterworth filter, \( a_1 = \sqrt{2} \) and \( b_1 = 1 \). Hence, from (11.39), we have

\[
\omega_c = 1/RC, \quad f_c = 1/2\pi RC
\]  

(11.40)

and from (11.38), we have

\[
\sqrt{2} = 3 - k
\]  

(11.41)

giving

\[
k = 3 - \sqrt{2} = 1.6.
\]  

(11.42)

For minimum offset, we have

\[
R_1 + R_2 = R_a/ \parallel R_b = \frac{R_a R_b}{R_a + R_b} = \frac{R_b}{k}.
\]  

(11.43)

Hence

\[
R_b = k (R_1 + R_2) = 3.2R.
\]  

(11.44)

Also

\[
R_1 + R_2 = R_a/ \parallel R_b = \frac{R_a R_b}{R_a + R_b} = \frac{R_a (k - 1)}{k}.
\]  

(11.45)

Hence

\[
R_a = \frac{k (R_1 + R_2)}{k - 1} = 3.2 \ R/0.6 = 5.3 \ R.
\]  

(11.46)

These equations enable the determination of \( R_a \) and \( R_b \) to satisfy both the gain requirement and the minimum offset requirement. We
can now state a design procedure for a specific cut-off frequency:

**Design Procedure**

1. Select $C_1 = C_2 = C$ usually between 100 pF and 1 μF.
2. Determine $R = 1/2\pi f_c C$.
3. Set $R_1 = R_2 = R$.
4. Find $R_a$ and $R_b$ using (11.46) and (11.44).

### 11.3.1.1 Simplified Design Procedure for Second-Order Low-Pass Unity-Gain Butterworth Filter

A simplified design procedure for the unity-gain second-order Butterworth filter can be developed. Consider the transfer function (11.19) for a low-pass second-order filter:

$$A(s) = \frac{A_o}{\left(1 + a_1 \left(s/\omega_c\right) + b_1 \left(s/\omega_c\right)^2\right)}. \quad (11.47)$$

For unity gain, $A_o = 1$, and for a Butterworth response from Table 11.1, $a_1 = \sqrt{2}$ and $b_1 = 1$. Then, setting $s = j\omega$, (11.10) becomes

$$A(jf) = \frac{1}{1 + j \sqrt{2} \frac{f}{f_c} + \left(j\frac{f}{f_c}\right)^2}. \quad (11.48)$$

**Table 11.1** Butterworth, Bessel, and Chebyshev (0.5 dB) coefficients

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<th>$i$</th>
<th>$a_i$ (Bu)</th>
<th>$b_i$ (Bu)</th>
<th>$a_i$ (Be)</th>
<th>$b_i$ (Be)</th>
<th>$a_i$ (0.5 dB)</th>
<th>$b_i$ (0.5 dB)</th>
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</table>

In the general second-order transfer function (11.23) of Fig. 11.14, if we let \( R_1 = R_2 = R \) and \( C_1 = C_2/2 = C \), then for \( s = j\omega \), the transfer function reduces to

\[
\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{1}{1 + 2RCj\omega + 2R^2C^2(j\omega)^2}.
\]  

(11.49)

Substituting \( \omega = 2\pi f \) and
Clearly, the transfer function (11.51) is identical to the transfer function (11.48), the transfer function of a second-order unity-gain Butterworth filter. Hence, a simplified design procedure for a unity-gain second-order Butterworth filter is as follows:

1. Choose the desired cut-off frequency $f_c$.
2. Choose $C_1$, usually an available value between about 100 pF and 1 μF.
3. Let $C_2 = 2C_1$.
4. Determine $R$ using $R = 1/2 \sqrt{2\pi f C_1}$ and then set $R_1 = R_2 = R$.
5. For minimum offset use $R_{os} = 2R$.

**Example 11.5** Using the configuration shown in Fig. 11.14, re-design the second-order Butterworth filter of Example 11.5 using the simplified approach.

**Solution** Choose $C_1 = 0.01 \mu F$ and then $C_2 = 0.02 \mu F$. Using (11.36),

$$R = 1/2 \sqrt{2\pi} \times 10 \times 10^3 \times 0.01 \times 10^{-6} = 1.1 \text{ k}$$

and hence

$$R_1 = R_2 = 1.1 \text{ k}, \quad R_{os} = 1.1 \text{ k} \times 2 = 2.2 \text{ k}.$$ 

**Example 11.6** Design a VCVS second-order unity-gain low-pass Chebyshev filter with a cut-off frequency of 10 kHz and a ripple width $RWdB = 2$ dB.
Solution  For this case, \( f_c = 10 \text{ kHz} \). Select \( C_1 = 0.01 \mu F \). From Table 11.2, the coefficients for \( RWdB = 2 \text{ dB} \) are \( a_1 = 1.1813 \) and \( b_1 = 1.7775 \). Then, from (11.31), \( C_2 \geq (4 \times 1.7775 \times 0.01 \times 10^{-6})/(1.1813)^2 = 0.05 \mu F \). Select \( C_2 = 0.1 \mu F \). Hence, from (11.30), \( R_1 = \frac{1.1813+\sqrt{(1.1813)^2-4(4\times 1.7775\times 0.01 \times 10^{-6})/0.01 \times 10^{-6}}}{4\pi \times 10^{-3} \times 0.01 \times 10^{-6}} = 1598 \Omega \), and from (11.32), \( R_2 = \frac{1.1813+\sqrt{(1.1813)^2-4(4\times 1.7775\times 0.01 \times 10^{-6})/0.01 \times 10^{-6}}}{4\pi \times 10^{-3} \times 0.01 \times 10^{-6}} = 282 \Omega \). Finally, for minimum offset, \( R_{os} = 1598 + 282 = 1880 \Omega \).

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<td>1.2614</td>
<td>0.1008</td>
<td>1.2638</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>0.0455</td>
<td>1.0277</td>
<td>0.0347</td>
<td>1.0294</td>
<td>0.0283</td>
<td>1.0304</td>
</tr>
</tbody>
</table>

**Example 11.7**  Design a VCVS second-order unity-gain low-pass Bessel filter with a cut-off frequency of 10 kHz.

**Solution**  For this case, $f_c = 10$ kHz. Select $C_1 = 0.01 \mu F$. From Table 11.1, the Bessel coefficients are $a_1 = 1.3617$ and $b_1 = 0.6180$. Then, $C_2 \geq (4 \times 0.6180 \times 0.01 \times 10^{-6})/(1.3617)^2 = 0.01333 \mu F$. Select $C_2 = 0.02 \mu F$. Hence, $R_1 = \sqrt{\frac{1.3617+\sqrt{(1.3617)^2-(4\times0.6180\times0.01\times10^{-6}/0.02\times10^{-6})}}{4\pi\times10\times10^3\times0.01\times10^{-6}}}$ = 1700 $\Omega$ and $R_2 = \frac{1.3617+\sqrt{(1.3617)^2-(4\times0.6180\times0.01\times10^{-6}/0.02\times10^{-6})}}{4\pi\times10\times10^3\times0.01\times10^{-6}} = 458 \Omega$.

Finally, for minimum offset, $R_{os} = 1700 + 458 = 2158 \Omega$.

**11.3.2 Low-Pass Multiple Feedback Topology**
Another available topology for implementation of second-order low-pass filters is the multiple feedback (MFB) topology shown in Fig. 11.16. In this circuit, there are multiple feedback paths, and the active element is operating in a high-gain mode. The amplifier introduces $180^\circ$ of phase shift in addition to that introduced by the network elements. Assuming an ideal op-amp as the active element, then for nodes $a$ and $b$, 

(11.52)
Noting that \( V_B = 0 \) because node \( b \) is a virtual earth and eliminating \( V_A \), we get

\[
\frac{V_i - V_A}{R_1} = V_A sC_2 + \frac{V_A - V_B}{R_3} + \frac{V_B - V_o}{R_2}
\]

\[
\frac{V_A - V_B}{R_3} = (V_B - V_o) sC_1.
\]  \hspace{1cm} (11.53)

Comparing the coefficients of (11.54) with the general second-order low-pass transfer function

\[
A(s) = -\frac{A_0}{1 + a_1 (s/\omega_c) + b_1 (s/\omega_c)^2}
\]  \hspace{1cm} (11.55)

(where a negative sign is introduced to account for the inversion produced by the MFB configuration) yields

\[
R_E \gg R_B/\beta
\]  \hspace{1cm} (11.56)

\[
(11.57)
\]
\[
a_{\omega_c} = C_1 \left( R_2 + R_3 + \frac{R_2 R_3}{R_1} \right),
\]

\[
b_{\omega_c^2} = C_1 C_2 R_2 R_3.
\]  \hspace{1cm} (11.58)

Solving for \( R_1, R_2, \) and \( R_3 \) in terms of \( C_1 \) and \( C_2 \), we get

\[
R_1 = \frac{a_1 + \sqrt{a_1^2 - 4b_1 (1 + A_o) C_1 / C_2}}{4\pi f_c C_1 A_o}.
\]  \hspace{1cm} (11.59)

In order to ensure a positive value under the square root and hence a real solution for \( R_1 \), then

\[
C_2 \geq C_1 \frac{4b_1 (1 + A_o)}{a_1^2}.
\]  \hspace{1cm} (11.60)

Using (11.59) in (11.56) and (11.58), we get

\[
R_2 = A_o R_1
\]  \hspace{1cm} (11.61)

and

\[
R_3 = \frac{b_1}{4\pi^2 f_c^2 C_1 C_2 R_2}.
\]  \hspace{1cm} (11.62)

**Design Procedure**

1. Select \( C_1 \) usually between 100 pF and 1 \( \mu \)F.

2. For the specific type of filter (Butterworth, Chebyshev, and Bessel) and the specific filter requirements, obtain the coefficients \( a_1 \) and \( b_1 \) from the relevant table.

3. Determine \( C_2 \) to satisfy \( C_2 \geq C_1 \frac{4b_1 (1 + A_o)}{a_1^2} \).

4. Find \( R_1, R_2, \) and \( R_3 \) using

\[
R_1 = \frac{a_1 + \sqrt{a_1^2 - 4b_1 (1 + A_o) C_1 / C_2}}{4\pi f_c C_1 A_o}, \quad R_2 = A_o R_1, \text{ and}
\]
Example 11.8  Design a MFB second-order low-pass Butterworth filter with a gain of 10 and a cut-off frequency of 10 kHz.

Solution  For this case, \( f_c = 10 \text{ kHz} \). Select \( C_1 = 0.001 \mu\text{F} \). From Table 11.1, the Butterworth coefficients are \( a_1 = 1.4142 \) and \( b_1 = 1 \). Then,

\[
C_2 \geq C_1 \frac{4b_1(1+A_o)}{a_1^2}.
\]

\[
C_2 \geq 0.001 \times 10^{-6} \times 4 \times 1 \times (1 + 10)/ (\sqrt{2})^2 = 0.022 \mu\text{F}.
\]

Select \( C_2 = 0.1 \mu\text{F} \). Hence, \( R_1 = \frac{4 \times 10 \times 10^3 \times 0.001 \times 10^{-6} \times 10}{1.4142 + \sqrt{(\sqrt{2})^2 - (4 \times 1 \times 11 \times 0.001 \times 10^{-6}/0.1 \times 10^{-6})}} = 2.12 \text{ k}, \)

\( R_2 = A_o R_1 = 21.2 \text{ k}, \) and \( R_3 = \frac{1}{4 \times \pi \times (10^4)^2 \times 0.001 \times 10^{-6} \times 0.1 \times 10^{-6} \times 21.2 \times 10^3} = 119.5 \Omega \).

11.4 Higher Order Low-Pass Filters

We wish to consider those higher order filters, in which the transfer function has a denominator polynomial that is of degree \( n \) corresponding to the order of the filter and a numerator polynomial with degree \( m < n \). There are two general methods for realizing these higher order transfer functions. The first is to synthesize the filter around a single active element such as an op-amp. This works well up to about \( n = 3 \), but problems arise for filters of higher order. The second general method is to factor the higher order transfer function \( A(s) \) into first- and second-order transfer functions \( A_1(s) \) and \( A_2(s) \), each of which can be synthesized and then cascaded. This approach has the advantage of simplicity, and the resulting first- and second-order transfer
functions are those already analyzed and used in filter implementation. In this chapter, the factorizing approach is pursued in the development of higher order filters.

Therefore, the approach adopted here in realizing higher order low-pass filters is to cascade first- and/or second-order filters in order to approximate the higher order filter. Thus, in order to realize a fourth-order filter, two second-order filters are cascaded. In order to realize an odd-order filter, at least one first-order must be cascaded with one or more second-order filters. For example, in order to synthesize a third-order filter, one first-order and one second-order filters are cascaded. Similarly, if a fifth-order filter is required, then one first-order and two second-order filters must be cascaded.

The transfer function of one second-order stage is given by

$$A(s) = \frac{A_o}{1 + a_1 (s/\omega_c) + b_1(s/\omega_c)^2}.$$  \hspace{1cm} (11.63)

In a first-order transfer function, the coefficient $b_1$ is zero giving the transfer function

$$A(s) = \frac{A_o}{1 + a_1 (s/\omega_c)}$$  \hspace{1cm} (11.64)

seen earlier. Therefore, the general transfer function representing this cascade of second- and first-order transfer functions is given by

$$A(s) = \frac{A_o}{\prod(i=1) \left(1+a_i(s/\omega_c)+b_i(s/\omega_c)^2\right)} = \frac{A_o}{\left(1+a_1(s/\omega_c)+b_1(s/\omega_c)^2\right)\left(1+a_2(s/\omega_c)+b_2(s/\omega_c)^2\right)\ldots\left(1+a_n(s/\omega_c)+b_n(s/\omega_c)^2\right)}.$$  \hspace{1cm} (11.65)

The multiplication of the factors in the denominator of the transfer function yields an $n$th-order polynomial, where $n$ represents the order of the filter. The filter coefficients $a_i$ and $b_i$ determine the filter characteristics such as Butterworth, Chebyshev, and Bessel, the types being considered in this discussion. These are tabulated in Table 11.1 up to order 10. This cascading of first- and second-order stages is shown diagrammatically in Fig. 11.17 up to the sixth order. As can be
seen, a filter with even order comprises only second-order stages, while a filter with odd order has a first-order stage included.

Fig. 11.17 Cascading first- and second-order stages to realize higher order filters
11.4.1 Third-Order Low-Pass Unity-Gain Filter

In order to develop a third-order unity-gain low-pass filter, we cascade first- and second-order filters such that

\[ A(s) = \frac{A_o}{(1 + a_1 (s/\omega_c)) \left(1 + a_2 (s/\omega_c) + b_2 (s/\omega_c)^2\right)}. \] (11.66)

Note that \( b_1 = 0 \) for the first-order part of the transfer function. For the unity-gain system under consideration, \( A_o = 1 \). Hence, (11.66) can be written as

\[ A(s) = \frac{1}{1 + a_1 (s/\omega_c)} \cdot \frac{1}{\left(1 + a_2 (s/\omega_c) + b_2 (s/\omega_c)^2\right)} \]. (11.67)

The circuit of this system is shown in Fig. 11.18, comprising a unity-gain noninverting first-order system cascaded with a unity-gain noninverting second-order system. The design process is as follows:

![Third-order low-pass unity-gain filter](image)

**Fig. 11.18** Third-order low-pass unity-gain filter

**Partial Filter 1**

The first-order system is

\[ A(s) = \frac{1}{1 + a_1 (s/\omega_c)} \] (11.68)

where \( \omega_c = 2\pi f_c \) is the cut-off frequency. The transfer function for the first-order *noninverting* unity-gain low-pass filter in Fig. 11.19 is given by
Fig. 11.19 First-order low-pass partial filter

Comparing coefficients in (11.68) and (11.69) gives

\[ A_{V2} = -40I_{c3}R_L \]  \hspace{1cm} (11.70)

The design steps are as follows:

1. Select \( C_3 \) usually between 100 pF and 1 \( \mu F \).
2. For the specific type of filter (Butterworth, Chebyshev, and Bessel) and the specific filter requirements, obtain the coefficient \( a_1(b_1 = 0) \) from the relevant table.
3. Determine \( R \) using \( R_3 = a_1/2\pi f_c C \).
4. Set \( R_{os2} = R \) for minimum offset.

Partial Filter 2
The second-order system is

$$A(s) = \frac{A_o}{\left(1 + a_1(s/\omega_c) + b_1(s/\omega_c)^2\right)}.$$  \hspace{1cm} (11.71)

The transfer function for the second-order noninverting unity-gain low-pass filter in Fig. 11.20 is given by

$$A_f = \frac{1}{1 + sC_1(R_1 + R_2) + s^2R_1R_2C_1C_2}.$$  \hspace{1cm} (11.72)

![Second-order low-pass partial filter](image)

**Fig. 11.20** Second-order low-pass partial filter

Comparing coefficients for (11.63) and (11.62) yields

$$\frac{a_1}{\omega_c} = C_1(R_1 + R_2)$$  \hspace{1cm} (11.73)

$$\frac{b_1}{\omega_c^2} = R_1R_2C_1C_2.$$  \hspace{1cm} (11.74)

From this, the design steps are as follows:

1. Select $C_1$ usually between 100 pF and 1 µF.
2. For the specific type of filter (Butterworth, Chebyshev, and Bessel) and the specific filter requirements, obtain the coefficients $a_2$ and $b_2$ from the relevant table.
3. Determine $C_2$ using $C_2 \geq 4b_2C_1/a_2^2$. 
4. Find $R_1$ and $R_2$ using $R_1 = \frac{a_2 + \sqrt{a_2^2 - 4b_2C_1/C_2}}{4\pi f_c C_1}$ and $R_2 = \frac{a_2 + \sqrt{a_2^2 - 4b_2C_1/C_2}}{4\pi f_c C_1}$.

5. Determine $R_{os1} = R_1 + R_2$ for minimum offset voltage.

**Example 11.9** Design a VCVS third-order unity-gain low-pass Butterworth filter with a cut-off frequency of 20 kHz.

**Solution** The design of each of the two partial filters is considered separately.

**Partial Filter 1**
For this case, $f_c = 20$ kHz. Select $C_3 = 1$ nF. From Table 11.1, $a_1 = 1$ and $b_1 = 0$. Hence, $R_3 = a_1/2\pi f_c C_3 = 1/2\pi \times 20 \times 10^3 \times 10^{-9} = 8$ k.

**Partial Filter 2**
For this case, $f_c = 20$ kHz. Select $C_1 = 0.001$ μF. From Table 11.1, $a_2 = 1$ and $b_2 = 1$. Then, $C_2 \geq 4b_2C_1/a_2^2 = 4 \times 1 \times 0.001 \times 10^{-6} = 0.004$ μF. Select $C_2 = 0.005$ μF. Hence, $R_1 = \frac{1 + \sqrt{1 - (4 \times 1 \times 0.001 \times 10^{-6}/0.005 \times 10^{-6})}}{4\pi \times 20 \times 10^3 \times 0.001 \times 10^{-6}} = 5.8$ k and $R_2 = \frac{1 + \sqrt{1 - (4 \times 1 \times 0.001 \times 10^{-6}/0.005 \times 10^{-6})}}{4\pi \times 20 \times 10^3 \times 0.001 \times 10^{-6}} = 2.2$ k. Finally, for minimum offset, $R_{os} = 5.8$ k + 2.2 k = 8 k.

The completed filter is shown in Fig. 11.21.
11.4.1.1 Simplified Design Procedure for Third-Order Low-Pass Unity-Gain Butterworth Filter

A simplified design procedure for the unity-gain third-order Butterworth filter can be developed. Consider the transfer function (11.75) for a low-pass third-order filter:

$$A(s) = \frac{A_o}{(1 + a_1 (s/\omega_c)) (1 + a_2 (s/\omega_c) + b_2 (s/\omega_c)^2)}.$$  \hspace{1cm} (11.75)

For unity gain, $A_o = 1$, and for a Butterworth response from Table 11.1, $a_1 = 1$ and $a_2 = 1, b_2 = 1$. Then, setting $s = j\omega$, (11.10) becomes

$$A = \frac{1}{1 + jf/f_c} \cdot \frac{1}{1 + jf/f_c + (jf/f_c)^2}.$$  \hspace{1cm} (11.76)

This transfer function can be implemented using the configuration shown in Fig. 11.18, which comprises cascaded first- and second-order systems. For this system, the transfer function is given by

$$A_f = \frac{1}{1 + sR_3 C_3} \cdot \frac{1}{1 + sC_1 (R_1 + R_2) + s^2 C_1 C_2 R_1 R_2}.$$  \hspace{1cm} (11.77)

Let $R_1 = R$, $R_2 = R$, $R_3 = R$, $C_1 = C_3/2$, and $C_2 = 2C_3$. Then, Fig. 11.18 becomes Fig. 11.22 and (11.77) becomes

$$A_f = \frac{1}{1 + sRC_3} \cdot \frac{1}{1 + sC_3 R + s^2 (C_3 R)^2} = \frac{1}{1 + jf/f_c} \cdot \frac{1}{1 + jf/f_c + (jf/f_c)^2}.$$  \hspace{1cm} (11.78)
where

\[ f_c = \frac{1}{2\pi RC_3} \]  \hspace{1cm} (11.79)

which is the cut-off frequency. Clearly, the transfer function (11.78) is identical to the transfer function (11.76). Hence, a simplified design procedure for a unity-gain third-order low-pass Butterworth filter is as follows:

1. Choose the desired cut-off frequency \( f_c \).
2. Choose \( C_3 \), usually an available value between about 100 pF and 1 \( \mu F \).
3. Let \( C_1 = C_3/2 \) and \( C_2 = 2C_3 \).
4. Determine \( R \) using \( R = 1/2\pi f_c C_3 \). Set \( R_1 = R_2 = R_3 = R \).

\[ \text{Fig. 11.22} \] Third-order low-pass unity-gain Butterworth filter

**Example 11.10** Using the circuit of Fig. 11.22 and the simplified design procedure, design a third-order low-pass Butterworth filter with a cut-off frequency of 9 kHz.

**Solution** Choose \( C_1 = 0.005 \text{ \( \mu F \)} \) and then \( C_3 = 2C_1 = 0.01 \text{ \( \mu F \)} \) and \( C_2 = 2C_3 = 0.02 \text{ \( \mu F \)} \). Using (11.70),

\[ R = 1/2\pi f_c C_3 = 1/2\pi \times 9 \times 10^3 \times 0.01 \times 10^{-6} = 1.8 \text{ k}. \]

Hence,

\[ R_1 = R_2 = R_3 = 1.8 \text{ k}. \]
**Example 11.11**  Design a VCVS fourth-order unity-gain low-pass Chebyshev filter with a cut-off frequency of 20 kHz and 1-dB ripple width.

**Solution**  The design of each of the two partial filters is considered separately.

**Partial Filter 1**
For this case, \( f_c = 20 \text{ kHz} \). Select \( C_1 = 0.001 \text{ μF} \). From Table 11.2, \( a_1 = 2.5904 \) and \( b_1 = 4.1301 \). Then, \( C_2 \geq 4b_1C_1/a_1^2 = 4 \times 4.1301 \times 0.001 \times 10^{-6}/(2.5904)^2 = 0.0025 \text{ μF} \). Select \( C_2 = 0.005 \text{ μF} \). Hence,

\[
R_1 = \frac{2.5904 + \sqrt{(2.5904)^2 - (4 \times 4.1301 \times 0.001 \times 10^{-6}/0.005 \times 10^{-6})}}{4 \pi \times 20 \times 10^3 \times 0.001 \times 10^{-6}} = 9.9 \text{ kΩ}
\]

and

\[
R_2 = \frac{2.5904 - \sqrt{(2.5904)^2 - (4 \times 4.1301 \times 0.001 \times 10^{-6}/0.005 \times 10^{-6})}}{4 \pi \times 20 \times 10^3 \times 0.001 \times 10^{-6}} = 2.6 \text{ kΩ}
\]

Finally, for minimum offset, \( R_{os} = 9.9 \text{ kΩ} + 2.6 \text{ kΩ} = 12.5 \text{ kΩ} \).

**Partial Filter 2**
For this case, \( f_c = 20 \text{ kHz} \). Select \( C_1 = 0.001 \text{ μF} \). From Table 11.2, \( a_2 = 0.3039 \) and \( b_2 = 1.1697 \). Then, \( C_2 \geq 4b_2C_1/a_2^2 = 4 \times 1.1697 \times 0.001 \times 10^{-6}/(0.3039)^2 = 0.05 \text{ μF} \). Select \( C_2 = 0.1 \text{ μF} \). Hence, \( R_1 = \)

\[
\frac{1.3617 + \sqrt{(1.3617)^2 - (4 \times 0.6180 \times 0.01 \times 10^{-6}/0.02 \times 10^{-6})}}{4 \pi \times 10 \times 10^3 \times 0.01 \times 10^{-6}} = 2 \text{ kΩ}
\]

and \( R_2 = \)

\[
\frac{1.3617 + \sqrt{(1.3617)^2 - (4 \times 0.6180 \times 0.01 \times 10^{-6}/0.02 \times 10^{-6})}}{4 \pi \times 10 \times 10^3 \times 0.01 \times 10^{-6}} = 360 \Omega
\]

Finally, for minimum offset, \( R_{os} = 2 \text{ kΩ} + 360 \Omega = 2360 \Omega \).

The completed filter is shown in Fig. 11.23.
Example 11.12  Design a VCVS fifth-order unity-gain low-pass Butterworth filter with a cut-off frequency of 50 kHz.

Solution  The design of each of the three partial filters is considered separately.

Partial Filter 1  
For this case, \( f_c = 50 \) kHz. Select \( C = 1 \) nF. From Table 11.1, \( a_1 = 1 \) and \( b_1 = 0 \). Hence, \( R = a_1 / 2\pi f_c C = 1 / 2\pi \times 50 \times 10^3 \times 10^{-9} = 3.2 \) k.

Partial Filter 2  
For this case, \( f_c = 50 \) kHz. Select \( C_1 = 820 \) pF. From Table 11.1, \( a_2 = 1.6180 \) and \( b_2 = 1 \). Then,  
\[
C_2 \geq 4b_2C_1/a_2^2 = 4 \times 1 \times 820 \times 10^{-12} / (1.618)^2 = 1.26 \text{ nF}. \text{Select} \\
C_2 = 1.5 \text{ nF}. \text{Hence,} \ R_1 = \frac{1.618 + \sqrt{1.618^2 - (4 \times 1 \times 0.820 \times 10^{-9} / 1.5 \times 10^{-9})}}{4\pi \times 50 \times 10^3 \times 0.820 \times 10^{-9}} = 4.4 \text{ k} \\
\]
and \( R_2 = \frac{1.618 + \sqrt{1.618^2 - (4 \times 1 \times 0.820 \times 10^{-9} / 1.5 \times 10^{-9})}}{4\pi \times 50 \times 10^3 \times 0.820 \times 10^{-9}} = 1.9 \text{ k} \). Finally, for minimum offset, \( R_{os} = 4.4 \text{ k} + 1.9 \text{ k} = 6.3 \text{ k} \).

Partial Filter 3  
For this case, \( f_c = 50 \) kHz. Select \( C_1 = 330 \) pF. From Table 11.1, \( a_3 = 0.6180 \) and \( b_3 = 1 \). Then,
\[ C_2 \geq 4b_3C_1/a_3^2 = 4 \times 1 \times 330 \times 10^{-12}/(0.6180)^2 = 3.5 \text{ nF. Select } C_2 = 4.7 \text{ nF. Hence, } R_1 = \frac{1.618 + \sqrt{(1.618)^2 - (4 \times 1 \times 0.820 \times 10^{-9} / 1.5 \times 10^{-9})}}{4\pi \times 50 \times 10^3 \times 0.820 \times 10^{-9}} = 4.5 \text{ k} \]

and \[ R_2 = \frac{1.618 + \sqrt{(1.618)^2 - (4 \times 1 \times 0.820 \times 10^{-9} / 1.5 \times 10^{-9})}}{4\pi \times 50 \times 10^3 \times 0.820 \times 10^{-9}} = 1.5 \text{ k}. \]

Finally, for minimum offset, \[ R_{os} = 4.5 \text{ k} + 1.5 \text{ k} = 6 \text{ k}. \]

The completed filter is shown in Fig. 11.24.

![Fig. 11.24 Completed fifth-order low-pass filter for Example 11.14](image)

### 11.5 High-Pass First-Order Filter-Butterworth Response

High-pass first-order Butterworth filter response can be generated from low-pass filters by changing resistors to capacitors and capacitors to resistors in the filter network. This corresponds to the transformation \( s \rightarrow 1/s \) or \( j(f/f_c) \rightarrow \frac{1}{j(f/f_c)} \). Thus, the first-order low-pass filter given by \( \frac{1}{1+jf/f_c} \) is transformed such that \( \frac{1}{1+jf/f_c} \rightarrow \frac{1}{1+jf/f_c} = \frac{jf/f_c}{1+jf/f_c} \). A basic first-order high-pass filter is shown in Fig. 11.25a. It employs a \( CR \) network to provide the high-pass filtering, the output of which feeds into a unity-gain buffer. It is obtained from the first-order low-pass filter by interchanging \( R \) and \( C \) in the filter network. A resistor
$R_{OS} = R$ may be included in the feedback loop in order to reduce DC offset at the output as shown in Fig. 11.25b. For the circuit, we have

$$A_f = \frac{V_o(s)}{V_i} = \frac{R}{R + 1/sC} = \frac{sCR}{1 + sCR} = \frac{j f / f_c}{1 + j f / f_c} \quad (11.80)$$

where

$$f_c = 1/2\pi RC. \quad (11.81)$$

![Diagram](image_url)

**Fig. 11.25** High-pass first-order filter

Note that for $f \gg f_c$, $|A_f| \to 1$ and for $f \ll f_c$, $|A_f| \to 0$. The frequency response plot for this circuit is shown in Fig. 11.26, where the cut-off frequency is $f_c = 1/2\pi RC$. At $f = f_c$, the filter transfer function becomes

$$A_f (f_c) = \frac{j f / f_c}{1 + j f / f_c} = \frac{j}{1 + j}. \quad (11.82)$$
First-order high-pass filter response

Hence, \[ |A_f(f_c)| = \left| \frac{j}{1+j} \right| = \frac{1}{\sqrt{2}} = 0.707 = -3 \text{ dB}. \] Thus, at the break frequency \( f = f_c \), the magnitude response falls by 3 dB from its mid-band value, as shown in Fig. 11.26.

**Example 11.13**  Design an \( RC \) high-pass first-order Butterworth filter with a cut-off frequency of 1 kHz.

**Solution**  Choose \( C = 0.01 \mu F \). Then, from (11.81),
\[ R = \frac{1}{2\pi f_c C} = \frac{1}{2\pi \times 10^3 \times 0.01 \times 10^{-6}} = 15.9 \text{ k}. \] Choose \( R_f = R = 15.9 \text{ k} \) for low DC offset.

**11.5.1 First-Order High-Pass Filter with Gain**

The high-pass first-order filter with gain is shown in Fig. 11.27, where the active device is modified to produce a gain greater than unity. The transfer function is given by

\[
A_f = \frac{V_o}{V_i} = \frac{k jf/f_c}{1 + jf/f_c}
\]  \hspace{1cm} (11.83)
where $k = 1 + R_2/R_1$ and $f_c = 1/2\pi RC$. The system has a high-frequency gain of $k = 1 + R_2/R_1$ and a break frequency of $f_c = 1/2\pi RC$. For low DC offset, $R = R_1/R_2$.

![First-order high-pass filter with gain](image)

**Fig. 11.27** First-order high-pass filter with gain

An alternative configuration for a first-order high-pass filter is shown in Fig. 11.28. It is an inverting configuration with a capacitor $C$ in series with the input resistor $R_1$. From Fig. 11.28, we have

$$\frac{V_i}{R_1 + 1/sC} = \frac{-V_o}{R_2}.$$  \hspace{1cm} (11.84)

![Inverting first-order high-pass filter](image)

**Fig. 11.28** Inverting first-order high-pass filter
Hence, the transfer function is given by

\[ A_f = \frac{R_2}{R_1} \cdot \frac{sCR_1}{1 + sCR_1} = -k \frac{jf/f_c}{1 + jf/f_c} \]  

(11.85)

where \( k = R_2/R_1 \) is the gain and

\[ f_c = \frac{1}{2\pi RC_3} \]  

(11.86)

is the break frequency.

**Example 11.14**  Design a first-order high-pass Butterworth noninverting filter using Fig. 11.27 with a gain of 10 and a cut-off of 1 kHz.

**Solution**  Choose \( C = 0.01 \ \mu F \). Then, from (11.86), \( R = 1/2\pi fC \) giving

\[ R = \frac{1}{(2 \times \pi \times 10^3 \times 0.01 \times 10^{-6})} = 15.9 \ \text{k} \]  

Since \( 1 + R_2/R_1 = 10 \) and \( R = R_1/R_2 \), therefore \( R_2 = 159 \ \text{k} \) and \( R_1 = 17.7 \ \text{k} \).

**Design Procedure**

As we did for the low-pass filters, we wish to write down an ordered procedure for designing first-order high-pass filters. Thus, the basic first-order system can be written as

\[ A(s) = \frac{A_\infty}{1 + a_1/(s/\omega_c)} \]  

(11.87)

where \( A_\infty = k \) is the pass-band gain, \( \omega_c = 2\pi f_c \) is the cut-off frequency, and \( a_1 = 1 \) for first-order filters. For higher order filters considered later, the condition \( a_1 \neq 1 \) will arise. Equation (11.87) can be written as

\[ A(s) = \frac{A_\infty s}{s + a_1 \omega_c} \]  

(11.88)

For the first-order noninverting high-pass filter, the transfer function is given by (see earlier)
\[
A_f(s) = \frac{\left(1 + \frac{R_2}{R_1}\right)}{s + 1/RC}.
\]

Comparing coefficients in (11.89) and (11.88) gives

\[
A_\infty = 1 + \frac{R_2}{R_1}
\]  
(11.90)

\[
a_1\omega_c = \frac{1}{RC}.
\]  
(11.91)

The design steps are as follows:

1. Select \( C \) usually between 100 pF and 1 \( \mu F \).
2. Set the coefficient \( a_1 = 1 \).
3. Determine \( R \) using \( R = 1/a_12\pi f_c C \).
4. Select \( R_1 \) and find \( R_2 \) using \( R_2 = R_1(A_\infty - 1) \).

For the first-order inverting low-pass filter, the transfer function is given by (see earlier)

\[
A(s) = -\frac{\frac{R_2}{R_1}s}{s + 1/R_1 C_1}.
\]  
(11.92)

Comparing coefficients in (11.92) with the general transfer function

\[
A(s) = -\frac{A_\infty s}{s + a_1\omega_c}
\]  
(11.93)

gives

\[
A_\infty = \frac{R_2}{R_1}
\]  
(11.94)
The design steps are as follows:

1. Select $C_1$ usually between 100 pF and 1 μF.
2. Set the coefficient $a_1 = 1$.
3. Determine $R_1$ using $R_1 = 1/a_12\pi f_c C_1$.
4. Determine $R_1$ using $R_1 = R_2/A_\infty$.

### 11.6 High-Pass Second-Order Filter

As in the case of second-order low-pass filters, a high-pass filter can be optimized to meet at least one of the following three requirements: (i) maximum flatness in the pass-band; (ii) maximum sharpness in the transition from pass-band to stop-band; and (iii) linear phase response. In order to allow this optimization of the filter, the transfer function must contain complex poles and, hence, for a second-order filter, can take the following form:

$$A(s) = \frac{A_\infty s^2}{s^2 + a_1\omega_c s + b_1\omega_c^2}$$

where $A_\infty$ is the low-frequency gain in the pass-band and $a_1$ and $b_1$ are positive real filter coefficients that define the location of the complex poles of the filter and, hence, the characteristics of the filter. The angular frequency $\omega_c = 2\pi f_c$ represents the cut-off frequency of the filter. This transfer function can be normalized by setting $\omega_c = 1$ giving

$$A(s) = \frac{A_\infty s^2}{s^2 + a_1 s + b_1}.$$  \hfill \text{(11.97)}

Only the Butterworth, Chebyshev, and Bessel responses are considered. These filter responses occur for second (and higher) order
and not for first order where complex poles are not possible, and therefore, all three filter types have identical responses for a first-order high-pass filter. The amplitude responses of first-, second-, and higher order high-pass Butterworth filters using the normalized characteristic are shown in Fig. 11.29. The second-order high-pass filter transfer function (11.97) can be realized around a single active device using two topologies: the Sallen–Key and the multiple feedback.

![Graph showing amplitude responses of filters](image)

**Fig. 11.29** High-pass filter response plots for Butterworth filters

### 11.6.1 Sallen–Key or Voltage-Controlled Voltage Source (VCVS) Topology

The circuit shown in Fig. 11.30 is the VCVS or Sallen–Key implementation of a second-order high-pass unity-gain filter. Comparing this with the second-order low-pass filter, it can be seen that the resistors and capacitors of the filter network are interchanged. Using KCL at nodes A and B, we have

\[
(V_i - V_A) s C_1 = (V_A - V_B) s C_2 + (V_A - V_o) / R_2
\]

and

\[
(V_A - V_B) s C_2 = V_B / R_1
\]
where $V_B = V_o$. These equations yield

$$A(s) = \frac{s^2C_1C_2R_1R_2}{1 + sR_2(C_1 + C_2) + s^2R_1R_2C_1C_2}.$$  \hfill (11.100)

![Second-order high-pass unity-gain filter](image)

**Fig. 11.30** Second-order high-pass unity-gain filter

In order to simplify the development, let $C_1 = C_2 = C$. Then, (11.100) becomes

$$A_f(s) = \frac{s^2}{s^2 + \frac{2}{R_1C}s + \frac{1}{C^2R_1R_2}}.$$  \hfill (11.101)

Comparing coefficients for (11.101) and (11.96) yields

$$A_\infty = 1$$  \hfill (11.102)

$$a_1\omega_c = \frac{2}{R_1C}$$  \hfill (11.103)

$$b_1\omega_c^2 = \frac{1}{R_1R_2C^2}.$$  \hfill (11.104)

From (11.103), we have

$$a_1\omega_c = \frac{2}{R_1C}$$  \hfill (11.105)
and from (11.104), we have

\[ R_2 = \frac{a_1}{b_1 4\pi f_c C}. \]  

(11.106)

We can now state a design procedure for a specific cut-off frequency:

**Design Procedure**

1. Select \( C_1 = C_2 = C \) usually between 100 pF and 1 μF.
2. For the specific type of filter (Butterworth, Chebyshev, and Bessel) and the specific filter requirements, obtain the coefficients \( a_1 \) and \( b_1 \) from the relevant table.
3. Find \( R_1 \) and \( R_2 \) using \( R_1 = \frac{1}{\pi f_c a_1 C} \) and \( R_2 = \frac{a_1}{4\pi f b_1 C} \).
4. Determine \( R_{os} = R_1 \) for minimum offset voltage if required.

**Example 11.15**  Design a VCVS second-order unity-gain high-pass Butterworth filter with a cut-off frequency of 10 kHz.

**Solution**  For this case, \( f_c = 10 \) kHz. Select \( C_1 = C_2 = 0.01 \) μF. From Table 11.1, \( a_1 = \sqrt{2} \) and \( b_1 = 1 \). Then, \( R_1 = \frac{1}{\pi \times 10^3 \times \sqrt{2} \times 0.01 \times 10^{-6}} = 2.3 \) k

and \( R_2 = \frac{\sqrt{2}}{4\pi \times 10^3 \times 0.01 \times 10^{-6}} = 1.1 \) k. Finally, for minimum offset, \( R_{os} = 2.3 \) k.

The system can be designed for gain as shown in Fig. 11.31, where

\[ k = 1 + \frac{R_b}{R_a}. \]  

(11.107)
The process of developing the associated design procedure follows that used for the unity-gain case.

**Example 11.16** Develop a design procedure for the VCVS Butterworth second-order high-pass filter with gain for the special case when $R_1 = R_2$ and $C_1 = C_2$.

**Solution** Using nodal analysis, the transfer function for the filter with gain is given by

$$A_f = \frac{V_o}{V_i} = \frac{k s^2}{s^2 + s \left[ \left( \frac{1}{C_1} + \frac{1}{C_2} \right) + \frac{1}{C_1 R_2} (1 - k) \right] + \frac{1}{R_1 R_2 C_1 C_2}}. \quad (11.108)$$

For the case where $R_1 = R_2 = R$ and $C_1 = C_2 = C$, (11.108) reduces to

$$A_f = \frac{V_o}{V_i} = \frac{k s^2}{s^2 + s \frac{1}{RC} (3 - k) + \frac{1}{R^2 C^2}}. \quad (11.109)$$

Comparing coefficients with

$$A(s) = \frac{A_\infty s^2}{s^2 + a_1 \omega_c s + b_1 \omega_c^2} \quad (11.110)$$

yields

$$\quad (11.111)$$
\[ A_\infty = k \]
\[ a_1/\omega_c = (3 - k) CR \]  \hspace{1cm} (11.112)
\[ b_1\omega_c^2 = R^2 C^2. \]  \hspace{1cm} (11.113)

For a Butterworth filter, \( a_1 = \sqrt{2} \) and \( b_1 = 1 \). Hence, from (11.113), we have
\[ \omega_c = 1/RC, \quad f_c = 1/2\pi RC \]  \hspace{1cm} (11.114)
and from (11.112), we have
\[ \sqrt{2} = 3 - k \]  \hspace{1cm} (11.115)
giving
\[ k = 3 - \sqrt{2} = 1.6. \]  \hspace{1cm} (11.116)

For minimum offset
\[ R = {\overline{R_a/R_b}} = \frac{R_a R_b}{R_a + R_b} = \frac{R_b}{k}. \]  \hspace{1cm} (11.117)

Hence
\[ R_b = kR = 1.6 \ R. \]  \hspace{1cm} (11.118)
Also
\[ A_f = -\frac{R_2}{R_1} \frac{sCR_1}{1 + sCR_1} = -k \frac{jf/f_c}{1 + jf/f_c} \]  \hspace{1cm} (11.119)

Hence
\[ R_a = \frac{kR}{k - 1} = 1.6 \ R/0.6 = 2.7 \ R. \]  \hspace{1cm} (11.120)

We can now state a design procedure for a specific cut-off frequency.
Design Procedure
1. Select $C_1 = C_2 = C$ usually between 100 pF and 1 μF.
2. Determine $R = 1/2\pi f_c C$.
3. Set $R_1 = R_2 = R$.
4. Find $R_a$ and $R_b$ using (11.120) and (11.118).

11.6.1.1 Simplified Design Procedure for Second-Order High-Pass Unity-Gain Butterworth Filter
A simplified design procedure for the unity-gain second-order Butterworth filter can be developed. Consider the transfer function (11.121) for a high-pass second-order filter:

$$A(s) = \frac{A_\infty s^2}{s^2 + a_1 \omega_c s + b_1 \omega_c^2}.$$  \hfill (11.121)

For unity gain, $A_\infty = 1$ and for a Butterworth response from Table 11.1, $a_1 = \sqrt{2}$ and $b_1 = 1$. Then, setting $s = j\omega$, (11.121) becomes

$$A(j\omega) = \frac{(j\omega/f_c)^2}{1 + \sqrt{2}j\omega/f_c + (j\omega/f_c)^2}. \hfill (11.122)$$

The transfer function for a second-order high-pass filter using the VCVS or Sallen–Key topology in Fig. 11.30 is given by

$$A_f = \frac{s^2 C_1 C_2 R_1 R_2}{1 + sR_2 (C_1 + C_2) + s^2 R_1 R_2 C_1 C_2}. \hfill (11.123)$$

In order to obtain the maximally flat Butterworth response, let $C_1 = C_2 = C$, $R_1 = R$, and $R_2 = R/2$. Then, (11.123) reduces to

$$A_f = \frac{s^2 C R^2}{1 + sR (C_1 + C_2) + s^2 R C_1 C_2}. \hfill (11.124)$$
where

\[ f_c = \frac{\sqrt{2}}{2\pi f_c R C}. \tag{11.125} \]

This transfer function is identical to the second-order Butterworth high-pass filter in (11.122). The design procedure is as follows:

1. Determine the desired cut-off frequency \( f_c \).
2. Choose a value of \( C \) between 100 pF and 1 \( \mu \)F.
3. Set \( C_2 = C_1 = C \).
4. Determine \( R \) using \( R = \frac{\sqrt{2}}{2\pi f_c C} \).

**Example 11.17** Using the configuration shown in Fig. 11.30, redesign the second-order high-pass Butterworth filter of Example 11.15 using the simplified approach.

**Solution** For \( f_c = 10 \) kHz, choose \( C_1 = C_2 = 0.01 \) \( \mu \)F. Using (11.125), \( R = \frac{\sqrt{2}}{2\pi} \times 10 \times 10^3 \times 0.01 \times 10^{-6} = 2.3 \) kΩ and hence \( R_1 = 2.3 \) kΩ, \( R_2 = 1.1 \) kΩ, and \( R_{os} = 2.3 \) kΩ.

**Example 11.18** Using \( C_1 = C_2 = 0.1 \) \( \mu \)F, determine the cut-off frequency in the high-pass filter if \( R_1 = 1 \) kΩ and \( R_2 = 500 \) Ω.

**Solution** From Eq. (11.125),

\[ f_c = \frac{\sqrt{2}}{2\pi} \times 10^3 \times 0.1 \times 10^{-6} = 2.3 \) kHz.
Example 11.19  Design a VCVS second-order unity-gain high-pass Chebyshev filter with a cut-off frequency of 10 kHz and a ripple width $RWdB = 1 \text{ dB}$.

Solution  For this case, $f_c = 10 \text{ kHz}$. Select $C_1 = C_2 = 0.001 \mu\text{F}$. From Table 11.2, the coefficients for $RWdB = 1 \text{ dB}$ are $a_1 = 1.3022$ and $b_1 = 1.5515$. Then, from (11.105) and (11.106), $R_1 = \frac{1}{\pi \times 10^3 \times 1.3022 \times 0.001 \times 10^{-6}} = 24 \text{ k}$ and $R_2 = \frac{1.3022}{4 \pi \times 10^3 \times 1.5515 \times 0.001 \times 10^{-6}} = 6.7 \text{ k}$. Finally, for minimum offset, $R_{os} = 24 \text{ k}$.

Example 11.20  Design a VCVS second-order unity-gain high-pass Bessel filter with a cut-off frequency of 10 kHz.

Solution  For this case, $f_c = 10 \text{ kHz}$. Select $C_1 = C_2 = 0.001 \mu\text{F}$. From Table 11.1, the Bessel coefficients are $a_1 = 1.3617$ and $b_1 = 0.6180$. Then, $R_1 = \frac{1}{\pi \times 10^3 \times 1.3022 \times 0.001 \times 10^{-6}} = 23.4 \text{ k}$ and $R_2 = \frac{1.3617}{4 \pi \times 10^3 \times 0.6180 \times 0.001 \times 10^{-6}} = 17.5 \text{ k}$. Finally, for minimum offset, $R_{os} = 23.4 \text{ k}$.

11.6.2 High-Pass Second-Order Multiple Feedback Filter

Another available topology for implementation of second-order high-pass filters is the multiple feedback (MFB) topology shown in Fig. 11.32. In this circuit, the resistors and capacitors are interchanged compared to the corresponding low-pass MFB circuit.
Assuming an ideal op-amp, then for nodes $a$ and $b$,

$$(V_i - V_a) sC_1 = (V_a - V_b) sC_2 + (V_a - V_b) sC_3 + \frac{V_a}{R_1}$$  \hspace{1cm} (11.126)

$$(V_a - V_b) sC_3 = \frac{(V_b - V_o)}{R_2}. \hspace{1cm} (11.127)$$

Noting that $V_b = 0$ because node $b$ is a virtual earth and eliminating $V_a$, we get

$$A_f(s) = -\frac{\frac{C_1}{C_2}s^2}{s^2 + \left(\frac{C_1+C_2+C_3}{R_2C_2C_3}\right)s + \frac{1}{R_1R_2C_2C_3}}. \hspace{1cm} (11.128)$$

For simplicity of the analysis, let $C_1 = C_3 = C$. Then, (11.128) reduces to

$$A_f(s) = -\frac{\frac{C}{C_2}s^2}{s^2 + \left(\frac{2C+C_2}{R_2C_2C}\right)s + \frac{1}{R_1R_2C_2C}}. \hspace{1cm} (11.129)$$

Comparing the coefficients of (11.129) with the general second-order high-pass transfer function

$$A_f(s) = -\frac{\frac{C}{C_2}s^2}{s^2 + \left(\frac{2C+C_2}{R_2C_2C}\right)s + \frac{1}{R_1R_2C_2C}}. \hspace{1cm} (11.130)$$
\[
A(s) = -\frac{A_\infty s^2}{s^2 + a_1\omega_c s + b_1\omega_c^2}
\]

(where a negative sign is introduced to account for the inversion produced by the MFB configuration) yields

\[
A_\infty = \frac{C}{C_2}
\]  \hspace{1cm} (11.131)

\[
a_1\omega_c = \frac{C_2 + 2C}{R_2C_2C}
\]  \hspace{1cm} (11.132)

\[
b_1\omega_c^2 = \frac{1}{R_1R_2C_2C^*}.
\]  \hspace{1cm} (11.133)

Solving for \(R_1\) and \(R_2\) in terms of \(C\) and \(C_2\), we get

\[
R_1 = \frac{a_1}{b_12\pi f_c\left(C_2 + 2C\right)}
\]  \hspace{1cm} (11.134)

\[
R_2 = \frac{(C_2 + 2C)}{a_12\pi f_cC_2C^*}.
\]  \hspace{1cm} (11.135)

**Design Procedure**

1. Select \(C\) usually between 100 pF and 1 µF.

2. Determine \(C_2\) using \(C_2 = C/A_\infty\).

3. For the specific type of filter (Butterworth, Chebyshev, and Bessel) and the specific filter requirements, obtain the coefficients \(a_1\) and \(b_1\) from the relevant table.

4. Find \(R_1\) and \(R_2\) using \(R_1 = \frac{a_1}{b_12\pi f_c(C_2 + 2C)}\) and \(R_2 = \frac{(C_2 + 2C)}{a_12\pi f_cC_2C^*}\).

5. Scale values if necessary.
**Example 11.21**  Design a MFB second-order high-pass Butterworth filter with a gain of 10 and a cut-off frequency of 1 kHz.

**Solution**  For this case, \( f_c = 1 \text{ kHz} \). Select \( C_1 = C_3 = C = 0.01 \mu \text{F} \). Then, \( C_2 = 0.01 \mu \text{F}/10 = 0.001 \mu \text{F} \). From Table 11.1, the Butterworth coefficients are \( a_1 = 1.4142 \) and \( b_1 = 1 \). Then, \( R_1 = \frac{a_1}{b_1 2 \pi f_c (C_2 + 2C)} = \frac{1.4142}{2 \times \pi \times 10^{3} \times (0.001 + 0.02) \times 10^{-6}} = 10.7 \text{ k} \) and \( R_2 = \frac{(C_2 + 2C)}{a_1 2 \pi f_c C_2 C} = \frac{(0.001 + 0.02) \times 10^{-6}}{1.4142 \times 2 \times \pi \times 10^{3} \times 0.001 \times 10^{-6} \times 0.01 \times 10^{-6}} = 236 \text{ k} \).

### 11.7 Higher Order High-Pass Filters

We come now to higher order filters, in which the transfer function has a denominator polynomial that is of degree \( n \). We again use the method of factoring the higher order transfer function \( A(s) \) into first- and second-order transfer functions \( A_1(s) \) and \( A_2(s) \), each of which is then synthesized and cascaded.

The transfer function of one stage is given by

\[
A(s) = \frac{A_\infty s^2}{s^2 + a_1 \omega_c s + b_1 \omega_c^2}.
\]  
(11.136)

In a first-order transfer function, the coefficient \( b_1 \) is zero giving the transfer function

\[
A(s) = \frac{A_\infty s}{s + a_1 \omega_c}.
\]  
(11.137)

Therefore, the general transfer function representing this cascade of second- and first-order transfer functions is given by

\[
A(s) = \frac{A_\infty s}{s + a_1 \omega_c}.
\]  
(11.138)
11.7.1 Third-Order High-Pass Unity-Gain Filter

In order to develop a third-order unity-gain high-pass filter, we cascade first- and second-order filters such that

\[
A(s) = A_\infty \prod_i \frac{s^2}{s^2 + a_i \omega_c s + b_i \omega_c^2}.
\]

(11.139)

Note again that \( b_1 = 0 \) for the first-order part of the transfer function. For the unity-gain system under consideration, \( A_\infty = 1 \). Hence, (11.139) can be written as

\[
A(s) = \frac{s^2}{s + a \omega_c \left( s^2 + a_2 \omega_c s + b_2 \omega_c^2 \right)}.
\]

(11.140)

The circuit of this third-order system is shown in Fig. 11.33. It comprises a unity-gain noninverting first-order system cascaded with a unity-gain noninverting second-order system. The design process is as follows:

**Fig. 11.33** Third-order high-pass filter

**Partial Filter 1**
The first-order system is

\[ A(s) = \frac{s}{s + a_1 \omega_c} \]  

(11.141)

where \( \omega_c = 2\pi f_c \) is the cut-off frequency. The transfer function for the first-order noninverting unity-gain high-pass filter in Fig. 11.33 is given by

\[ A_f(s) = \frac{R_3 C_3 s}{1 + R_3 C_3 s} = \frac{s}{s + 1/R_3 C_3}. \]  

(11.142)

Comparing coefficients in (11.142) and (11.141) gives

\[ a_1 \omega_c = \frac{1}{R_1 C_1}. \]  

(11.143)

The design steps are as follows:

1. Select \( C_3 \) usually between 100 pF and 1 \( \mu \)F.
2. For the specific type of filter (Butterworth, Chebyshev, and Bessel) and the specific filter requirements, obtain the coefficient \( a_1(b_1 = 0) \) from the relevant table.
3. Determine \( R \) using \( R_3 = 1/a_1 2\pi f_c C_3 \).

**Partial Filter 2**

The second-order system is

\[ A(s) = \frac{s^2}{(s^2 + a_2 \omega_c s + b_2 \omega_c^2)}. \]  

(11.144)

The transfer function for the second-order noninverting unity-gain low-pass filter in Fig. 11.33 is given by \((C_1 = C_2 = C)\)

\[ A_f(s) = \frac{s^2}{s^2 + \frac{2}{R_1 C} s + \frac{1}{C^2 R_1 R_2}}. \]  

(11.145)

Comparing coefficients for (11.145) and (11.144) yields
From (11.146), we have
\[ R_1 = \frac{1}{a_1 \pi f_c C} \]  
(11.148)

and from (11.147), we have
\[ R_2 = \frac{a_1}{b_1 4\pi f_c C}. \]  
(11.149)

We can now state a design procedure for a specific cut-off frequency:

**Design Procedure**

1. Select \( C \) usually between 100 pF and 1 \( \mu \)F. Set \( C_1 = C_2 = C \).
2. For the specific type of filter (Butterworth, Chebyshev, and Bessel) and the specific filter requirements, obtain the coefficients \( a_2 \) and \( b_2 \) from the relevant table.
3. Find \( R_1 \) and \( R_2 \) using \( R_1 = \frac{1}{\pi f_c a_1 C} \) and \( R_2 = \frac{a_2}{4\pi f_c b_2 C} \).

**Example 11.22** Design a VCVS third-order unity-gain high-pass Butterworth filter with a cut-off frequency of 20 kHz.

**Solution** The design of each of the two partial filters is considered separately.

**Partial Filter 1**
For this case, \( f_c = 20 \) kHz. Select \( C_3 = 1 \) nF. From Table 11.1, \( a_1 = 1 \) and \( b_1 = 0 \). Hence, \( R_3 = \frac{1}{2\pi f_c a_1 C_3} = \frac{1}{2\pi \times 20 \times 10^3 \times 10^{-9}} = 8 \) k.
Partial Filter 2
For this case, \( f_c = 20 \) kHz. Select \( C = 0.001 \) μF and select \( C_1 = C_2 = C \). From Table 11.1, \( a_2 = 1, b_2 = 1 \). Hence, \( R_1 = \frac{1}{\pi f_c a_2 C} = \frac{1}{\pi \times 20 \times 10^3 \times 0.001 \times 10^{-6}} = 15.9 \) k and \( R_2 = \frac{a_2}{4\pi f_c b_2 C} = \frac{1}{4\pi \times 20 \times 10^3 \times 0.001 \times 10^{-6}} = 4 \) k. The completed filter is shown in Fig. 11.34.

![Solution to Example 11.24](image)

11.7.1.1 Simplified Design Procedure for Third-Order High-Pass Unity-Gain Butterworth Filter
A simplified design procedure for the unity-gain high-pass third-order Butterworth filter can be developed. Consider the transfer function for a high-pass third-order filter:

\[
A(s) = A_\infty \frac{s}{s + a_1 \omega_c} \cdot \frac{s^2}{(s^2 + a_2 \omega_c s + b_2 \omega_c^2)}.
\]

(11.150)

For unity gain, \( A_\infty = 1 \), and for a Butterworth response from Table 11.1, \( a_1 = 1, a_2 = 1, \) and \( b_2 = 1 \). Then, setting \( s = j\omega \), (11.150) becomes

\[
A = \frac{(jf/f_c)^2}{1 + jf/f_c + (jf/f_c)^2} \cdot \frac{jf/f_c}{1 + jf/f_c}
\]

(11.151)

where \( f_c \) is the cut-off frequency. This transfer function can be implemented using the configuration shown in Fig. 11.33, which
comprises cascaded first- and second-order systems. For this system, the transfer function is given by

\[ A_f = \frac{s^2C_1C_2R_1R_2}{1 + sR_2(C_1 + C_2) + s^2C_1C_2R_1R_2} \cdot \frac{sC_3R_3}{1 + sR_3C_3}. \]  

(11.152)

Let \( C_1 = C_2 = C_3 = C, R_1 = 2R_3, \) and \( R_2 = R_3/2. \) Then, (11.152) becomes

\[ A_f = \frac{s^2(CR_3)^2}{1 + sR_3C + s^2(CR_3)^2} \cdot \frac{sCR_3}{1 + jf/f_c + (jhf/f_c)^2} \cdot \frac{jhf/f_c}{1 + jf/f_c} \]  

(11.153)

where

\[ f_c = 1/2\pi RC_3 \]  

(11.154)

which is the cut-off frequency. This transfer function (11.153) is the same as (11.151). We can, therefore, write down a simplified design procedure:

1. Choose the desired cut-off frequency \( f_c. \)
2. Choose \( C, \) usually an available value between about 100 pF and 1 \( \mu F. \) Let \( C_1 = C_2 = C_3 = C. \)
3. Determine \( R_3 \) using \( R_3 = 1/2\pi f_cC. \) Set \( R_1 = 2R_3 \) and \( R_2 = R_3/2. \)

**Example 11.23** Using the simplified design procedure, design a third-order high-pass Butterworth filter with a cut-off frequency of 9 kHz.

**Solution** Choose \( C = 0.01 \mu F \) and then \( C_1 = C_2 = C_3 = 0.01 \mu F. \) Using (11.154), \( R_3 = 1/2\pi f_cC = 1/2\pi \times 9 \times 10^3 \times 0.01 \times 10^{-6} = 1.8 \) k. Hence, \( R_1 = 2R_3 = 3.6 \) k and \( R_2 = R_3/2 = 1.8 \) k/2 = 900 \( \Omega. \)

**Example 11.24** Design a VCVS third-order unity-gain Bessel high-pass filter using Fig. 11.33 with a cut-off frequency of 1 kHz.

**Solution** The design of each of the two partial filters is considered separately.
Partial Filter 1
For this case, \( f_c = 1 \text{ kHz} \). Select \( C_3 = 0.1 \mu \text{F} \). From Table 11.1, \( a_1 = 0.756 \) and \( b_1 = 0 \). Hence,
\[
R_3 = \frac{1}{2\pi f_c a_1 C} = \frac{1}{2\pi \times 10^3 \times 0.756 \times 0.1 \times 10^{-6}} = 2.1 \text{ k}.
\]

Partial Filter 2
For this case, \( f_c = 1 \text{ kHz} \). Select \( C = 0.1 \mu \text{F} \) and select \( C_1 = C_2 = C \). From Table 11.1, \( a_2 = 0.9996 \), \( b_2 = 0.4772 \). Hence,
\[
R_1 = \frac{1}{\pi f_c a_2 C} = \frac{1}{\pi \times 10^3 \times 0.9996 \times 0.1 \times 10^{-6}} = 3.2 \text{ k}
\]
\[
R_2 = \frac{a_2}{4\pi f_c b_2 C} = \frac{0.9996}{4\pi \times 10^3 \times 0.4772 \times 0.1 \times 10^{-6}} = 1.7 \text{ k}.
\]
The completed filter is shown in Fig. 11.35.

![Solution to Example 11.24](image)

**Fig. 11.35** Solution to Example 11.24

### 11.8 Band-Pass Filter
A band-pass filter passes frequencies within a particular frequency band and attenuates all frequencies outside that band. This is shown in Fig. 11.36. This filter has a maximum gain at a frequency \( f_R \) referred to as the resonant or center frequency. The frequencies \( f_L \) and \( f_U \), where the output falls to 0.707 of its maximum value, are the lower cut-off frequency and upper cut-off frequency, respectively. The bandwidth \( B \) is the frequency difference given by
\[
B = f_U - f_L. \quad (11.155)
\]
The relationship between $f_U$, $f_L$, and the resonant frequency $f_R$ is $f_R = \sqrt{f_L f_U}$. Band-pass filters are generally classified as being either narrow-band or wide-band. A narrow-band filter is one having a bandwidth less than one-tenth of the resonant frequency, otherwise the filter is classified as wide-band. The quality factor $Q$ of the circuit is the ratio of resonant frequency to bandwidth given by

$$V_{Bq} \approx V_{RE}$$

(11.156)

It is a measure of the selectivity of the band-pass filter, i.e., its ability to select a specific band of frequencies while rejecting signals outside the band. The higher the $Q$, the more selective the band-pass filter, as shown in Fig. 11.37. From (11.156), $B < 0.1f_R$ is equivalent to $Q > 10$, which corresponds to a narrow-band filter, and $B > 0.1f_R$ is equivalent to $Q < 10$, which corresponds to a wide-band filter.
In general, a band-pass filter can be realized by cascading a low-pass filter and a high-pass filter of the same order and gain with the respective cut-off frequencies suitably separated with appropriate overlap. Such a circuit is shown in Fig. 11.38.

The lower cut-off frequency is set by the high-pass filter, and the upper cut-off frequency is set by the low-pass filter. The pass-band gain will be the gain of each filter and will be constant for a band of frequencies. The roll-off rate on each side of the frequency response characteristic would be determined by the order of the filters. In the
case of first-order filters, the low-pass and high-pass filters can be combined in an inverting amplifier, as shown in Fig. 11.39.

![Inverting Amplifier Diagram](image)

**Fig. 11.39** Band-pass filter using combined first-order filters

In narrow-band filters, \( B < 0.1f_R \). This type of filter has a general second-order transfer function given by

\[
\frac{V_o}{V_i} = \frac{s\omega_o G}{s^2 + s\frac{\omega_o}{Q} + \omega_0^2}
\]

(11.157)

where \( \omega_o \) is the center frequency, \( G \) is the center frequency gain, and \( Q \) is the quality factor. There are several topologies that can be used to implement this transfer function, including the Sallen–Key, multiple feedback, and Wien.

### 11.8.1 Sallen–Key Band-Pass Filter

The circuit shown in Fig. 11.40 is a second-order Sallen–Key (VCVS) band-pass filter. Node analysis at \( A \) and \( B \) yields the equations.

\[
V_A \left( \frac{1}{R_1} + \frac{1}{R_2} + s(C_1 + C_2) \right) = \frac{V_i}{R_1} + sC_2 V_B + \frac{V_o}{R_2}
\]

(11.158)

\[
V_B \left( \frac{1}{R_3} + sC_2 \right) = sC_2 V_A
\]

(11.159)

\[
(11.160)
\]
\[ V_B = \frac{V_o}{k} \]

where

\[ k = 1 + \frac{R_b}{R_a}. \]  \hspace{1cm} (11.161)

This gives

\[ \frac{V_o(s)}{V_i(s)} = \frac{\frac{k}{C_1R_1}S}{s^2 + s\left(\frac{1}{R_1} + \frac{1}{R_3} + \frac{1}{R_2} (1 - k) + \frac{C_1}{C_2R_3}\right) + \frac{R_1 + R_2}{C_1C_2R_1R_2R_3}}. \]  \hspace{1cm} (11.162)

Let \( C_1 = C_2 = C, R_1 = R_2 = R, \) and \( R_3 = 2R. \) Then, (11.162) reduces to

\[ \frac{V_o(s)}{V_i(s)} = \frac{\frac{k}{CR}S}{s^2 + s\left(\frac{3-k}{RC} + \frac{1}{C^2R^2}\right)}. \]  \hspace{1cm} (11.163)

Comparing coefficients in (11.163) and (11.157) yields

\[ \omega_o^2 = \frac{1}{R^2C^2} \]  \hspace{1cm} (11.164)

\[ \omega_o^2 = \frac{1}{R^2C^2} \]  \hspace{1cm} (11.165)
From this, we have

\[
\frac{\omega_o}{Q} = \frac{3 - k}{RC}
\]

\[
\frac{G\omega_o}{Q} = \frac{k}{RC}
\]

(11.166)

In the design process, a value of \( C \) is selected, and then, using (11.167), \( R \) is determined for a given \( f_o \). Following this, either a particular \( Q \) using (11.168) or \( G \) using (11.169) can be designed for by selecting \( k \). Note that as \( Q \) increases, the value of \( 3 - k \) becomes smaller indicating that \( k \) approaches \( 3(k < 3) \), and hence, the circuit gain \( G \) in (11.169) changes.

**Example 11.25** Design a Sallen–Key second-order band-pass filter with a center frequency of 5 kHz and a quality factor of 5.

**Solution** We select \( C = 0.01 \mu F \). Then, using (11.167),

\[
R = \frac{1}{2\pi \times 5 \times 10^3 \times 0.01 \times 10^{-6}} = 3.2 \text{ k}
\]

Using (11.168), for \( Q = 5 \), we have \( k = 3 - 1/Q = 3 - 1/5 = 2.8 \). Since \( k = 1 + R_b/R_a \), for \( R_a = 1 \text{ k} \), then \( R_b = 1.8 \text{ k} \). Note that the resulting value for \( G \) using (11.169) is \( G = 2.8/(3-2.8) = 14 \).

Thus, this design process allows designing for a particular \( f_o \) and either \( Q \) or \( G \). If greater design freedom is desirable for specified values of \( f_o \), \( Q \) and \( G \), then the conditions \( C_1 = C_2 = C \) and \( R_1 = R_2 = R, R_3 = 2R \) would need to be relaxed.
11.8.2 Multiple Feedback Band-Pass Filter

A simple circuit to implement the band-pass transfer function is shown in Fig. 11.41. It is a multiple feedback configuration referred to as the Delyiannis–Friend circuit. Setting the capacitor values equal such that \( C_1 = C_2 = C \) simplifies the analysis without compromising the filter. The node equations are given by

\[
\frac{V_i - V_A}{R_1} = \frac{V_A}{R_2} + (V_A - V_o) sC + V_A sC
\]

\[
Z_i = \frac{V_i}{I_b} = h_{ie}.
\]

Eliminating \( V_A \) yields

\[
\frac{V_o}{V_i} = -\frac{\frac{s}{CR_1}}{s^2 + \frac{2s}{CR_3} + \frac{R_1 + R_2}{C^2R_1R_2R_3}}. \quad (11.172)
\]

Comparing terms in (11.172) and

\[
\frac{V_o}{V_i} = -\frac{s\omega_o G}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2}. \quad (11.173)
\]
yields

$$\omega_o = \frac{1}{C \sqrt{R_1//R_2.R_3}}, f_o = \frac{1}{2\pi C \sqrt{R_1//R_2.R_3}}$$  \hspace{1cm} (11.174)$$

$$Q = \frac{1}{2} \sqrt{\frac{R_3}{R_1//R_2}}$$ \hspace{1cm} (11.175)$$

$$G = \frac{1}{2} \frac{R_3}{R_1}.$$ \hspace{1cm} (11.176)$$

Solving for $R_1, R_2,$ and $R_3$ yields

$$BW_p = \frac{SR}{2\pi V_a}.$$ \hspace{1cm} (11.177)$$

$$R_3 = \frac{2Q}{\omega_C}.$$ \hspace{1cm} (11.178)$$

$$G_2 = \frac{1}{R_2} = 4\pi f_o C Q \left(1 - \frac{G}{2Q^2}\right)$$ \hspace{1cm} (11.179)$$

where $G_2$ is the conductance. This must be positive, and therefore, the following realizability condition must be satisfied:

$$\left(1 - \frac{G}{2Q^2}\right) \geq 0 \Rightarrow \frac{G}{2Q^2} \leq 1.$$ \hspace{1cm} (11.180)$$

If the realizability condition is satisfied such that $G/2Q^2 = 1$, then $G_2 = 0$, which means $R_2 \to \infty$ (open circuit). In these circumstances, resistor $R_2$ is removed from the circuit.

**Example 11.26** Design a second-order MFB band-pass filter with $f_0 = 1$ kHz, $Q = 7$, and $G = 10$. 


Solution Checking the realizability condition, we have
\[ G/2Q^2 = 10/2 \times 7^2 = 0.1 < 1. \] Hence, the condition is satisfied. Select \( C_1 = C_2 = C = 0.01 \ \mu F. \) Then

\[
R_1 = \frac{Q}{2\pi f_0 GC} = \frac{7/2 \times 10^3 \times 10 \times 0.01 \times 10^{-6}}{11.1 \ k}
\]

\[
\eta = \frac{P_L}{P_{CC}} \times 100 = \frac{1}{2} \left( \frac{1}{\pi} \right) I_{C_{max}} R_L \times 100 = \frac{\pi I_{C_{max}} R_L}{4 V_{CC}} \times 100
\]

\[
R_2 = 1/4\pi f_0 C Q \left( 1 - \frac{G}{2Q^2} \right) = 1/4\pi \times 10^3 \times 0.01 \times 10^{-6} \times 7 \times (1 - 0.1) = 1.1 \ k.
\]

(In the case where the center frequency gain \( G \) is not specified, then \( G \) can be selected to ensure that the realizability condition is satisfied with equality. Then, resistor \( R_2 \) can be removed from the circuit.) If the realizability condition is not met, then the requirement \( C_1 = C_2 \) would have to be relaxed.

11.8.3 Wien Band-Pass Filter

A third band-pass filter is shown in Fig. 11.42. It utilizes a Wien network, which has a band-pass response. At \( f_o = 1/2\pi RC \), the output of the network is at a maximum of \( 1/3 \) of the input voltage. By placing this network in a positive feedback loop, the band-pass response is sharpened. The transfer function is given by

![Wien band-pass filter](image.png)

*Fig. 11.42* Wien band-pass filter
\[ \frac{V_o}{V_i} = \frac{\alpha \frac{R_2}{R_1} \omega_o s}{s^2 + \left(3 - \alpha \frac{R_2}{R_1}\right) \omega_o s + \omega_o^2} \]  \hspace{1cm} (11.181)

where

\[ \omega_o = \frac{1}{RC}, \quad f_o = \frac{1}{2\pi RC} \]  \hspace{1cm} (11.182)

\[ Q = \frac{1}{3 - \alpha \frac{R_2}{R_3}} \]  \hspace{1cm} (11.183)

\[ I_D \approx I_o e^{\frac{V_D}{mV_T}} \]  \hspace{1cm} (11.184)

In designing this filter, \( C \) is first chosen, and then, \( R \) is selected to achieve the desired center frequency using (11.182). Following this, \( R_2, \) \( R_3, \) and \( \alpha \) are determined to give the desired \( Q \) using (11.183), and then, \( R_1 \) is adjusted to give the desired center frequency gain using (11.184). This procedure is called orthogonal tuning.

**Example 11.27**  Design a second-order Wien band-pass filter with \( f_0 = 1 \) kHz, \( Q = 7, \) and \( G = 10.\)

**Solution**  Select \( C = 0.01 \) \( \mu \)F and then

\[ R = \frac{1}{2\pi} \times 10^3 \times 0.01 \times 10^{-6} = 15.9 \text{ k} \text{.} \]  

To get the specified \( Q, \) choosing \( \alpha = 1 \) in (11.183) gives

\[ 7 = \frac{1}{3 - \alpha \frac{R_2}{R_3}} \Rightarrow \frac{R_2}{R_3} = \frac{1}{7 - 1} = \frac{1}{6} \]

Selecting \( R_3 = 10 \text{ k} \text{,} \) we get \( R_2 = 8.6 \text{ k} \text{.} \)

Finally, using (11.184), in order to achieve the desired gain, we get

\[ 10 = \frac{8.6 \times k}{R_1} \times 7 \]

which yields \( R_1 = 6 \text{ k} \text{.} \)

---

**11.9 Band-Stop Filter**

The general transfer function of a second-order band-stop or notch filter is given by
where \( \omega_o = 2\pi f_o \) is the notch frequency and \( Q \) is the quality factor. The normalized response for this filter is shown in Fig. 11.43 for varying values of \( Q \).

![Normalized band-stop filter response for varying values of Q](image)

**Fig. 11.43** Normalized band-stop filter response for varying values of \( Q \)

### 11.9.1 Twin-T Notch Filter

A very popular notch filter is the twin-T circuit shown in Fig. 11.44. It utilizes a twin-T network at the input to create the notch at frequency \( f_o \) and sharpens the notch with positive feedback. The feedback here is applied to both legs of the T network, and the level of this feedback is adjustable with the potential divider \( R_1, R_2 \). Both op-amps provide buffering. The transfer function is given by

\[
\frac{V_o}{V_i} = \frac{s^2 + \omega_o^2}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2}
\]  

where.
With this notch filter, $Q$s up to about 50 are achievable.

**Example 11.29** Using the circuit in Fig. 11.44, design a twin-T notch filter to have a notch frequency of 60 Hz and a $Q$ of 20.

**Solution** Select $C = 1 \mu F$. Then, using (11.187),

$$R = \frac{1}{2 \pi \times 60 \times 10^{-6}} = 2.7 \, k.$$ Using (11.188), $20 = \frac{1}{4} \times (1 - \rho)$, from which $\rho = 0.9875$. From (11.189) with $R_1 = 10 \, k$, then $R_2 = 127 \, \Omega$.

**11.9.2 Wien Notch Filter**

The notch filter shown in Fig. 11.45 is easier to tune than the twin-T filter, and higher $Q$s can be achieved. It utilizes the Wien network in a feedback loop to increase $Q$. The transfer function is given by (11.190)
\[
\frac{V_o}{V_i} = k \frac{s^2 + \omega_o^2}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2}
\]

where

\[
\omega_o = \frac{1}{RC}, f_o = \frac{1}{2\pi RC}
\]  

(11.191)

\[
Q = \frac{1}{3} \left( 1 + \frac{R_2}{R_3} \right)
\]  

(11.192)

\[
k = -\frac{R_2/\parallel R_3}{R_1}
\]  

(11.193)

and \(k\) is the low-frequency gain. Thus, \(R\) and \(C\) are selected to give a particular notch frequency, and \(R_2\) and \(R_3\) are selected to give the desired \(Q\) after which \(R_1\) is chosen to achieve a particular gain.

\textbf{Fig. 11.45}  Wien notch filter

\textbf{Example 11.30}  Using the circuit in Fig. 11.45, design a Wien notch filter to have a notch frequency of 60 Hz, a \(Q\) of 20, and a gain of 10.
Solution Select \( C = 1 \, \mu \text{F} \). Then, using (11.191),
\[
R = \frac{1}{2\pi} \times 60 \times 10^{-6} = 2.7 \, \text{k}.
\]
Using (11.192),
\[
20 = \frac{1}{3} \left( 1 + \frac{R_2}{R_3} \right),
\]
and therefore, for \( R_3 = 10 \, \text{k} \), \( R_2 = 590 \, \text{k} \). From (11.193) and noting that \( R_2/R_3 = 9.8 \, \text{k} \), we have
\[
10 = \frac{R_2/R_3}{R_1} = 9.8 \frac{\text{k}}{R_1}.
\]
Hence, \( R_1 = 980 \, \Omega \).

11.10 All-Pass Filters

An all-pass filter is one in which the output signal amplitude is constant for all frequencies but whose phase varies with frequency. Because of these properties, all-pass filters are used to correct spurious signal phase shifts and to introduce signal delay. The all-pass filter needs to have a constant group delay over the relevant frequency band, in order that transmitted signal suffer minimum distortion. The group delay refers to the time by which signal frequencies within the band are delayed. It is defined as
\[
t_{gr} = -\frac{d\phi}{d\omega} \tag{11.194}
\]
where \( \phi \) is the phase difference between output and input.

11.10.1 First-Order All-Pass Filter

The transfer function of a first-order all-pass filter is given by
\[
\frac{V_o(s)}{V_i} = \frac{1 - s/\omega_0}{1 + s/\omega_0} \tag{11.195}
\]

The amplitude response is given by
\[
\left| \frac{V_o}{V_i} \right| = \left| \frac{1 - s/\omega_0}{1 + s/\omega_0} \right| = \frac{\sqrt{1 + (\omega/\omega_0)^2}}{\sqrt{1 + (\omega/\omega_0)^2}} = 1 \tag{11.196}
\]
which is constant for all frequencies. Note that at low frequencies,
The phase response is given by

\[
\angle \left( \frac{V_o}{V_i} \right) = \angle (1 - s/\omega_o) - \angle (1 + s/\omega_o) = -\tan^{-1}(\omega/\omega_o) - \tan^{-1}(\omega/\omega_o) = -2\tan^{-1}(\omega/\omega_o).
\]  

(11.198)

This system produces zero phase at low frequencies with no inversion and \(-180^\circ\) at high frequencies. The magnitude and phase responses are shown in Fig. 11.46. At \(f = f_o\), \(\angle(V_o/V_i) = -90^\circ\). Using (11.194), the group delay produced by this filter is given by

\[
t_{gr} = -\frac{d\phi}{d\omega} = -\frac{d}{d\omega} \left(-2\tan^{-1}(\omega/\omega_o)\right) = \frac{1/\pi f_o}{1 + (f/f_o)^2}.
\]  

(11.199)

![Magnitude and phase response of first-order all-pass filter](image)

**Fig. 11.46** Magnitude and phase response of first-order all-pass filter

This has a value

\[
t_{gr} = 1/\pi f_o, \quad f \ll f_o
\]  

(11.200)

which is the maximum group delay occurring at low frequencies. A plot of \(t_{gr}\) against \(f\) is shown in Fig. 11.47.
11.10.2 First-Order All-Pass Filter Realization

A first-order all-pass filter which produces this response is shown in Fig. 11.48. It is based on a single op-amp with negative feedback to the inverting terminal but where the noninverting terminal is fed through an $RC$ network. For this system at the noninverting terminal,

$$V_A = \frac{1/sC}{R + 1/sC} V_i = \frac{1}{1 + sCR} V_i.$$  (11.201)
Noting that at the two input terminals, \( V_A = V_B \), we have

\[
P_D > V_Z \frac{V_{i_{\text{max}}} - V_Z}{R}
\]

Therefore

\[
\frac{V_o}{V_i} = \frac{1 - sCR}{1 + sCR}.
\]

This is the transfer function of an all-pass lag network with

\[
V_{BB} = I_B R_B + V_{BE} + I_C R_E
\]

The amplitude response is given by

\[
\left| \frac{V_o}{V_i} \right| = \left| \frac{1 - sCR}{1 + sCR} \right| = \frac{\sqrt{1 + (\omega CR)^2}}{\sqrt{1 + (\omega CR)^2}} = 1
\]

which is constant for all frequencies. The phase angle \( \phi \) is given by

\[
\phi = \arg\left( \frac{V_o}{V_i} \right) = \arg(1 - sCR) - \arg(1 + sCR)
\]

\[
= -\tan^{-1}(\omega CR) - \tan^{-1}(\omega RC)
\]

\[
= -2\tan^{-1}(\omega RC).
\]

This system produces zero phase at low frequencies with no inversion and \(-180^\circ\) at high frequencies. At \( f = f_0 = 1/2\pi RC \), \( \phi = -90^\circ \). If resistor \( R \) is made variable, then the phase of the output signal relative to the input can be continuously varied.

**Example 11.31** Design a first-order all-pass filter with a \( 45^\circ \) phase lag at \( f = 1 \text{ kHz} \).

**Solution** For a phase lag of \( 45^\circ \), \( \phi = -45^\circ \). From equation (11.205),

\[
R = \frac{\tan(-\phi/2)}{2\pi f C}.
\]

Choose \( C = 0.01 \text{ \mu F} \). Then,

\[
R = \frac{\tan(45^\circ/2)}{2\pi \times 10^3 \times 0.01 \times 10^{-6}} = 6.6 \text{ k}.
\]

Choose \( R_A = 10 \text{ k} \).
**Example 11.32** Determine the phase shift that this circuit will produce for a signal of frequency $f = 5 \text{ kHz}$.

**Solution** From Eq. (11.205),

$$\phi = -2\tan^{-1}2\pi f RC = -2\tan^{-1} \left(2 \times \pi \times 5 \times 10^3 \times 6.6 \times 10^3 \times 0.01 \times 10^{-6}\right) = -128.5^\circ.$$

Using (11.194), the group delay produced by this filter is given by

$$t_{gr} = -\frac{d\phi}{d\omega} = -\frac{d}{d\omega} \left(-2\tan^{-1}\omega RC\right) = 2\frac{RC}{1 + \omega^2 R^2 C^2}.$$  

This has a value $t_{gr} = 2RC$, $\omega \ll 1/RC$, which is the maximum group delay occurring at low frequencies.

A first-order all-pass filter, which produces a lead in the phase is shown in Fig. 11.49. In this circuit, $R$ and $C$ are interchanged as compared to the first-order all-pass lag circuit. For this circuit

$$V_A = \frac{R}{R + 1/sC} V_i = \frac{sCR}{1 + sCR} V_i.$$  

(11.207)

**Fig. 11.49** First-order all-pass filter (lead)

Noting that at the two input terminals, $V_A = V_B$, we have

$$P_D > V_Z \frac{V_{i_{max}} - V_Z}{R}.$$  

(11.208)
Therefore
\[
\frac{V_o}{V_i} = \frac{-(1 - sCR)}{1 + sCR}.
\] (11.209)

This is the transfer function of an all-pass lead network. At low frequencies,
\[
\frac{V_o}{V_i} \text{ (DC)} = -1.
\] (11.210)

The amplitude response is given by
\[
\left| \frac{V_o}{V_i} \right| = \left| \frac{-(1 - sCR)}{1 + sCR} \right| = \frac{\sqrt{1 + (\omega CR)^2}}{\sqrt{1 + (\omega CR)^2}} = 1
\] (11.211)

which is constant for all frequencies. The phase angle $\phi$ is given by
\[
\phi = \angle \left( \frac{V_o}{V_i} \right) = \angle (-1) + \angle (1 - sCR) - \angle (1 + sCR)
\]
\[
= 180^\circ - \tan^{-1}(\omega RC) - \tan^{-1}(\omega RC)
\]
\[
= 180^\circ - 2\tan^{-1}(\omega RC).
\] (11.212)

This system produces $180^\circ$ phase shift at low frequencies, which is inversion and zero phase shift at high frequencies. At $f = f_o = 1/2\pi RC$, $\Delta(V_o/V_i) = +90^\circ$.

**Example 11.33** Design a first-order all pass filter with a $60^\circ$ phase lead at $f = 1$ kHz.

**Solution** For a phase lead of $60^\circ$, $\phi = +60^\circ$. From Eq. (11.212),
\[
R = \frac{\tan[(180^\circ - \phi)/2]}{2\pi fC}
\]

Choose $C = 0.01$ $\mu$F. Then,
\[
R = \frac{\tan[(180^\circ - 60^\circ)/2]}{2\pi \times 10^3 \times 0.01 \times 10^{-6}} = 27.6$ k.

Choose $R_A = 10$ k.
**Example 11.34** Determine the phase shift that this circuit will produce for a signal of frequency \( f = 2 \) kHz.

**Solution** From Eq. (11.212),
\[
\phi = 180^\circ - 2\tan^{-1}(2\pi f RC) = 180^\circ - 2\tan^{-1}\left(2 \times \pi \times 2 \times 10^3 \times 27.6 \times 10^3 \times 0.01 \times 10^{-6}\right) = 32^\circ.
\]

### 11.11 State Variable Filter

The state variable filter also called the Kerwin, Huelsman, Newcomb filter is another versatile filter realization. Because of its great flexibility, its good performance and low sensitivity to component variation, it is one of the most widely used active filters. The filter name arises from the state variable method used to solve differential equations that is used here to develop the filter topology. In outlining the method, consider the second-order low-pass transfer function
\[
\frac{V_o}{V_i} = \frac{1}{s^2 + a_1 s + a_o}.
\]  

(11.213)

In this equation, an arbitrary function \( X(s)/s^2 \) is introduced such that (11.213) becomes
\[
\frac{V_o}{V_i} = \frac{\frac{X(s)}{s^2}}{\frac{X(s)}{s^2} (s^2 + a_1 s + a_o)} = \frac{\frac{X(s)}{s^2}}{X(s) + a_1 \frac{X(s)}{s} + a_o \frac{X(s)}{s^2}}.
\]  

(11.214)

Equating numerator and denominator, we get
\[
V_o = \frac{X(s)}{s^2}
\]  

(11.215)

and
\[
V_i = X(s) + a_1 \frac{X(s)}{s} + a_o \frac{X(s)}{s^2}.
\]  

(11.216)

Expressing (11.215) and (11.216) in the time domain (by taking the inverse Laplace transform) yields
\[
(11.217)
where the quantities \( x(t), \int x(t) dt, \) and \( \int (\int x(t) dt) dt \) are referred to as state variables and hence the name of the filter. A block diagram of this system is shown in Fig. 11.50, and an implementation of this using op-amps is shown in Fig. 11.51. Here, op-amp 1 provides the summing action, while op-amp 2 and op-amp 3 are used as integrators. For this system, the output \( V_{o3} \) of op-amp 3 represents the low-pass output \( V_o \), as given in (11.213), i.e., \( V_{o3} = V_o = V_{LP} \). Also, the output \( V_{o2} \) of op-amp 2 is \( V_{o2} = -sV_{o3} = -V_{BP} \), and the output \( V_{o1} \) of op-amp 1 is \( V_{o1} = -sV_{o2} = V_{HP} \). The actual transfer functions are given by setting \( R_4 = R_5 = R, C_1 = C_2 = C, \) and \( R_2 = R_3 = R_x \); then.

\[
\frac{V_{HP}}{V_i} = \frac{-\frac{R_5}{R_1}S^2}{S^2 + \frac{R_7(2R_1+R_x)}{CRR_1(R_6+R_7)}S + \frac{1}{C^2R^2}} \quad (11.219)
\]

of general form

\[
\frac{V_{HP}}{V_i} = -\frac{kS^2}{S^2 + S\omega_0/Q + \omega_o^2} \quad (11.220)
\]

\[
\frac{V_{BP}}{V_i} = \frac{\frac{R_5}{R_1}1CRS}{S^2 + \frac{R_7(2R_1+R_x)}{CRR_1(R_6+R_7)}S + \frac{1}{C^2R^2}} \quad (11.221)
\]

of general form

\[
\frac{V_{BP}}{V_i} = \frac{s\omega_0G}{S^2 + S\omega_0/Q + \omega_o^2} \quad (11.222)
\]

\[
\frac{V_{BP}}{V_i} = \frac{s\omega_0G}{S^2 + S\omega_0/Q + \omega_o^2} \quad (11.223)
\]
of general form

\[
\frac{V_{LP}}{V_i} = \frac{\frac{R_2}{R_1} \frac{1}{C^2 R^2}}{s^2 + \frac{R_7(2R_1+R_2)}{CRR_1(R_6+R_7)} s + \frac{1}{C^2 R^2}}.
\]

(11.224)

\[\frac{V_{LP}}{V_i} = -\frac{k\omega_o^2}{s^2 + s\omega_o/Q + \omega_o^2}.\]

**Fig. 11.50** Block diagram of the state variable filter system

**Fig. 11.51** Circuit implementation of the state variable filter system

From these, for \(\beta = R_7/(R_6 + R_7)\),

\[f_0 = \frac{1}{2\pi RC}\]

(11.225)
Using the state variable filter, design a band-pass filter with a center frequency \( f_0 = 10 \text{ kHz} \), a quality factor \( Q = 50 \), and a center frequency gain \( G = 10 \).

**Solution**  
Choosing \( C = 0.001 \mu F \), then  
\[
R = \frac{1}{2\pi} \times 10 \times 10^3 \times 0.001 \times 10^{-6} = 15.9 \text{ k\Omega}.
\]
\( G = kQ \) giving \( 10 = 50k \) from which \( k = 1/5 \). This yields \( R_x = 10 \text{ k\Omega} \) and \( R_1 = 50 \text{ k\Omega} \). Finally,  
\[
Q = \frac{1}{\beta(2+k)},
\]
which becomes \( 50 = \frac{1}{\beta(2+0.2)} \), which yields \( \beta = 1/110 \). For \( R_7 = 1 \text{ k\Omega} \), then \( R_6 = 109 \text{ k\Omega} \).

### 11.11.1 Modified State Variable Filter

We wish to exploit the excellent summing properties of the virtual earth of an op-amp in the inverting configuration. Thus, in the state variable filter configuration in Fig. 11.50, instead of adding the term \(-a_1 \int x(t)dt\) derived from the band-pass output at the noninverting terminal of the op-amp, the term \(- \int x(t)dt\) is inverted (sign changed) using an inverting amplifier and the term \(a_1 \int x(t)dt\) added at the inverting terminal using the normal summing process via the virtual earth. The resulting modified block diagram is shown in Fig. 11.52, and the modified circuit is shown in Fig. 11.53.
The inverting amplifier is op-amp 4 with the output signal being applied to the virtual earth of the input op-amp 1 via $R_6$. This modified topology achieves the same results as the original circuit. However, the presence of op-amp 4 allows the input to be moved from op-amp 1 to op-amp 4 such that the notch filter response becomes available at the output of op-amp 4. This is so since, in general, $V_i - V_{BP} = V_N$ with the summing action resulting in $-V_N$. The fully redrawn circuit is shown in Fig. 11.54 and may be considered a universal filter as it provides band-
stop, high-pass, band-pass, and low-pass outputs. Moreover, the availability of quad op-amp packages such as the LM148 series or the superior OPA4134 facilitates the implementation of this system.

Fig. 11.54 Universal filter

For this system, the transfer functions are as follows:

\[
\frac{V_N}{V_i} = \frac{-\frac{R_1}{VR_1} \left( s^2 + \frac{1}{VR_3^2C^2} \right)}{s^2 + \frac{R_2}{VR_2VR_3C}s + \frac{1}{VR_3^2C^2}}
\]

(11.229)

\[
\frac{V_{HP}}{V_i} = \frac{\frac{R_1R_2}{VR_1VR_2} s^2}{s^2 + \frac{R_2}{VR_2VR_3C}s + \frac{1}{VR_3^2C^2}}
\]

(11.230)

\[
\frac{V_{BP}}{V_i} = \frac{-\frac{R_1R_2}{VR_1VR_2} \frac{1}{CVR_3} s}{s^2 + \frac{R_2}{VR_2VR_3C}s + \frac{1}{VR_3^2C^2}}
\]

(11.231)

\[
\frac{V_{LP}}{V_i} = \frac{\frac{R_1R_2}{VR_1VR_2} \frac{C^2VR_3^2}{s^2 + \frac{R_2}{VR_2VR_3C}s + \frac{1}{VR_3^2C^2}}}{VR_1VR_2 C^2VR_3^2}
\]

(11.232)

For this system,
From these equations, it can be seen that $f_o$ is continuously variable using a variable resistor for $VR_3$, $Q$ is continuously variable using a variable resistor for $VR_2$, and $G$ is variable using a variable resistor for $VR_1$.

**Example 11.35**  Design a universal filter with a cut-off frequency of 20 kHz, a quality factor of 100, and a center frequency gain of 10.

**Solution**  Using Eq. (11.233) and choosing $C = 0.001 \, \mu F$, we get $VR_3 = 7957 \, \Omega$. For $Q = 100$ from Eq. (11.234), we get $VR_2 = 100 \, k$ and $R_2 = 1 \, k$. Finally, for $G = 10$ from Eq. (11.235), we have $VR_1 = 10 \, k$ and $R_1 = 100 \, k$.

### 11.12 Biquadratic Filters

Biquadratic filters are a class of filters whose general transfer function can be represented as the ratio of two quadratic expressions. These filters are stable and easily tuned. They, like the state variable filters, generally require more components than the other filter circuits discussed previously but they can produce higher $Q$ factors than those filters.

Consider the general transfer function of a second-order high-pass filter given by
\[
\frac{V_o(s)}{V_i(s)} = \frac{-ks^2}{s^2 + \frac{\omega_o}{Q} s + \omega_o^2}
\]  \hspace{1cm} (11.237)

For simplicity, the normalized transfer function with \(\omega_o = 1\) is used. This may be written as
\[
\frac{V_o(s)}{V_i(s)} = \frac{-k}{1 + \frac{1}{Qs} + \frac{1}{s^2}} \cdot \frac{M}{k}
\]  \hspace{1cm} (11.238)

where
\[
V_o = -M
\]  \hspace{1cm} (11.239)

and
\[
V_i = \frac{M}{k} + \frac{M}{k} \frac{1}{Qs} + \frac{M}{s^2} \frac{1}{s^2}
\]  \hspace{1cm} (11.240)

Rearranging (11.240) and using (11.239) gives
\[
M = kV_i - M \frac{1}{Qs} - M \frac{1}{s^2} = kV_i + \frac{1}{Q} V_o + \frac{V_o}{s^2}
\]  \hspace{1cm} (11.241)

Hence, again, using (11.239), we have
\[
V_o = - \left(kV_i + \frac{1}{Q} V_o + \frac{V_o}{s^2} \right)
\]  \hspace{1cm} (11.242)

This equation can be realized using the summing amplifier circuit shown in Fig. 11.55 as is easily verified. What is required in Fig. 11.55 are the input voltages \(V_i\), \(\frac{V_o}{s}\), and \(\frac{V_o}{s^2}\).
From our consideration of integrators in Chap. 8, $1/s$ represents integration, and hence, $1/s^2$ represents double integration. We will now demonstrate that the circuit in Fig. 11.56 (ignoring for the moment the impractical component values) fulfills the requirements of Fig. 11.55.

Op-amp $S$ is equivalent to the summing amplifier of Fig. 11.55. Its output $V_o$ drives op-amp 1, which is an integrator giving an output $V_1$ given by $G_{mf} = \frac{I_o}{V_s}$. The output of op-amp 1 drives op-amp 2, which is a
second integrator and whose output $V_2$ is given by $V_2 = -\frac{V_1}{s} = \frac{V_o}{s^2}$. Op-amp 3 inverts the signal $G_{mf} = \frac{l_o}{V_o}$, thereby producing $V_3 = -V_1 = \frac{V_o}{s}$.

The three signals $V_i$, $\frac{V_o}{s}$, and $\frac{V_o}{s}$ are now available for input to the summing amplifier op-amp $S$ via resistors with values $1/k$, $Q$, and 1, respectively, as shown in Fig. 11.55. The output $V_o$ of summing op-amp $S$ represents a **high-pass** filter characteristic given in the transfer function as

$$\frac{V_o(s)}{V_i} = \frac{-k s^2}{s^2 + \frac{1}{Q} s + 1} \quad (11.243)$$

Noting that $\frac{V_i}{V_o} = -1/s$, then

$$\frac{V_1}{V_i} \cdot \frac{V_o}{V_i} = \frac{-1}{s} \cdot \frac{-k s^2}{s^2 + \frac{1}{Q} s + 1} = \frac{ks}{s^2 + \frac{1}{Q} s + 1} \quad (11.244)$$

The transfer function (11.244) is a **band-pass** function. Also, noting that $\frac{V_i}{V_o} = -1/s$, then

$$\frac{V_2}{V_i} \cdot \frac{V_1}{V_i} = \frac{-1}{s} \cdot \frac{ks}{s^2 + \frac{1}{Q} s + 1} = \frac{k}{s^2 + \frac{1}{Q} s + 1} \quad (11.245)$$

The transfer function (11.245) is a **low-pass** function.

In the event that the high-pass function is not needed, then one of the op-amps can be eliminated by combining summation and integration in one device, as shown in Fig. 11.57. The transfer function for this system is easily shown to be

$$\frac{V_o}{V_i} = \frac{-ks}{s^2 + \frac{1}{Q} s + 1} \quad (11.246)$$

which is the band-pass function of op-amp 1 of Fig. 11.56 as desired. The three inputs required are $V_i$, $V_o$, and $V_o/s$. The first $V_i$ is the input
signal, the second \( V_o \) is the output of the integrator, and the third \( V_o/s \) is obtained by integrating \( V_o \) followed by an inverter to get the correct sign. The resulting system is shown in Fig. 11.58. Noting that \( \frac{V_i}{V_o} = -1/s \), then

\[
\frac{V_2}{V_i} = \frac{V_2}{V_o} \cdot \frac{V_o}{V_i} = -\frac{1}{s} \cdot \frac{-ks}{s^2 + \frac{1}{Q}s + 1} = \frac{k}{s^2 + \frac{1}{Q}s + 1}
\]

(11.247)

![Fig. 11.57 Circuit function combining summation and integration](image)
Fig. 11.58  Tow-Thomas Low-Pass biquadratic filter
Fig. 11.59  Band-pass biquadratic filter
Fig. 11.60  Band-stop biquadratic filter
**Fig. 11.61** Second-order speech filter

![Second-order speech filter](image1)

**Fig. 11.62** All-pass notch filter

![All-pass notch filter](image2)

**Fig. 11.63** Variable wide-band filter

![Variable wide-band filter](image3)

**Fig. 11.64** Universal filter system

![Universal filter system](image4)
Fig. 11.65  Variable frequency band-pass filter

Fig. 11.66  Active cross-over system

Fig. 11.67  Circuit for Question 7
Fig. 11.68 Circuit for Question 12

Fig. 11.69 Circuit for Question 21

Fig. 11.70 Circuit for Question 26
Fig. 11.71  Circuit for Question 29

Fig. 11.72  MFB band-pass filter for Question 31
The transfer function (11.247) is the low-pass function and the resulting circuit is the well-known *Tow-Thomas biquadratic filter*. The integrating configuration is referred to as a lossy integrator because of the presence of the resistor in parallel with the capacitor in the feedback loop.

The design process follows the standard procedure. The node equations for this filter using resistor and capacitor labels as shown and setting $C_1 = C_2 = C$ and $R_4 = R_5 = R_6 = R_3$ are given by

$$11.248$$
These lead to

\[ V_1 \frac{R_4}{V_2} = -V_2 sC \]  

(11.250)

Comparing this with the general form of the low-pass transfer function.

\[ \frac{V_2}{V_i} = \frac{R_3}{R_1 C^2 R_3 R_4} s^2 + \frac{s}{s CR_2} + \frac{1}{C^2 R_3 R_4} = \frac{R_3}{R_1 C^2 R_3^2} \]  

(11.251)

yields

\[ f_o = \frac{1}{2\pi CR_3} \]  

(11.253)

\[ Q = \frac{R_2}{R_3} \]  

(11.254)

\[ k = \frac{R_3}{R_1} \]  

(11.255)

In the design process, \( C \) is selected; then, \( R_3 \) is determined to give the desired \( f_o \). Following this, \( R_2 \) is determined to give the specified \( Q \), and finally, \( R_1 \) is adjusted to give the desired gain.

**11.12.1 Band-Pass Filter Design**
If only the band-pass function is desired, then the circuit can be re-
arranged by moving the inverter, as shown in Fig. 11.59, such that the
(inverted) band-pass output available at the output of the lossy
integrator is inverted. The result is a noninverting band-pass filter of
basic form

\[ \frac{V_o}{V_i} = \frac{kS}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \]  

(11.256)

The design process for this and the other configurations follows a
procedure similar to earlier treatments. The node equations for this
filter using resistor and capacitor labels and setting \( C_1 = C_2 = C \) and
\( R_4 = R_5 = R_6 = R_3 \) are given by

\[ \frac{V_i}{R_1} + \frac{V_B}{R_3} = -V_A \left( sC + \frac{1}{R_2} \right) \]  

(11.257)

\[ A_\infty = 1 + \frac{R_2}{R_1} \]  

(11.258)

\[ I_C = \beta F I_B \]  

(11.259)

These lead to

\[ \frac{V_o}{V_i} = \frac{\frac{s}{CR_1}}{s^2 + \frac{s}{CR_2} + \frac{1}{C^2 R_3 R_4}} = \frac{\frac{S^2 R_2}{R_1 CR_2}}{s^2 + \frac{s}{CR_2} + \frac{1}{C^2 R_3^2}} \]  

(11.260)

Comparing this with the general form of the band-pass transfer
function given in Eq. (11.157) gives

\[ \frac{V_o}{V_i} = -\frac{s\omega_o G}{s^2 + s \frac{\omega_o}{Q} + \omega_o^2} \]  

(11.261)

yields

\[ f_o = \frac{1}{2\pi CR_3} \]  

(11.262)
In the design process, $C$ is selected; then, $R_3$ is determined to give the desired $f_o$. Following this, $R_2$ is determined to give the specified $Q$, and finally, $R_1$ is adjusted to give the desired center frequency gain $G$.

**Example 11.36** Design a biquadratic band-pass filter using the topology in Fig. 11.59 for a center frequency of 5 kHz, a quality factor of 50, and a gain of 10.

**Solution** Select $C = 0.01 \mu F$. Then, from (11.262),

$$R_3 = \frac{1}{(2\pi f_0 C)} = \frac{1}{(2\pi \times 5 \times 10^3 \times 0.01 \times 10^{-6})} = 3.2 \text{ k}.$$  

From (11.263),

$$R_2 = 50 \times 3.2 \times 10^3 = 160 \text{ k},$$  

and from (11.264), $R_1 = R_2/10 = 16 \text{ k}$.

### 11.12.2 Band-Stop Filter Design

A band-stop filter can be realized using the biquadratic band-pass topology by subtracting the band-pass output from the input signal. This is shown in Fig. 11.60. Since the band-pass output is inverted, it can simply be added to the input signal in the summing amplifier. Thus,

$$Y_{out} = -I_o/V_o$$  

where

$$V_{bp} = -\frac{\frac{S^{R_2}}{R_1 C_1 R_2} V_i}{S^2 + \frac{S}{C_1 R_2} + \frac{1}{C_1 C_2 R_3 R_4}}$$  

Thus, substituting (11.266) into (11.265) yields

$$\frac{Q}{R_3} = \frac{R_2}{R_1}$$  

(11.263)
Setting the center frequency gain of the band-pass filter to unity corresponding to setting $R_2 = R_1$, Eq. (11.267) reduces to

$$
\frac{V_n}{V_i} = \frac{s^2 + \frac{1}{C_1 R_2}}{s^2 + \frac{s}{C_1 R_2} + \frac{1}{C_1 C_2 R_3 R_4}}
$$

(11.268)

From Eq. (11.185), the general form for a notch filter transfer function is

$$
\frac{V_o}{V_i} = \frac{k \omega_o^2}{s^2 + \frac{s \omega_o}{Q} + \omega_o^2}
$$

(11.269)

Comparing coefficients, we have

$$
f_o = \frac{1}{2 \pi \sqrt{C_1 C_2 R_3 R_4}}
$$

(11.270)

$$
a_1 / 2 \pi f_c = RC.
$$

(11.271)

If we set $C_1 = C_2 = C$ and $R_4 = R_3$, then these equations reduce to

$$
f_o = \frac{1}{2 \pi C R_3}
$$

(11.272)

$$
Q = \frac{R_2}{R_3}
$$

(11.273)

Thus, select $C$ and determine $R_3$ for a specific frequency using (11.272); then, adjust $R_2$ for a particular $Q$ using (11.273).

**Example 11.37**  Design a biquadratic notch filter with a center frequency of 200 Hz and a quality factor of 20.
**Solution**  Select $C = 0.1 \ \mu F$. Using (11.272),

$R_3 = \frac{1}{2\pi} \times 200 \times 0.1 \times 10^{-6} = 8 \ \text{k.}$ Using (11.273),

$R_2 = 20 \times 8 \times 10^3 = 160 \ \text{k}.$

---

**11.13 Applications**

Several active filter applications are presented in this section.

**11.13.1 Second-Order Speech Filter**

This system shown in Fig. 11.61 is a straightforward application of a wide-band filter comprising a second-order low-pass filter with a cut-off frequency of 300 Hz and a second-order high-pass filter with cut-off frequency 3.4 kHz. Both filters are Sallen and Key types, which employ a simplified design procedure such that the cut-off frequency is given by $f_c = \frac{1}{2\pi RC}$ and the circuit gain is set at 1.6 by resistors $R_a = 39 \ \text{k}$ and $R_b = 22 \ \text{k}$.

*Ideas for Exploration*: (i) Compare the performance of the 741 op-amp with the OPA134 op-amp in this application.

**11.13.1.1 All-Pass Notch**

Figure 11.62 shows a notch filter made using two first-order all-pass filters. The output of the second all-pass filter is

$V_A = \left(\frac{1-T_2}{1+T_2}, \frac{1-T_2}{1+T_2}\right) V_i = \left(\frac{1-2T_2^2}{1+2T_2^2+T_2^2s^2}\right) V_i$, where $T = RC$. This output is applied to one end of the potential divider comprising two series connected equal value resistors $R_{x1} = R_{x2}$ (Assume initially $VR = 0$). The input signal is applied at the other end of these two resistors, and op-amp 3 connected as a buffer takes its input from the junction of these two resistors. The voltage across these resistors is, therefore,

$V_A - V_i = \left(\frac{1-2T_2^2}{1+2T_2^2+T_2^2s^2} - 1\right) V_i = -\left(\frac{4T_2}{1+2T_2^2+T_2^2s^2}\right) V_i$. Half of this is dropped across each resistor $R_{x1}$ and is given by $V_{R_{x1}} = -\left(\frac{2T_2}{1+2T_2^2+T_2^2s^2}\right) V_i$.

Therefore, the voltage $V_o$ at the output $V_o$ of op-amp 3 is given by
This goes to zero at \( f_o = 1/2\pi RC \) and is nonzero at all other frequencies. This represents a notch filter with notch frequency \( f_o = 1/2\pi RC \) and \( Q = 1/2 \). We can choose \( R_A = 10\, k \) and \( R_{x1} = R_{x2} = 10\, k \). In the circuit, the potentiometer \( VR = 1\, k \) has been added to enable an adjustment for the deepest possible notch. Finally, for a notch frequency \( f_o = 1\, k\)Hz, choose \( C = 0.01\, \mu F \) and, therefore, \( R = 1/2\pi \times 10^3 \times 0.01 \times 10^{-6} = 15.9\, k \).

**Ideas for Exploration:** (i) Replace fixed resistors \( R \) by ganged variable resistors in series with fixed resistors such that the notch frequency can be continuously varied.

### 11.13.1.2 Variable Wide-Band Filter

The circuit in Fig. 11.63 is a variable wide-band filter whose cut-off frequencies are made variable by including variable resistors in series with fixed resistors. Each filter uses equal value resistors and capacitors and unity gain for simplicity. In order to realize a Butterworth response, the gain of each op-amp must be set to 1.6. Such a response is especially useful in audio systems as a scratch and rumble filter to remove unwanted high and low frequencies. The Butterworth response ensures minimum amplitude distortion in the pass-band. The dual-ganged potentiometers are 100 k linear type.

**Ideas for Exploration:** (i) Adjust the gains to 1.6 for Butterworth response. (ii) Compare the performance of the 741 op-amp with the OPA134 op-amp in this application.

### 11.13.1.3 Universal Filter

The circuit in Fig. 11.64 is a universal filter based on the modified sate variable filter. With the values selected \( (C = 0.01\, \mu F \) and the ganged potentiometer \( VR_3 = 100\, k \), the resonant frequency \( f_o = 1/2\pi CVR_3 \) is variable from about 160 Hz to about 16 kHz, the quality factor \( (Q = (VR_2 + 1\, k)/R_2) \) is variable from 0.1 to 100, and the center frequency gain \( (G = R_1/(VR_1 + 1\, k)) \) is variable from about 1 to 10. The circuit is assembled around a quad op-amp such as the OPA2134.
Ideas for Exploration: (i) Use a bank of switched capacitors to increase the frequency range.

**11.13.1.4 Research Project 1**

This research project involves the analysis and optimization of the variable frequency band-pass filter in Fig. 11.65. It uses cascaded all-pass filters in a feedback loop such that at the frequency where the phase shift is $180\degree$, the feedback around the input op-amp goes to zero such that the gain is at its maximum. At all other frequencies, the gain is reduced by the feedback. The loop gain is kept less than unity to ensure that there is no oscillation. Potentiometer $VR_1 = 20 \, k$ adjusts the quality factor, while the ganged potentiometers $VR_2$ vary the center frequency of the band-pass filter.

Ideas for Exploration: (i) Introduce a bank of switched capacitors for $C$ in order to realize a wide frequency range.

**11.13.1.5 Research Project 2**

This project involves research into and the design of an active crossover system used in audio speaker systems. A diagrammatic representation of such a system is shown in Fig. 11.66. This system separates the high frequencies and the low frequencies of a line level audio signal coming from a preamplifier using a high-pass filter and a low-pass filter, respectively. The output of the high-pass filter drives a power amplifier which delivers power to the tweeter in the speaker enclosure, while the output of the low-pass filter drives a separate power amplifier which drives the woofer in the speaker system. Such an approach allows the signal separation to take place at low signal levels, thereby avoiding the use of the expensive components found in passive cross-over filters used in speaker systems.

Ideas for Exploration: (i) Examine the introduction of an active band-pass filter that separates the mid-band frequencies and used to drive a third power amplifier that delivers power to a mid-range speaker.

**Problems**

1. Design a first-order low-pass noninverting filter with unity gain and a break frequency of 5 kHz.
2. Design a first-order noninverting low-pass filter with gain of 8 and a cut-off frequency of 17 kHz.

3. Design a first-order low-pass filter with gain of 12 and a cut-off frequency of 25 kHz using the inverting configuration.

4. Show that in a first-order low-pass filter, the amplitude response is down 3 dB at the cut-off frequency and determine the phase angle of the output relative to the input at that frequency.

5. Using the Sallen–Key configuration, design a second-order low-pass Butterworth filter with unity gain and a cut-off frequency of 50 kHz. Ensure that offset voltage is minimized.

6. Show that in the Sallen–Key second-order low-pass Butterworth filter, for the case where the network resistors are equal and the network capacitors are equal, the gain must be 1.6. Hence, repeat the design of Question 5 using this modified approach.

7. Show that in the Sallen–Key second-order unity-gain low-pass filter configuration shown in Fig. 11.67, if \( R_1 = R_2 \) and \( C_2 = 2C_1 \), then the transfer function reduces to a second-order Butterworth response.

8. Design a VCVS second-order unity-gain low-pass Chebyshev filter with a cut-off frequency of 22 kHz and a ripple width \( RWdB = 1 \) dB.

9. Design a VCVS second-order unity-gain low-pass Bessel filter with a cut-off frequency of 550 Hz.

10. Design a MFB second-order low-pass Butterworth filter with a gain of 8 and a cut-off frequency of 3 kHz.

11. Design a VCVS third-order unity-gain low-pass Butterworth filter with a cut-off frequency of 33 kHz. What is the ultimate roll-off rate of such a filter?
12. Show that in the Sallen–Key third-order unity-gain low-pass filter configuration shown in Fig. 11.68, if $R_1 = R_2 = R_3$, $C_2 = 2C_3$, and $C_1 = C_3/2$, then the transfer function reduces to a third-order Butterworth response. Hence, repeat Question 11 using this simplified design procedure.

13. Design a VCVS fourth-order unity-gain low-pass Chebyshev filter with a cut-off frequency of 12 kHz and 3-dB ripple width.


15. Design a first-order high-pass noninverting filter with unity gain and a break frequency of 5 kHz.

16. Design a first-order noninverting high-pass filter with gain of 8 and a cut-off frequency of 17 kHz.

17. Design a first-order high-pass filter with gain of 15 and a cut-off frequency of 10 kHz using the inverting configuration.

18. Show that in a first-order high-pass filter, the amplitude response is down 3 dB at the cut-off frequency, and determine the phase angle of the output relative to the input at that frequency.

19. Using the Sallen–Key configuration, design a second-order high-pass Butterworth filter with unity gain and a cut-off frequency of 5 kHz.

20. Show that in the Sallen–Key second-order high-pass Butterworth filter, for the case where the network resistors are equal and the network capacitors are equal, the gain must be 1.6. Hence, repeat the design of Question 19 using this modified approach.

21. Show that in the Sallen–Key second-order unity-gain high-pass filter configuration shown in Fig. 11.69, if $R_1 = 2R_2$ and $C_1 = C_2$, then the transfer function reduces to a second-order high-pass Butterworth response.
22. Design a VCVS second-order unity-gain high-pass Chebyshev filter with a cut-off frequency of 14 kHz and a ripple width $R_{WdB} = 1$ dB.

23. Design a VCVS second-order unity-gain high-pass Bessel filter with a cut-off frequency of 5 kHz.

24. Design a MFB second-order high-pass Butterworth filter with a gain of 6 and a cut-off frequency of 2 kHz.

25. Design a VCVS third-order unity-gain high-pass Butterworth filter with a cut-off frequency of 900 Hz. What is the ultimate roll-off rate of such a filter?

26. Show that in the Sallen–Key third-order unity-gain low-pass filter configuration shown in Fig. 11.70, if $C_1 = C_2 = C_3$, $R_1 = 2R_3$, and $R_2 = R_3/2$, then the transfer function reduces to a third-order Butterworth response. Hence, repeat Question 25 using this simplified design procedure.

27. Design a VCVS fourth-order unity-gain high-pass Chebyshev filter with a cut-off frequency of 1200 Hz and 2-dB ripple width.

28. Design a VCVS fifth-order unity-gain high-pass Bessel filter with a cut-off frequency of 6 kHz.

29. Using the VCVS band-pass filter shown in Fig. 11.71, design a Sallen–Key second-order band-pass filter having $C_1 = C_2$, $R_1 = R_2$ with a center frequency of 13 kHz and a quality factor of 8.

30. For the VCVS band-pass filter shown in Fig. 11.65, develop design equations for $R_1$, $R_2$ and $R_3$ if $C_1 = C_2 = C$ and $1 + R_b/R_a = 2$. Hence, design a VCVS band-pass filter having $f_o = 20$ kHz, $Q = 6$, and $G = 10$.

31. Design a second-order MFB band-pass filter with $f_o = 2$ kHz, $Q = 9$,
and \( G = 5 \). Use the circuit shown in Fig. 11.72.

32. For the second-order MFB band-pass filter shown in Fig. 11.66, develop design equations without imposing the condition \( C_1 = C_2 \). Hence, design a second-order MFB band-pass filter having \( f_0 = 1 \) kHz, \( Q = 5 \), and \( G = 10 \).

33. Design a second-order Wien band-pass filter with \( f_0 = 60 \) Hz, \( Q = 10 \), and \( G = 2 \).

34. Design a twin-T notch filter having a notch frequency of 2.5 kHz and \( Q = 25 \).

35. Using the circuit shown in Fig. 11.73, design a Wien notch filter to have a notch frequency of 200 Hz, a \( Q \) of 25, and a gain of 2.

36. By using a ganged potentiometer for \( R \) and two banks of switched capacitors for \( C \), convert the Wien notch filter in Fig. 11.73 to a variable frequency circuit and specify the frequency range.

37. Design a first-order all pass filter with a 25\(^\circ\) phase lag at \( f = 3 \) kHz. What phase shift will this circuit produce for a signal of frequency \( f = 10 \) kHz?

38. Design a first-order all pass filter with a 25\(^\circ\) phase lead at \( f = 12 \) kHz. What phase shift will this circuit produce for a signal of frequency \( f = 25 \) kHz?

39. Using the state variable filter, design a band-pass filter with a center frequency \( f_0 = 25 \) kHz, a quality factor \( Q = 33 \), and a center frequency gain \( G = 8 \).

40. Derive the transfer functions for the universal filter shown in Fig. 11.74.

41. Develop the transfer function for a Tow-Thomas biquadratic filter. Design a biquadratic band-pass filter using the topology in Fig.
42. Design a biquadratic band-pass filter using the topology in Fig. 11.59 for a center frequency of 38 kHz, a quality factor of 45, and a gain of 4.

43. Design a biquadratic notch filter with a center frequency of 1400 Hz and a quality factor of 20.

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[Crossref]
12. Oscillators

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Oscillators deliver an essentially sinusoidal output waveform without input excitation. They are used in a wide range of applications including testing, communication systems, and computer systems. Frequencies range from about $10^{-3}$ to $10^{10}$ Hz, and in many applications a low distortion is required. There are two main classes of oscillators; RC oscillators in which the frequency determining elements are resistors and capacitors and LC oscillators in which the frequency-determining elements are inductors and capacitors. RC oscillators operate from very low frequencies up to about 10 MHz, making them very useful for audio frequency applications, while LC oscillators are useful for frequencies above about 100 kHz, and they are usually used in communication applications. This chapter explores the basic principles governing this class of circuits. The conditions required for oscillation are investigated and frequency and amplitude stability studied. At the end of the chapter, the student will be able to:

- Explain the principle of operation of an oscillator and the criterion for oscillation.
- Explain the operation of a wide range of oscillators.
Design a wide range of oscillators.
Create new oscillator systems.

### 12.1 Conditions for Oscillation
The diagram in Fig. 12.1 shows a closed-loop positive feedback system consisting of an amplifier $A$, a feedback network $\beta$, and a summing junction $\Sigma$. The transfer function for this system is given by

$$\frac{X_o}{X_i} = \frac{A(s)}{1 - A(s)\beta(s)}$$

(12.1)

where $X_o$ is the output signal, $X_i$ is the input signal, $X_f$ is the feedback signal, and $X_e$ is the error signal resulting from a summation of the feedback signal with the input signal. $A\beta(s)$ is the loop gain. In negative feedback systems, the feedback signal $X_f$ is subtracted from the input signal. In positive feedback systems, $X_f$ is added as it is here, resulting in an increase in the error signal $X_e$. If the loop gain goes to unity then the closed-loop transfer function goes to infinity implying that the system can sustain a finite output signal with no input signal. In such a circumstance, the output waveform need not be sinusoidal, and the amplifier need not be linear. All that is required is that $A\beta = 1$ which means that the instantaneous value of $X_i$ is at all times equal to the value of $X_f$. This condition is called the Barkhausen criterion and is expressed as

$$I_{sc} = -h_feI_b,$$

(12.2)
This condition is really equivalent to two conditions:

\[ |A(s)| |\beta(s)| = 1 \]  \hspace{1cm} (12.3)

i.e., the magnitude of the loop gain must be unity and

\[ A_{V2} = -40I_{C3}R_L \]  \hspace{1cm} (12.4)

where \( n = 0,1,2,... \), i.e., the total phase shift through the amplifier and feedback network must be zero or multiples of \( 2\pi \).

If the feedback network (or amplifier) contains reactive elements and the entire oscillator is approximately linear, then the only periodic waveform which will preserve its form is the sinusoid. What this means in effect is that since the reactive element introduces phase shift that changes with frequency, then the Barkhausen criterion will only be met at a particular frequency, and hence a sustained sinusoidal output at that frequency is produced. A general principle for oscillators can therefore be stated:

The frequency of operation of an oscillator is that frequency at which the total phase shift around the system is zero (or multiples of \( 2\pi \)) and the loop gain is one (or greater).

When these conditions are satisfied, a signal \( X_i \) entering the system returns such that \( X_f \) is equal to or greater than \( X_i \). This results in an equal or larger signal \( X_i \) entering the system, which will again reappear as a still larger signal \( X_f \). This will continue and the output signal \( X_o \) will increase indefinitely. It is limited by the saturation of the amplifier delivering the output signal \( X_o \). If the loop gain is less than one, i.e., \( |A\beta| < 1 \), then removal of the external signal will result in the cessation of oscillations. If the loop gain is greater than one, i.e., \( |A\beta| > 1 \), the amplitude of the oscillations will increase until limited by amplifier saturation. Since it is impossible to set the loop gain exactly equal to one, i.e., \( |A\beta| = 1 \), in practice, the loop gain is usually set somewhat larger than unity in which case the amplitude of the oscillations is limited by the onset of nonlinearity. This onset of nonlinearity through saturation of the oscillator amplifier is a general feature of practical
oscillators. However, it results in distortion of the output signal, which increases as the loop gain is made greater than one. As a practical matter, it is therefore important that the loop gain be made only slightly greater than one, say by about 5% or so, so that oscillation is maintained while distortion is minimized. It is possible to manually set the loop gain close to unity but this is not a reliable approach. Amplitude stabilization by electronic means is possible and is discussed in Sect. 12.6. We will now apply the basic criterion to the design of several types of sinusoidal oscillators.

12.2 RC Oscillators

From the analysis in Sect. 12.1, an oscillator that produces sinusoidal waveforms can be realized by combining a linear amplifier with a frequency-dependent network in its feedback loop. Oscillators that utilize networks comprising resistors and capacitors are referred to as \( RC \) oscillators.

12.2.1 Wien Bridge Oscillator

An RC oscillator circuit that works on the basis of the Barkhausen criterion is the Wien bridge oscillator shown in Fig. 12.2a. It consists of an amplifier A with a Wien network comprising \( RC \) elements connected in its feedback loop as shown. The input impedance of the amplifier is assumed to be high, while the output impedance is assumed to be low. These conditions are easily met by using an operational amplifier as the amplifying element. The term Wien bridge derives from the fact that the Wien network and the amplifier gain-setting resistors \( R_A \) and \( R_B \) as shown in Fig. 12.2b form a bridge across which a null occurs at \( f_o \).
In analyzing this system, consider the Wien network as shown in Fig. 12.3. The transfer function $\frac{V_{wo}}{V_{wi}}$ for this network is given by

$$
\frac{V_{wo}}{V_{wi}} = \frac{Z_2}{Z_1 + Z_2} = \frac{R\frac{1}{sC}/(R + \frac{1}{sC})}{R + \frac{1}{sC} + R\frac{1}{sC}/(R + \frac{1}{sC})}
$$

(12.5)

This reduces to

$$
(12.6)
$$
This response is called a band pass response and has center frequency $\omega_o = 2\pi f_o$ and pass band gain $G$ given by

$$\omega_o = \frac{1}{RC}, f_o = \frac{1}{2\pi RC}$$  \hspace{1cm} (12.7)

and

$$G = \frac{1}{3}$$ \hspace{1cm} (12.8)

The magnitude and phase responses can be determined analytically by setting $s = j\omega$ in (12.6) giving

$$\frac{V_{wo}(j\omega)}{V_{wi}} = \frac{j\omega CR}{1 + 3CRj\omega + (j\omega)^2C^2R^2} = \frac{jf/f_o}{1 + 3jf/f_o + (jf/f_o)^2}$$  \hspace{1cm} (12.9)

The responses are shown in Fig. 12.4. Clearly at the frequency $f_o$, the phase response shows that there is no phase shift between $V_{wo}$ and $V_{wi}$. Also, at this frequency, $|V_{wo}/V_{wi}| = 1/3$. 
From (12.9) for $V_{wo}$ to be in phase with $V_{wi}$, since the numerator is imaginary, then the denominator must also be imaginary. Hence, the real part of the denominator must be zero, that is

$$1 - \omega^2 C^2 R^2 = 0$$

(12.10)

i.e.

$$\omega_0 = \frac{1}{CR} \quad \text{or} \quad f_0 = \frac{1}{2\pi CR}$$

(12.11)

This gives

$$\frac{V_{wo}}{V_{wi}}(\omega_0) = \frac{j\omega CR}{3j\omega CR} = \frac{1}{3}$$

(12.12)

Thus, a signal $V_{wi}$ entering the network produces a signal $V_{wo}$ at the output and at the frequency $f_0$; both signals are in phase with the output signal being attenuated relative to the input by a factor of 3. When this signal passes through the amplifier $A$, if the amplifier has a gain 3, then the Barkhausen criterion $A\beta = 1$ is satisfied and oscillation results.

The conditions for oscillation in the Wien bridge oscillator can be more directly determined by applying the Barkhausen criterion to the system. Thus, for the system in Fig. 12.2a,

$$A\beta = A\frac{j\omega CR}{1 + 3j\omega CR + (j\omega CR)^2} = 1$$

(12.13)

where $\beta$ is the transfer function of the Wien network given in (12.9) and $A$ is the amplifier gain. From (12.13), we have

$$j\omega CRA = 1 + 3j\omega CR - (\omega CR)^2$$

(12.14)

from which

$$j\omega CRA = 1 + 3j\omega CR - (\omega CR)^2$$

(12.15)
Hence, equating real and imaginary parts to zero, we have \( A - 3 = 0 \) and \( 1 - \omega^2 C^2 R^2 = 0 \) giving

\[
A = 3
\]  \hspace{1cm} (12.16)

\[
f_o = \frac{1}{2\pi RC}
\]  \hspace{1cm} (12.17)

Thus, the amplifier gain for oscillation at \( f_o = 1/2\pi RC \) in the Wien bridge oscillator is \( A = 3 \). A practical implementation of this method is shown in Fig. 12.5 where an operational amplifier is used as the amplifying element with \( R_A = 1 \text{k} \) and \( R_B = 2 \text{k} \).

![Fig. 12.5 Complete circuit of Wien bridge oscillator](image)

**Example 12.1**  Design a Wien bridge oscillator to operate at a frequency of 1 kHz.

**Solution**  Using the configuration in Fig. 12.5, we first choose a reasonable value for \( C \) say \( C = 0.01 \mu\text{F} \). Then, for oscillation at \( f = 1 \text{kHz} \) using Eq. (12.17) the value of \( R \) is given by

\[
R = \frac{1}{2\pi \times 10^3 \times 0.01 \times 10^{-6}} = 15.9 \text{ k}
\]

Also, from (12.16), the gain of the op-
amp is given by $1 + \frac{R_R}{R_A} = 3$. If we choose $R_A = 1$ k then $R_B = 2$ k. In order to sustain oscillation, we make $R_2$ slightly greater than 2 k say 2.01 k.

This circuit was simulated in the laboratory using an LF351 operational amplifier and a ± 15-volt supply. The frequency of the resulting sinusoidal waveform was 968 Hz and the amplitude 13.3 V peak. Better accuracy in the frequency can be achieved by using an operational amplifier with a higher gain bandwidth product. For amplitude stabilization, $R_B$ can be a thermistor with a negative temperature coefficient. This is discussed in Sect. 12.6. An advantage of the Wien bridge oscillator is its ability to cover a wide frequency range by using ganged variable resistors for $R$ for continuous variation of $f_o$ over a given band and switched banks of capacitors for $C$ to vary the frequency band as shown in Fig. 12.6.

![Wien bridge oscillator with wide-range tuning](image)

**Example 12.2**  Derive the transfer function for the $RC$ network shown in Fig. 12.7, and determine the frequency at which the output is in phase with the input. If the network is used as the basis of a sinusoidal oscillator, determine the minimum voltage gain required from the associated amplifier, and design the system to oscillate at 10 kHz.
Solution  For the network, where $s = j\omega$. For $V_o$ to be in phase with $V_i$, $1 - 4\omega^2 R^2 C^2 = 0$ which gives $\omega_o^2 = 1/4C^2 R^2$ or $f_o = 1/4\pi CR$. Hence, $\frac{V_o}{V_i}(f_o) = \frac{2}{7}$. An oscillator using this network would replace the Wien network in Fig. 12.5 by this one. Since the network attenuation at the oscillating frequency is $2/7$, for oscillation, based on the Barkhausen criterion, it follows that the amplifier gain must be $7/2$, i.e., $1 + \frac{R_B}{R_A} = \frac{7}{2}$. If we choose $R_A = 1$ k, then $R_B = 2.5$ k. For $f_o = 10$ kHz $= 1/4\pi CR$, choose $C = 0.001$ μF. Then, $R = \frac{1}{4\pi \times 0.001 \times 10^{-6} \times 10^4} = 8$ k. Hence, $2R = 16$ k and $2C = 0.002$ μF.

12.2.2 Phase-Shift Oscillator-Lead Network

The phase-shift oscillator is shown in Fig. 12.8 and consists of an inverting amplifier A driving three cascaded $RC$ combination, the output of the last $RC$ combination being returned to the input of the amplifier. If the loading of the phase-shift network by the amplifier is neglected, the amplifier shifts the signal appearing at its input by 180° and the $RC$ network shifts the signal phase by an additional 180°. At the frequency $f_o$ at which the phase shift introduced by the $RC$ network is
precisely $180^\circ$, the total phase shift around the system will be zero. This frequency $f_o$ will be the frequency at which the circuit will oscillate, provided that the magnitude of the loop gain is sufficiently large, i.e., greater than or equal to one. For the lead phase-shift network shown in Fig. 12.9, the transfer function $V_o/V_i$ is given by

$$\frac{V_o}{V_i} = \frac{V_o}{V_B} \frac{V_B}{V_A} \frac{V_A}{V_i} = \frac{R}{R - jX_C} \frac{Z_B}{Z_B - jX_C} \frac{Z_A}{Z_A - jX_C}$$

(12.18)

where

$$R_5 = \frac{0.7}{I_{L(\text{max})}}$$

(12.19)

$$Z_B = \frac{R(R - jX_C)}{2R - jX_C}$$

(12.20)

$$Z_A = \frac{R(Z_B - jX_C)}{R + Z_B - jX_C}$$

(12.21)
After substitution and extensive manipulation, the transfer function becomes
\[ \frac{V_o}{V_i} = \frac{1}{1 - 5\alpha^2 - j(6\alpha - \alpha^3)} \] (12.22)

where
\[ \alpha = \frac{1}{\omega CR} \] (12.23)

In order that the phase-shift network contributes 180° at \( f_o \), the imaginary term in (12.22) must be zero, i.e.
\[ 6\alpha - \alpha^3 = 0 \] (12.24)
giving
\[ \omega_0 = \frac{1}{\sqrt{6CR}} \quad \text{or} \quad f_0 = \frac{1}{2\pi \sqrt{6CR}} \] (12.25)

By substituting \( \omega_0 = 2\pi f_0 \) in (12.22), we get
\[ \frac{V_o}{V_i}(f_o) = -\frac{1}{29} \] (12.26)

In order to satisfy the Barkhausen criterion, then \( A = -29 \), i.e., the magnitude of the gain of the associated amplifier must be 29 or greater.
A practical implementation of the phase-shift oscillator using the lead network is shown in Fig. 12.10. An inverting op-amp is used to provide $180^\circ$ phase shift as well as the gain of $-29$. Note that the input resistor $R$ of the op-amp is one of the resistors of the phase-shift network. This is possible since the inverting input of the op-amp is a virtual earth. The phase-shift oscillator is not very useful as a variable frequency oscillator since frequency variation requires variation of three components simultaneously. It can however be used as a fixed frequency oscillator.

**Fig. 12.10** Practical phase-shift oscillator

**Example 12.3** Design a phase-shift oscillator to operate at a frequency of 1 kHz.

**Solution** Using the circuit of Fig. 12.10, we first design the phase-shift network. Choosing $C=0.01 \, \mu F$, Eq. (12.25) yields

$$R = \frac{1}{2\pi 10^3 \sqrt{6\times0.01\times10^{-6}}} = 6497 \, \Omega \approx 6.5 \, k.$$ 

Hence, $R_F = 29 \times R = 29 \times 6.5 \, k = 188.5 \, k$. Use $R_F = 190 \, k$ to ensure oscillation. This circuit was
simulated using an LF351 op-amp and ± 15-volt supply. The measured frequency was 958 Hz, and the measured peak amplitude was 13.1 V.

### 12.2.3 Phase-Shift Oscillator-Lag Network

The phase-shift oscillator may be constructed using three lag $RC$ sections instead of the lead $RC$ sections used previously. The basic system is shown in Fig. 12.11.

---

**Fig. 12.11** Phase-shift oscillator system

Neglecting amplifier loading, the inverting amplifier shifts the signal by 180°, while the lag network shifts negatively by an additional factor. At a frequency $f_0$ at which this shift is $-180°$, with a loop gain of one or greater, oscillation results. For the phase shift lag network shown in Fig. 12.12, the transfer function $V_o/V_i$ is given by

$$\frac{V_o}{V_i} = \frac{V_o V_B V_A}{V_B V_A V_i} = \frac{-jX_C}{R - jX_C Z_B + R Z_A + R}$$  \hspace{1cm} (12.27)

where

$$R_S = \frac{0.7}{I_{L(max)}}$$  \hspace{1cm} (12.28)

$$R_S$$  \hspace{1cm} (12.29)
After substitution and considerable manipulation, the transfer function becomes

\[
Z_B = \frac{-jX_C (R - jX_C)}{R - 2jX_C}
\]

\[
Z_A = \frac{-jX_C (R + Z_B)}{R + Z_B - jX_C}
\]

(12.30)

*Fig. 12.12* Lag RC network

After substitution and considerable manipulation, the transfer function becomes

\[
\frac{V_o}{V_i} = \frac{1}{1 - 5\alpha^2 - j(6\alpha - \alpha^3)}
\]

(12.31)

where

\[X_f = \beta X_o\]

(12.32)

For a 180° phase shift contribution at \(\omega_o\), the imaginary term in (12.31) must be zero, i.e.

\[6\alpha - \alpha^3 = 0\]

(12.33)

giving

\[\omega_0 = \frac{\sqrt{6}}{CR} \quad \text{or} \quad f_0 = \frac{\sqrt{6}}{2\pi CR}\]

(12.34)

Substituting \(\omega_0\) in (12.31) gives

(12.35)
\[
\frac{V_o}{V_i}(f_o) = -\frac{1}{29}
\]

In order to satisfy the Barkhausen criterion, \( A = -29 \) which means that the associated amplifier must have a gain whose magnitude is 29 or greater. In order to prevent the inverting amplifier from loading the network and thereby affect its oscillating frequency, the phase-shift oscillator is implemented using the configuration shown in Fig. 12.13 in which a buffer is included at the output of the third \( RC \) section. Again, an inverting operational amplifier is used to provide 180° phase shift and –29 gain. A dual op-amp such as the LF353 is convenient for the implementation of this circuit.

![Phase-shift lag oscillator with buffered network output](image)

**Example 12.4**  Design a phase-shift lag oscillator with an oscillating frequency of 1 kHz.

**Solution**  Using the circuit of Fig. 12.13, for the phase-shift network, choose \( C = 0.1 \, \mu F \). Then, Eq. (12.34) yields

\[
R = \frac{\sqrt{6}}{2\pi10^3 \times 0.1 \times 10^{-6}} = 4 \, \text{k}
\]

For \( R_f = 2.5 \, \text{k} \), then \( R_F = 72.5 \, \text{k} \). This circuit based on the LF351 was simulated and produced a sinusoidal waveform of frequency 965 Hz and amplitude 1.22 V peak. An interesting feature of this circuit is that the three \( RC \) low-pass sections filter out harmonics from the signal and hence the distortion at the output of the voltage follower is low.

**12.2.4 Buffered Phase-Shift Oscillator**
The buffered phase-shift oscillator shown in Fig. 12.14 involves buffering all $RC$ sections of the phase shift lag network such that there is no interaction between the sections. The effect of this is the simplification of the analysis since there is no interaction between successive RC sections. The transfer function for each section is given by $\frac{1}{(1 + sCR)}$, and hence the Barkhausen criterion gives

$$A\beta = \frac{1}{(1 + sCR)^3} = 1$$

(12.36)

**Fig. 12.14** Buffered phase-shift oscillator

This reduces for $s = j\omega$ to

$$A = \left(1 - 3\omega^2C^2R^2\right) + j\omega CR \left(3 - \omega^2C^2R^2\right)$$

(12.37)

For $A$ real, it follows that the imaginary component on the right must be zero, i.e.

$$1 - \omega^2C^2R^2 = 0$$

(12.38)

giving

$$\omega_0 = \frac{\sqrt{3}}{CR} \quad \text{or} \quad f_0 = \frac{\sqrt{3}}{2\pi CR}$$

(12.39)

This is the frequency of oscillation. Substituting this in (12.37) gives $A = -8$, i.e., each RC section produces an attenuation of $1/2$ at $f_0$ resulting in a total attenuation of $1/8$. This circuit is easily implemented.
using a quad operational amplifier. It is particularly useful for low distortion oscillation as each RC network filters the harmonics from the signal. Also, since the amplifier gain is only 8, more feedback can be employed around this amplifier than for the case where the gain is 29.

**Example 12.5**  Design a buffered phase-shift oscillator to oscillate at 5 kHz. Use an LF347 quad op-amp and a ± 15-volt power supply.

**Solution**  Using the circuit in Fig. 12.14, for oscillation at 5 kHz, we choose \( C = 0.01 \, \mu \text{F} \). Then Eq. (12.39) gives

\[
R = \frac{\sqrt{3}}{2\pi \times 5 \times 10^4 \times 0.01 \times 10^{-6}} = 5.5 \, \text{k}.
\]

The gain of the amplifier is given by \( \frac{R_F}{R_I} = 8 \). We choose \( R_I = 5k \) giving \( R_F = 40k \). We use \( R_2 = 42 \, \text{k} \) in order to sustain oscillation. This circuit was simulated, and it oscillated at a frequency of 4.92 kHz with amplitude of 1.9 V peak.

**12.2.5 Multiphase Sinusoidal Oscillator**

Another type of phase-shift oscillator is the multiphase sinusoidal oscillator shown in Fig. 12.15. This circuit uses active phase shift first-order elements to produce 360° around the loop. Each of the elements is identical, and therefore three equal amplitude outputs are produced, each shifted in phase from the other by 120°. This kind of oscillator is particularly useful in communications systems. The transfer function for each section is given by \(-k/(1 + sRC)\), where \( k = R/R_I \). Applying the Barkhusen criterion gives

\[
A\beta = \left( \frac{-R/R_I}{1 + sRC} \right)^3 = 1 \quad \text{(12.40)}
\]
For \( s = j\omega \), this reduces to

\[
(1 + j\omega \tau)^3 + k^3 = 0
\]  \hspace{1cm} (12.41)

where \( k = R/R_1 \) and \( \tau = RC \). This becomes

\[
R_3 = \left( 15 \sqrt{2} - 6.8 \right) / 10 \text{ mA} = 1.4 \text{ k}.
\]  \hspace{1cm} (12.42)

In order that (12.42) be satisfied, the imaginary part must be zero, i.e.

\[
3 - \omega^2 \tau^2 = 0
\]  \hspace{1cm} (12.43)

from which

\[
\omega_o = \frac{\sqrt{3} \text{ } \text{mA}}{RC} \text{ or } f_o = \frac{\sqrt{3} \text{ } \text{kHz}}{2\pi RC}
\]  \hspace{1cm} (12.44)

Substituting this in (12.42) gives \( k^3 = 8 \), and therefore \( k = 2 \), i.e., each stage must have a gain of 2.

**Example 12.6**  Design a multiphase sinusoidal oscillator using the circuit of Fig. 12.15 to give a sinusoidal output of frequency 2 kHz.
Solution Using the circuit of Fig. 12.15, we select $C = 0.01 \, \mu F$. Hence, Eq. (12.44) gives

$$R = \frac{\sqrt{3}}{2\pi \times 2 \times 10^3 \times 0.01 \times 10^{-6}} = 13.8 \, \text{k}.$$  

The gain of the amplifier is given by $\frac{R}{R_1} = 2$. For $R = 13.8 \, \text{k}$, $R_1 = 6.9 \, \text{k}$. The simulated circuit oscillated at a frequency of 1.96 kHz and an amplitude of 13.3 V peak.

12.2.6 Quadrature Oscillator

The quadrature oscillator achieves oscillation by cascading sections that shift the phase of the signal 360° at a loop gain of unity. Three RC sections are cascaded such that two of the sections each produce 45° of phase shift while the third in conjunction with the inversion of the op-amp produces 270°. The outputs of the two op-amps are 90° out of phase and hence are referred to as sine and cosine, i.e., quadrature. The basic circuit is shown in Fig. 12.16.

![Quadrature oscillator](image)

**Fig. 12.16** Quadrature oscillator

The loop gain $A\beta$ is given by

(12.45)
Aβ = \frac{1}{R_1C_1s} \cdot \frac{1}{1 + R_2C_2s} \cdot \frac{1 + R_3C_3s}{R_3C_3s}

For

R_1C_1 = R_2C_2 = R_3C_3

Equation (12.45) reduces to

Aβ = -\frac{1}{R^2C^2s^2} = \frac{1}{R^2C^2\omega^2}

(12.47)

For oscillation, \(Aβ = 1\), and hence (12.47) yields the frequency of oscillation.

\[\omega_o = \frac{1}{RC} \text{ or } f_o = \frac{1}{2\pi RC}\]

(12.48)

By inspection of the second and third terms in the transfer function (12.45), it can be seen that at \(f_o\), the second term corresponding to the passive section \(R_2C_2\) contributes 45° phase lag while the third term corresponding to the elements \(R_3C_3\) and the operational amplifier contributes 45° phase lag. Hence, the output \(V_{o1}\) is 90° out of phase with \(V_{o2}\). These outputs are therefore labelled sine and cosine or quadrature. One advantage of this circuit is that the circuit offsets tend to balance each other. Dual operational amplifiers such as the 1458 are convenient for the implementation of this oscillator. \(R_3\) is usually made slightly less than \(R\) to ensure that the circuit oscillates. In such a scenario, the op-amps will eventually saturate, and it may be necessary to use amplitude limiting Zener diodes across the capacitor in the Miller integrator. As is the case with all of these circuits, the maximum oscillating frequency is determined by the GBP of the operational amplifiers involved.

Example 12.7  Design a quadrature oscillator to oscillate at 1 kHz.

Solution  Using the configuration in Fig. 12.16, for \(C = 0.01 \mu F\) and \(f_o = 1\ kHz\), Eq. (12.48) gives \(R = \frac{1}{2\pi \times 10^3 \times 10^{-8}} = 15.9\ k\). This circuit
oscillated at a frequency of 1 kHz and amplitude 13.5 V peak. $R_3$ was set at 15.5 k in order to start oscillation.

### 12.2.7 Another Quadrature Oscillator

The final RC oscillator to be discussed is another quadrature oscillator. It utilizes two Miller integrators, each producing a phase shift of 90° along with an inverting amplifier, which produces a further phase shift of −180° such that the total phase shift is 0°. The circuit is shown in Fig. 12.17. The loop gain $A\beta$ is given by

$$A\beta = \frac{-1}{sC_1R_1} \cdot \frac{-1}{sC_2R_2} \cdot \frac{-R_4}{R_3}$$

(12.49)

![Another quadrature oscillator](image)

Since $A\beta = 1$ for oscillation, then, letting $C_1 = C_2 = C$, $R_1 = R_2 = R$ and $R_3 = R_4 = R_A$, then (12.49) gives

$$\omega_o = \frac{1}{RC} \quad \text{or} \quad f_o = \frac{1}{2\pi RC}$$

(12.50)

This circuit has the disadvantage that offset voltages must be precisely balanced; otherwise, they will cause a build-up of voltage across the capacitors of the two integrators and consequently dampen the oscillations. The circuit in Fig. 12.16 automatically balances its offsets and hence is superior.
12.3 LC Oscillators

RC oscillators require at least two RC sections in order to produce the required phase shift to realize oscillation. Any resulting signal loss is compensated for by amplification. If the amplifier gain is excessive, the distortion level is higher since less negative feedback is available. LC oscillators are able to produce the necessary phase shift with two components and the frequency of oscillation is the resonant frequency of the LC circuit. Moreover, tuning is usually via one component. Finally, LC oscillators are often used at higher frequencies than RC oscillators since the amplifying element can be a single transistor having a higher frequency response than an op-amp. In this section, we consider the theory and design of LC oscillators.

12.3.1 LC Resonant Oscillator

The first of the LC oscillators for producing sinusoidal waveforms to be considered is the LC resonant oscillator shown in Fig. 12.18. It utilizes an LC frequency-selective circuit in the drain of a JFET. A secondary winding couples signal from the coil back to the JFET input. The JFET in the common source configuration produces 180° phase shift while an appropriate connection of the transformer (see dots) produces a further 180° phase shift. For the FET, the voltage gain $A_V$ is given by

$$A_V = \frac{V_o}{V_i} = -g_m r_d \| jX_L \|-jX_C$$

where $r_d$ is the output resistance of the FET. The high FET input impedance prevents transformer loading. Now, for the circuit,

$$V_o = L \frac{di_1}{dt} + M \frac{di_2}{dt} \approx L \frac{di_1}{dt}$$

$$V_i = V_f = -L \frac{di_2}{dt} - M \frac{di_1}{dt} \approx -M \frac{di_1}{dt}$$

since $i_2 \approx 0$ and where $M$ is the mutual inductance between the two windings, $i_1$ is the current in the transformer primary and $i_2$ is the
current in the transformer secondary. From (12.52) to (12.53)

\[
\beta = \frac{V_f}{V_o} = \frac{-M}{L}
\]  

(12.54)

**Fig. 12.18** LC resonant oscillator

Hence

\[
A\beta = -g_m r_d \|jX_L\| - jX_C \cdot \frac{-M}{L}
\]  

(12.55)

\[
A\beta = \frac{M}{L} g_m \left(1 + \frac{r_d}{jX_L\|jX_C\|} \right) = \frac{M}{L} g_m \frac{r_d}{1 + r_d \frac{j(x_L - x_C)}{x_L x_C}}
\]  

(12.56)

For the Barkhausen criterion to be satisfied, we must have zero phase shift. From (12.56), this occurs when the imaginary component of \( A\beta \) is zero, i.e.

\[
X_L = X_C
\]  

(12.57)

giving

\[
(12.58)
The system will sustain oscillations if $A\beta = 1$, i.e.

$$\frac{M}{L} g_m r_d = 1 \quad (12.59)$$

If the coil has resistance $r_s$ which is effectively in series with the inductor $L$, then the equivalent parallel resistance $R_{eff}$ is given by

$$R_{eff} = r_s Q^2 \quad (12.60)$$

where $Q$ is the quality factor of the inductor given by

$$Q = \frac{\omega_0 L}{R} \quad (12.61)$$

The equations are adjusted by replacing $r_d$ by $r_d/|R_{eff} = \bar{r}_d$. The frequency of oscillation is therefore unaffected while the loop gain condition (12.59) becomes

$$\frac{M}{L} g_m r_d = 1 \quad (12.62)$$

**Example 12.8** Design an LC resonant oscillator to operate at 31.8 kHz. Use a 2N3819 JFET and a 15-volt supply.

**Solution** For the 2N3819, $V_P = -3$ V, $I_{DSS} = 10$ mA, and $r_d = 50$ k. Choose $I_D = 1$ mA for the JFET operating current. Then using Shockley’s equation,

$$R_S = \left(\sqrt{\frac{I_D}{I_{DSS}}} - 1\right) \frac{V_P}{I_D} = \left(\sqrt{\frac{1}{10}} - 1\right) \frac{3}{1} = 2.1 \text{ k}$$

$C_S$ is chosen to have a reactance that is low (one tenth or less) compared with $R_S$ at the lowest frequency of operation. Use $C_S = 1 \mu$F. The transconductance $g_m$ of the FET at this current is using Shockley’s equation given by
For \( C = 1000 \text{ pF} \), (12.58) gives \( L = 25 \text{ mH} \). Hence, \( \frac{M}{L} \geq \frac{1}{g_{m}f_{d}} = 0.009 \). In order to ensure oscillation in the simulation, \( M \) was set at \( 10 \text{ mH} \) and the gain of the amplifier reduced by bypassing only half of \( R_{S} \). The system oscillated at 29.3 kHz with amplitude of 24.2 V peak to peak.

The LC resonant oscillator may be implemented using a special current feedback amplifier, the AD844, in which access to the compensation node is available. This is shown in Fig. 12.19. The Barkhausen criterion gives

\[
A_{\beta} = \frac{r_{z} \| jX_{L} \| - jX_{C}}{R_{3} + r_{x}} \rho = \frac{\rho}{R_{3} + r_{x} + r_{z} + \frac{\rho}{X_{L}}} = 1 \angle 0^\circ
\]

(12.63)

where

\[
\beta = \frac{R_{1}}{R_{1} + R_{2}}
\]

(12.64)

and \( r_{x} \) and \( r_{z} \) are parameters of the AD844. From (12.63), it follows that the imaginary component of \( A_{\beta} \) must be zero, i.e.

\[
X_{L} = X_{C}
\]

(12.65)

giving

\[
f_{o} = \frac{1}{2\pi \sqrt{LC}}
\]

(12.66)
At the frequency of oscillation, $A\beta(f_o) = 1$, i.e.

$$\frac{R_1}{R_1 + R_2 R_3 + r_x} = 1$$

(12.67)

In this implementation, the amplifier produces zero phase shift at $f_o$, and, hence, no further signal inversion is required. The signal is fed back to the noninverting input of the current feedback amplifier.

**Example 12.9** Design an LC resonant oscillator using the AD844 to operate at 1 kHz.

**Solution** For a frequency of 1 kHz, choose $C = 0.005 \mu$F. Then using (12.66), we get $L = 5$ H. Condition (12.67) gives $\frac{R_1}{R_1 + R_2} \cdot \frac{r_z}{R_3 + r_x} = 1$. For the AD844, $r_z = 3 \times 10^6 \Omega$ and $r_x = 50 \Omega$. Choose $R_1 = 1$ k$\Omega$, $R_2 = 2$ k$\Omega$ and hence $R_3 = 500$ k$\Omega$. This circuit was simulated and the frequency of oscillation was measured at 980 Hz. The primary advantage of this implementation is that a coupling transformer is not required.

### 12.3.2 Colpitts and Hartley Oscillators
The Colpitts and Hartley oscillators can be represented in the general form shown in Fig. 12.20. The active device may be a FET or operational amplifier with high input impedance. Its gain with no load is $A_v$ and its output impedance $R_o$. The equivalent circuit is shown. The load impedance $Z_L$ consists of $Z_2$ in parallel with a series combination $Z_1$ and $Z_3$. Feedback to the amplifier is taken from the junction of $Z_1$ and $Z_3$. The gain $A$ of the forward loop is given by

$$\frac{V_o}{V_i} = 1 + \frac{R_2}{R_1}$$

(12.68)

where $Z_L$ is the load impedance. The feedback factor $\beta$ is given by

$$\beta = \frac{Z_1}{Z_1 + Z_3}$$

(12.69)

Fig. 12.20  Generalized Colpitts–Hartley oscillator

Hence the loop gain $A\beta$ is

$$A\beta = \frac{-A_vZ_L}{Z_L + R_o} \cdot \frac{Z_1}{Z_1 + Z_3}$$

(12.70)

where
\[ Z_L = Z_2 \parallel (Z_1 + Z_3) = \frac{Z_2 (Z_1 + Z_3)}{Z_1 + Z_2 + Z_3} = \frac{Z_2 (Z_1 + Z_3)}{\Sigma Z} \quad (12.71) \]

therefore

\[
A\beta = \frac{-A_v \frac{Z_2 (Z_1 + Z_3)}{\Sigma Z} \cdot Z_1}{R_o + \frac{Z_2 (Z_1 + Z_3)}{\Sigma Z} \cdot Z_1 + Z_3} = \frac{R_o (Z_1 + Z_2 + Z_3) + Z_2 (Z_1 + Z_3)}{R_o (Z_1 + Z_2 + Z_3) + Z_2 (Z_1 + Z_3)} \quad (12.72)
\]

If the load impedance are pure reactances (either inductive or capacitive), then \( Z_1 = jX_1, Z_2 = jX_2 \) and \( Z_3 = jX_3 \). For an inductor, \( X = \omega L \), and for a capacitor \( X = -1/\omega C \). Then

\[
A\beta = \frac{A_v X_1 X_2}{jR_o (X_1 + X_2 + X_3) - X_2 (X_1 + X_3)} \quad (12.73)
\]

For zero phase shift around the loop, the imaginary component in \( A\beta \) must go to zero, i.e.

\[
X_1 + X_2 + X_3 = 0 \quad (12.74)
\]

giving

\[
A\beta = \frac{A_v X_1 X_2}{-X_2 (X_1 + X_3)} = \frac{-A_v X_1}{X_1 + X_3} \quad (12.75)
\]

From \( \Sigma X = 0 \), it follows that the circuit will oscillate at the resonant frequency of the series combination of \( X_1, X_2, \) and \( X_3 \). Using \( \Sigma X = 0 \),

\[
A\beta = A_v \frac{X_1}{X_2} \quad (12.76)
\]

Since \( A\beta \) must be positive and at least unity in magnitude, then \( X_1 \) and \( X_2 \) must have the same sign. This means that they must be the same kind of reactance, either both inductive or both capacitive. Then \( X_3 = -(X_1 + X_2) \) must be inductive if \( X_1 \) and \( X_2 \) are capacitive or vice versa. If \( X_1 \) and \( X_2 \) are capacitors and \( X_3 \) is an inductor, the circuit is called a
Colpitts oscillator. If $X_1$ and $X_2$ are inductors and $X_3$ is a capacitor, the circuit is called a Hartley oscillator. These circuits can be implemented using BJT technology, but the low input impedance makes the analysis more difficult.

For the Colpitts oscillator in Fig. 12.21 where $X_1$ and $X_2$ are capacitors of equal value, the condition (12.74) gives

$$f_L = \frac{1}{2\pi (R_L + Z_i) C_o} \quad (12.77)$$

yielding

$$f_o = \frac{\sqrt{2}}{2\pi \sqrt{LC}} \quad (12.78)$$

![Colpitts oscillator](image)

**Fig. 12.21** Colpitts oscillator

Hence

$$I_{R_2} = 0.7/R_2 \quad (12.79)$$
If the amplifier is a FET, then $A_v = g_m R_D$ and therefore $g_m R_D \geq 1$ for oscillation. Note that at $f_o$,

$$\beta = \frac{Z_1}{Z_1 + Z_3} = -1$$ \hspace{1cm} (12.80)

Inclusion of $R_o$ is necessary to enable identification of the condition for oscillation.

For the Hartley oscillator in Fig. 12.22, $X_1$ and $X_2$ are inductors and the condition (12.74) gives

$$\omega L + \omega L - \frac{1}{\omega C} = 0$$ \hspace{1cm} (12.81)

giving

$$f_o = \frac{1}{2\pi \sqrt{2LC}}$$ \hspace{1cm} (12.82)

and $A_v \geq 1$ for oscillation.
**Example 12.10**  Design a Hartley oscillator to operate at 35.6 kHz using a 2N3819 JFET. Use a supply voltage of 15 V.

**Solution**  Using a 2N3819 n-channel JFET, we choose a 1 mA drain current. Then, as in Example 12.8, $R_s = 2.1 \, \text{k}\Omega$ and $C_s$ is chosen to be 1 $\mu$F. Hence, for $V_{DD} = 15 \, \text{V}$ and $V_{RS} = 2.1 \, \text{V}$, then for maximum symmetrical swing, $V_{DS} = (15 - 2.1)/2 = 6.45 \, \text{V}$ giving $R_D = 6.45 \, \text{k}$. Use a 5.6 k resistor. Note that no biasing resistor is needed since the gate is grounded through $L$. The coupling capacitor $C_D$ is chosen to be 1 $\mu$F so that its impedance compared to $R_D$ is small. Using (12.82), for $f = 35.6 \, \text{kHz}$ and $C = 0.001 \, \mu$F, $L = 10 \, \text{mH}$. Since $g_mR_D = 2.2 \times 5.6 = 12.3 \geq 1$ the circuit will oscillate. Under simulation the circuit oscillated at 32 kHz with amplitude of 8 V peak to peak. For effective oscillation in the simulation, the gain of the amplifier was reduced by introducing local feedback at the source of the FET.

**Example 12.11**  Design a Colpitts oscillator to oscillate at 31.8 kHz using a 2N3819 JFET. Use a supply voltage of 15 V.

**Solution**  For $I_D = 1 \, \text{mA}$, Shockley’s equation gives $R_S = 2.1 \, \text{k}$. $C_S = 1 \, \mu$F is chosen. Also, $R_G = 1 \, \text{M}$ is used to ground the gate while giving it a high input impedance. Using (12.78), for $C = 0.005 \, \mu$F, then $L = 10 \, \text{mH}$. Since $g_mR_D = 12.3 \geq 1$, the circuit will oscillate. $C_D = 1 \, \mu$F is a coupling capacitor. The circuit was simulated in the laboratory, and $f_o$ was measured at 31 kHz. In order to reduce the distortion, the FET gain may be reduced by only bypassing a part of $R_S$.

### 12.3.3 Clapp Oscillator

The Clapp oscillator shown in Fig. 12.23 is a variation of the Colpitts oscillator in which the tuning element is an inductor $L$ in series with a capacitor $C_T$ across the normal dual capacitor arrangement of the Colpitts.
Thus, \( Z_1 \) and \( Z_2 \) are capacitors, and \( Z_3 \) is an inductor in series with a capacitor. For this circuit, the loop gain is given by

\[
A\beta = \frac{-A_V Z_1 Z_2}{R_o (Z_1 + Z_2 + Z_3) + Z_2 (Z_1 + Z_3)}
\]

where \( Z_1 \) and \( Z_2 \) are capacitors \( C \) and \( Z_3 \) is an inductor \( L \) in series with a capacitor \( C_T \). Substituting \( Z_1 = jX_C \), \( Z_2 = jX_C \), and \( Z_3 = j(X_L + X_{CT}) \) in (12.83) results in

\[
A\beta = \frac{A_V X_C X_C}{jR_o (2X_C + X_L + X_{CT}) - X_C (X_C + X_L + X_{CT})}
\]

(12.84)

For zero phase shift around the loop, then

\[
2X_C + X_L + X_{CT} = 0
\]

(12.85)

Substituting this in (12.84) results in the condition \( A_v \geq 1 \). Note that (12.85) yields

(12.86)
The capacitor $C_T$ enables easy tuning of the oscillator.

**Example 12.12** Evaluate the frequency of oscillation of the resulting Clapp oscillator by the introduction of a capacitor $C_T = 0.01 \, \mu F$ in the Colpitts oscillator of Example 12.11.

**Solution** Using Eq. (12.86), $C_T = 0.01 \, \mu F$ along with $C = 0.005 \, \mu F$ and $L = 10 \, \text{mH}$ gives $f_0 = 35.6 \, \text{kHz}$. The simulated circuit oscillated at 34 kHz with amplitude 7.3 V peak to peak.

**12.3.4 Simple LC Oscillator**

The LC oscillator shown in Fig. 12.24 utilizes an $LC$ tank circuit in the positive feedback loop of an amplifier. At the resonant frequency of the circuit, the impedance becomes (i) very large such that positive feedback is maximum and (ii) resistive such that the phase shift of the feedback signal is zero. Hence, since the phase shift produced by the amplifier is zero, the conditions for oscillation can be met. The loop gain is given by

$$A\beta = \frac{Z_{LC}}{R + Z_{LC}} \cdot \frac{R_1 + R_2}{R_1} \quad (12.87)$$

where

$$Z_{LC} = \frac{jX_L(-jX_C)}{jX_L - jX_C} \quad (12.88)$$
At the resonant frequency $\omega_o$

$$jX_L - jX_C = 0 \tag{12.89}$$

giving

$$Q = \frac{R_1}{\beta(2R_1 + R_x)} = \frac{1}{\beta(2 + k)} \tag{12.90}$$

At this frequency, from (12.87) the loop gain goes to

$$A_V = \frac{V_o}{V_i} = g_m R_L \tag{12.91}$$

**Example 12.13** Design a simple LC oscillator to oscillate at a frequency of 1 kHz, using an LF351 op-amp.

**Solution** Using an LF351 op-amp, we choose $L = 5$ H. Then, (12.90) gives $C = 0.005 \mu F$ with $R = 1$ k$\Omega$. Then based on (12.91), we select $R_2 = 1$ k$\Omega$ and $R_1 = 500$ k$\Omega$. This circuit was simulated and oscillated at 1 kHz with amplitude of 13.5 V peak. Note that the loop gain was set close to one to avoid undue waveform clipping.
There are many variations of LC-type oscillators that can be explored. Many of these can be implemented using BJT technology, and the reader is encouraged to explore some of these circuits.

12.4 Crystal Oscillators

Apart from RC and LC circuits, crystals also represent a frequency-dependent circuit. A small crystal, normally made using quartz, is mounted under tension in a mechanical frame. Stress is applied to create a natural mechanical resonant frequency of vibration, which depends on both crystal properties and characteristics of the mount. Quartz possesses the piezoelectric property, i.e., it generates electricity when the material is subjected to pressure. Thus, when a piezoelectric crystal is mechanically deformed, a voltage appears across its faces. Inversely, when a voltage is applied to the faces of the crystal, the crystal will mechanically deform.

Because quartz is piezoelectric in a circuit, a mechanical–electrical interaction can occur with the crystal. These characteristics provide the device with an equivalent circuit as shown in Fig. 12.25. It comprises a series $RLC$ circuit in parallel with a capacitor. The reactance characteristic is shown in Fig. 12.26. It has both series resonance frequency $f_s$ and parallel resonance frequency $f_p$. At the series resonance, the inductive reactance cancels the capacitive reactance, and the resulting impedance is resistive and at a minimum. The parallel resonant frequency occurs a few kilohertz higher, and the crystal impedance is at a maximum. The fundamental frequency or frequency of operation and the load capacitance in the case of parallel resonance must be specified. The fundamental frequency is usually between 500 kHz and 20 MHz and is usually parallel resonance. It is difficult to make crystals operating at higher frequencies. Below about 500 kHz, the fundamental frequency is usually series resonance, which is more stable.
The electrical characteristics of the crystal can be determined by considering the equivalent circuit of the crystal. The two parameters $L_s$ and $C_s$ are set by the mechanical properties of the crystal. The damping is represented by $R_s$ which is small while the capacitance of the electrodes is represented by $C_p$. Typical values for these parameters in a 4 MHz crystal are as follows: $L_s = 100$ mH, $C_s = 0.015$ pF, $R_s = 100$ Ω, $C_p = 5$ pF, and $Q = 25,000$. The impedance of the circuit in Fig. 12.25 is given by

\[(12.92)\]
Since $R_s$ is small, this reduces to

$$Z_{cry} = \left(\frac{1}{sC_s} + \frac{R_s}{sL_s}\right) + \frac{1 - \omega^2 C_s L_s + j\omega C_s R_s}{-R_s C_s C_p + j\omega \left(C_s + C_p - \omega^2 C_s C_p L_s\right)}$$

(12.93)

From Eq. (12.92), the crystal has two resonant frequencies. The series-resonant frequency $\omega_s$ corresponds to $Z_{cry} = 0$ which is obtained by setting the numerator in (12.93) to zero. This gives

$$\omega_s = \frac{1}{\sqrt{L_s C_s}} \quad \text{or} \quad f_s = \frac{1}{2\pi \sqrt{L_s C_s}}$$

(12.94)

The parallel resonance frequency $\omega_p$ corresponds to $Z_{cry} = \infty$ which is obtained by setting the denominator in (12.93) to zero. This results in

$$\omega_p = \frac{1}{\sqrt{L_s C_s}} \sqrt{1 + \frac{C_s}{C_p}} \quad \text{or} \quad f_p = \frac{1}{2\pi \sqrt{L_s C_s}} \sqrt{1 + \frac{C_s}{C_p}}$$

(12.95)

Note that $f_p > f_s$. From (12.94), it is clear that the series-resonant frequency is determined solely by the parameters $L_s$ and $C_s$, which are well defined by the crystal. From (12.95), however, the parallel resonant frequency is dependent on the electrode capacitance $C_p$ that is susceptible to variations.

**12.4.1 Crystal Oscillator Using an Op-Amp**

In the circuit shown in Fig. 12.27, the crystal, along with resistor $R$, provides positive feedback around the operational amplifier. The loop gain is given by

$$A\beta = \left(1 + \frac{R_2}{R_1}\right) \cdot \frac{Z_{cry}}{R + Z_{cry}}$$

(12.96)
Near parallel resonance, which is set for a given crystal, $|Z_{cry}|$ is large resulting in $\frac{Z_{cry}}{R+Z_{cry}} \approx 1$, and the phase shift is zero. At other frequencies, $|Z_{cry}|$ falls and $A\beta = 1$ is not met. Hence, for oscillation at the crystal resonant frequency $f_o$

$$A\beta \approx \left(1 + \frac{R_2}{R_3}\right) \geq 1 \quad (12.97)$$

The operation of this circuit is similar to the simple LC oscillator; the crystal effectively replaces the $LC$ tank circuit of that oscillator.

**Example 12.14** Design a crystal oscillator to oscillate at 100 kHz using a suitable operational amplifier.

**Solution** Using a suitable operational amplifier and a 100 kHz crystal, the circuit was configured using $R_1 = 1 \text{k}\Omega$, $R_2 = 1 \text{k}\Omega$, and $R = 1 \text{k}\Omega$. Note that the amplifier gain $A = 2$ ensures that $A\beta > 1$ and hence that oscillation occurs.

**12.4.2 Miller Oscillator**
A simple crystal oscillator making use of the natural oscillations of the crystal is the Miller oscillator shown in Fig. 12.28. The output of the crystal is used to drive a tuned amplifier. The load of the amplifier consists of an LC circuit tuned approximately to the crystal frequency. The design procedure is quite straightforward. At the resonant frequency of the tank circuit

\[ jX_L - jX_C = 0 \]  

(12.98)

giving

\[ Q = \frac{R_1}{\beta (2R_1 + R_x)} = \frac{1}{\beta (2 + k)} \]  

(12.99)

**Example 12.15**  Design a Miller oscillator using a 2N3819 JFET to oscillate at 100 kHz. Use a 15V supply.

**Solution**  The bias resistor \( R_2 \) as well as the bypass capacitor \( C_1 \) can be the same values as those in the LC-tuned oscillator. The drain current is therefore 1 mA. The gate bias resistor \( R_1 \) is chosen to be 1 MΩ. Using (12.99), for \( L = 1 \) mH, \( C = 2.53 \) nF. A 100 kHz crystal must be used at the
input of the circuit. In order that oscillations begin, this circuit relies on Miller feedback capacitance between the drain and gate of the FET.

### 12.4.3 Clapp Oscillator with Crystal Control

The resonant frequency of an *LC* oscillator can be stabilized by the appropriate inclusion of a crystal. In such an application, it is preferable to operate the crystal in its series resonance rather than parallel resonance mode as this provides better frequency stability. The circuit of Fig. 12.29 illustrates the use of a crystal to improve the frequency stability of a Clapp oscillator discussed in Sect. 12.3.3.

![Clapp oscillator with crystal control](image)

**Fig. 12.29** Clapp oscillator with crystal control

### 12.4.4 Pierce Crystal Oscillator

This oscillator, shown in Fig. 12.30, involves the incorporation of a crystal in the *LC* resonant oscillator to improve its stability. The crystal permits feedback only at the series-resonant frequency when the impedance is near zero.
12.4.5 AD844 Crystal Oscillator

The $LC$ resonant oscillator of Fig. 12.19 involving the AD844 may be implemented using a crystal instead of the $LC$ tank circuit. This circuit is shown in Fig. 12.31. The design equations of the original circuit apply with the parallel resonant frequency of the crystal being operational. As a result, the output of the circuit will be a maximum at the parallel resonant frequency of the crystal.
12.5 Frequency Stability

The frequency of an oscillator will tend to drift from its design frequency as a result of aging, temperature changes, and other factors. The frequency stability of an oscillator is a measure of its ability to maintain its frequency over time. The frequency of oscillation is usually determined by a small number of components, and this enables reasonable levels of stability to be achieved. In these frequency-determining components, the ratio $d\theta/d\omega$ is a measure of the phase shift as a function of frequency change. In a circuit where this parameter is large, then if phase changes introduced by other circuit elements, as the frequency changes to satisfy the Barkhausen criterion, the phase shift introduced by the frequency-determining components as a result of the frequency change is large, and hence only a small shift in frequency results. Thus, for frequency-determining components with large $d\theta/d\omega$, the frequency stability is high. LC-tuned circuits and crystals tend to have large $d\theta/d\omega$ at $f_o$ and hence excellent frequency stability.

12.6 Amplitude Stabilization

The Barkhausen criterion includes the condition that the loop gain must be equal to unity for oscillation, i.e., $A\beta = 1$. If $A\beta < 1$, the circuit ceases to oscillate. Since $A\beta = 1$ is not practical, $A\beta > 1$ has to be set in order to ensure that oscillation is sustained. The extent to which the loop gain is greater than unity largely determines the amplitude of the output waveform. Without appropriate amplitude control, this amplitude will increase indefinitely thereby producing extreme levels of distortion as the amplifier saturates. In such circumstances, the output progressively changes from a sinusoidal waveform to a square wave as the loop gain exceeds unity.

For a value of loop gain marginally above the critical value of unity, the output amplitude increases. However, as the nonlinear region of the amplifier is entered, the amplifier gain drops, and the output is reduced, causing the amplifier to return to the linear region, this in turn causes an increase in amplifier gain. A dynamic point may be reached where the nonlinearity reduces the gain such that oscillation is
sustained with a stable amplitude and low distortion. Adjusting the loop gain manually to achieve this is extremely difficult. Automatic gain control can be introduced by using a thermally sensitive nonlinear device as one of the gain-setting components of the associated amplifier. Thus, amplitude increase would cause heating and hence resistance increase (sensor) or decrease (thermistor) that can be used to regulate oscillator output amplitude. Examples of this amplitude control are shown in the Wien bridge oscillator.

Figure 12.32 illustrates amplitude control in a Wien bridge oscillator using the R53 thermistor. This device, though now rare, has suitable negative temperature coefficient characteristics for use in this application. In the particular case where $A > 3$, $R_1$ needs to be between 600 $\Omega$ and 1 k$\Omega$. Thus, as the amplitude of the output signal increases, more current flows into R53 resulting in heating. As a result, the resistance of the thermistor decreases, and hence the amplifier gain also decreases. The overall effect is a reduction in the amplitude of the output signal. Conversely, a falling output signal causes a decrease of the heating in R53 and hence an increase in its resistance. The overall effect is an increase in the amplifier gain resulting in the increase of the amplitude of the output signal. A dynamic equilibrium is reached where the output signal is approximately constant.
Figure 12.32 Thermistor amplitude stabilization

Figure 12.33 illustrates amplitude control in a Wien bridge oscillator using a sensistor, specifically a low-voltage incandescent lamp, a cheaper alternative to the R53. Note that the lamp replaces $R_1$ in the negative feedback loop. Thus, if the output signal increases, the lamp is heated and its resistance increases. As a result, the amplifier gain is reduced thereby reducing the amplitude of the output signal. The converse occurs for a decrease in signal amplitude and the overall effect is the stabilization of the output signal amplitude. Typically, the lamp is a low-voltage medium-current device. The value of $R_2$ depends on the characteristics of the specific lamp but is likely to be in the range 250 Ω to 1 kΩ.
A third amplitude stabilization technique is the use of an electronically variable resistor such as a FET, in conjunction with $R_1$ and $R_2$ to set the amplifier gain. The scheme is shown in Fig. 12.34. It utilizes the fact that over a limited range of drain–source voltage, a JFET behaves as a variable resistor. It operates as follows: At turn-on, the gate resistor $R_g$ biases the FET on (zero gate–source voltage) such that with a drain–source voltage less than pinch-off, the drain–source resistance is low. The gain of the oscillator amplifier is therefore set by $R_1$ and $R_2$ giving a gain greater than three; oscillation therefore begins. The sinusoidal output signal is amplified by the control amplifier A then half-wave rectified by diode $D_1$. 

Fig. 12.33  Sensistor amplitude stabilization
This signal is then filtered by $C_1$, and the resulting negative DC voltage is applied to the gate of the JFET to reverse bias it. This increases the channel resistance of the FET and as a result reduces the gain of the oscillator amplifier. The amplitude of the negative DC voltage is proportional to the amplitude of the sinusoidal signal, and the actual value that is applied to the gate of the FET is adjusted until a stable output signal is obtained. This circuit works very well and maintains constant output amplitude over a wide frequency range. For proper operation the amplitude of the signal across the FET must maintain it in the ohmic region.

### 12.7 Oscillator Creation

Having discussed the principle of operation of an oscillator and the Barkhausen criterion, it is possible to create “new” oscillator structures by employing these principles.

**Oscillator 1:** A simple illustration of this is the use of an all-pass filter network to realize an oscillator structure. Each of the cascaded stages in Fig. 12.35 is an all-pass filter. Its transfer function is given by $H(s) = \frac{1-Ts}{1+Ts}$ where $T = RC$. It has the unique feature of unity gain and...
varying phase with changing frequency. The phase varies from 0° to 180°, and hence the Barkhausen criterion can be easily met by combining three all-pass stages as shown.

![Oscillator using all-pass filters](image)

**Fig. 12.35** Oscillator using all-pass filters

The Barkhausen criterion gives

\[ A\beta = \left( \frac{1 - Ts}{1 + Ts} \right)^3 = 1 \]  \hspace{1cm} (12.100)

which is equivalent to

\[ P_D \geq V_Z I_{Z_{\text{max}}} \]  \hspace{1cm} (12.101)

and

\[ t_{gr} = \frac{1}{\pi f_o}, f \ll f_o \]  \hspace{1cm} (12.102)

Since \(|H(s)| = 1\) in the all-pass network, condition (12.101) is satisfied. From condition (12.102)

\[ V_o = 0.5 \times \left(1 + \frac{3}{1}\right) = 2 \text{ V} \]  \hspace{1cm} (12.103)

from which the oscillation frequency is given by

\[ f_o = \frac{1}{2\pi RC} \tan \left(\frac{\pi}{3}\right) = \frac{\sqrt{3}}{2\pi RC} \]  \hspace{1cm} (12.104)
This circuit was tested using LF351 operational amplifiers. All resistors were set to 10 kΩ and C was set at 0.01 μF. From (12.104), we get 
\[ f_o = \frac{\sqrt{3}}{2\pi \times 10 \times 10^2 \times 0.01 \times 10^{-6}} = 2757 \text{ Hz}. \] The system was tested in the laboratory and oscillated at 2756 Hz the calculated frequency.

**Exercise 12.1** Show that for four all-pass networks, the frequency of oscillation is \( f_o = \frac{1}{2\pi RC} \).

**Oscillator 2:** Another oscillator can be created using the network shown in Fig. 12.36. The simple interchange of a capacitor and a resistor in a twin-T network changes a band-stop response into a bandpass response. For this network, using nodal analysis the transfer function is given by

\[
\frac{V_o}{V_i} = \frac{nsCR(m+n+1)}{n(sCR)^2 + sCR(mn+n^2+m+1) + n}
\]

(12.105)

**Fig. 12.36** RC network

Setting \( s = j\omega \), then at a frequency \( \omega_0 = 1/RC \) corresponding to \( f_o = 1/2\pi RC \), the transfer function becomes.

\[
\frac{V_o}{V_i}(f_o) = \frac{n(1+m+n)}{1+m+mn+n^2}
\]

(12.106)
Since the transfer function in (12.106) is real, this indicates that the phase shift introduced by the network is zero at $f_o$. If $n = 3$ and $m = 0.2$, then

$$\frac{V_o}{V_i}(f_o) = \frac{n (1 + m + n)}{1 + m + mn + n^2} = \frac{3 (1 + 0.2 + 3)}{1 + 0.2 + 0.2 \times 3 + 3^2} = 1.16 \quad (12.107)$$

This means that the network produces an output that is greater than the input at the frequency $f_o$ at which the phase shift is zero. This network can therefore be used with an emitter follower to produce oscillation providing the gain of the emitter follower is greater than $1/1.16 = 0.862$ which ensures that the Barkhausen criterion for oscillation is satisfied. A simple application is shown in Fig. 12.37. The output of the network drives the input of the emitter follower while the output of the emitter follower drives the input of the network. At the single frequency $f_o$ the signal phase shift is zero while the loop gain is greater than unity and therefore oscillation occurs. The potentiometer sets the loop gain for minimum distortion while sustaining oscillation. The load at the output of the emitter follower must be high so that its gain is not reduced below 0.862. The transistor is biased using $R_4 = 16.8 \, k$ and $R_3 = 16.8 \, k$ through $R_1 = 42 \, k$. Since resistor $R_4$ is grounded through the power supply, resistor $R$ of the network comprises $R = R_3//R_4 = 8.4 \, k$. Hence, $R_2 = R/n = 8.4 \, k/3 = 2.8 \, k$, and $R_1 = R/m = 8.4 \, k/0.2 = 42 \, k$. For $C = 0.01 \, \mu F$, then $C_1 = nC = 3 \times 0.01 = 0.03 \, \mu F$ and $C_2 = mC = 0.2 \times 0.01 = 0.002 \, \mu F$. The resulting frequency of oscillation is $f_o = 1/2\pi RC = 1/2\pi \times 8.4 \times 10^3 \times 0.01 \times 10^{-6} = 1895 \, Hz.$
Exercise 12.2   Design an oscillator using $n = 2$ and $m = 0.5$.

Oscillator 3: The oscillator shown in Fig. 12.38 is based on the Colpitts circuit but here using an emitter follower which has gain less than unity instead of an inverting amplifier with gain greater than unity. The model shown in Fig. 12.39 representing this oscillator now contains a noninverting $A_v$ instead of an inverting amplifier as discussed in the Colpitts–Hartley system in Fig. 12.20.
Thus, the system loop gain is given by

\[ A\beta = \frac{A_v X_1}{X_1 + X_3} = -\frac{A_v X_1}{X_2} \]  \hspace{1cm} (12.108)

where
\[ X_1 + X_2 + X_3 = 0 \]  \hspace{2cm} (12.109)

In order to satisfy the Barkhausen criterion for oscillation, \( A\beta > 1 \), and therefore \( X_1 \) and \( X_2 \) must have different signs. Let \( X_1 = \omega L_1 \) and \( X_2 = -\frac{1}{\omega C_2} \). Then,

\[ A\beta = -A_v \frac{\omega L_1}{-\frac{1}{\omega C_2}} = A_v \omega^2 L_1 C_2 > 1 \]  \hspace{2cm} (12.110)

Since \( A_v \) is only slightly less than unity, this condition reduces to

\[ \omega^2 L_1 C_2 > 1 \]  \hspace{2cm} (12.111)

From (12.109), \( X_3 = -(X_1 + X_2) \). For \( X_3 = -\frac{1}{\omega C_3} \), then \(-\frac{1}{\omega C_3} = -\omega L_1 + \frac{1}{\omega C_2} \), and therefore the frequency of oscillation is given by

\[ \omega_o = \frac{1}{\sqrt{L_1 C_T}}, \quad f_o = \frac{1}{2\pi \sqrt{L_1 C_T}} \]  \hspace{2cm} (12.112)

where \( C_T = \frac{C_2 C_3}{C_2 + C_3} \). Using \( R_1 = 470 \, k \) and \( R_2 = 4.7 \, k \) to bias the transistor, with coupling capacitors \( C_1 = C_4 = 0.1 \, \mu F \), then for \( C_2 = C_3 = 1 \, nF \) and \( L_1 = 1 \, mH \), we get \( f_o = \frac{1}{2\pi \sqrt{10^{-3} \times 0.5 \times 10^{-9}}} = 225 \, kHz \). The frequency of oscillation using simulation software was measured at 215 kHz. Note that using (12.112), (12.111) becomes

\[ \omega^2 L_1 C_2 = \frac{L_1 C_2}{L_1 C_T} = \frac{C_2}{C_T} > 1 \]. Therefore, the Barkhausen criterion is generally satisfied.

**Exercise 12.3** Show that if \( X_1 \) and \( X_3 \) are capacitors and \( X_2 \) is an inductor, while \( X_1 \) and \( X_2 \) have different signs as required, the system will not oscillate.

### 12.8 Applications

Oscillators producing sinusoidal outputs are used in a wide range of applications including laboratory testing, communications, and
reference standards. In laboratory testing, a sinusoidal generator is a standard piece of equipment. It is used for determining the frequency and phase response of amplifiers and other signal processing circuits. This enables the transfer function of the circuit to be determined and also gives an indication of the stability of the circuit, particularly under varying loads. The sine-wave generator is also used for troubleshooting as it can be injected into a circuit at different points and monitored at others.

Another extremely important application of sine-wave generators is in communication systems. In radio transmitters, information to be transmitted is superimposed on a sinusoidal signal called a carrier. The resulting modulated carrier signal is then amplified and radiated through radio antennas as radio waves. In radio receivers, this radio wave induces an electrical signal in a receiving antenna. It is then mixed with a sinusoidal signal produced by a local oscillator and the resulting lower-frequency signal processed by the receiver circuitry to extract the information. This mixing technique has long formed the basis of super heterodyne receivers. Sinusoidal oscillators are also used in standard frequency sources and in the production of synthesized music.

### 12.8.1 Wide-Range Wien Bridge Oscillator

The Wien bridge oscillator circuit in Fig. 12.40 uses the LF351 JFET input op-amp and is intended for laboratory use. It covers the frequency range 15 Hz – 150 kHz in four bands. It is a simple system and the frequency is easily varied over a wide frequency range using the switched banks of capacitors and the ganged variable potentiometer. The components of the Wien network giving the frequency ranges shown are selected using Eq. (12.11). Fixed resistors $R_a = 1 \text{k}$ are used to set the minimum value of $R$, and a dual 10 k linear potentiometer is used for $VR_a$ as the remaining part of $R$. This arrangement provides continuous variation within a band set by a pair of equal capacitors $C$. Values of $C$ of 1 μF, 0.1 μF, 0.01 μF, and 0.001 μF establish four bands. By switching in different equal pairs of $C$ using the two-pole multithrow switch, four frequency bands can be realized, each allowing a decade change in frequency by varying the potentiometer. These bands are 15 Hz–150 Hz, 150 Hz – 1.5 kHz, 1.5 kHz–15 kHz, and 15 kHz–150 kHz.
The gain of the oscillator amplifier is set by $R_1$ and $R_2$ along with the channel resistance of the JFET. From its specifications, the 2N3819 for $V_{DS} < V_P$ has a channel resistance $r_d$ that varies between 100 $\Omega$ and 3.6 kΩ for $V_{GS}$ varying from 0 V to −2.5 V. Therefore, $R_2 = 20$ kΩ and $R_1 = 8$ kΩ result in gain variation from 3.4 when $r_d = 100$ $\Omega$ to 2.7 when $r_d = 3.6$ kΩ, inclusive of the critical value 3. The gate-biasing resistor $R_5$ is set at 1 MΩ. Capacitor $C_1$ is chosen to provide adequate filtering of the output ripple and thereby produces a DC voltage. Since $R_5$ is large, this capacitor need not be very large. It cannot be too large otherwise the time constant $R_5 C_1$ will prevent a quick response to varying amplitude changes. A compromise value of 2 $\mu$F is used. The diodes are small signal devices such as 1N4148. The output of the Wien bridge oscillator is low and the output amplifier opa3 is used to boost this signal by a factor of two by setting $R_3 = R_4 = 10$ kΩ. The control amplifier opa2 is set at a gain of 6 with $R_7 = 10$ kΩ and $R_6 = 2$ kΩ in order to provide sufficient drive for the half-wave rectifier. The potentiometer $VR_2 = 10$ kΩ provides a variable signal level to the control amplifier. The circuit is operated from
a ± 15 V supply. Resistors are 2% tolerance and all capacitors are polystyrene.

Ideas for Exploration: (i) Introduce another potentiometer in order to provide a variable output signal amplitude from the oscillator.

12.8.2 Wien Bridge Oscillator Using a 741 Op-Amp

The circuit in Fig. 12.41 uses the 741 op-amp in a simple Wien bridge oscillator. It uses the Wien network components as the previous case. An $R_{53}$ thermistor (if available) and resistor $R_1 = 470 \, \Omega$ produce the necessary gain of three with amplitude stabilization as a result of the action of the thermistor. Note however that the GBP of the 741 limits the upper frequency of operation of the circuit to less than $1 \, \text{MHz}/3 = 333 \, \text{kHz}$.

![Wien bridge oscillator using a 741 op-amp](image)

**Fig. 12.41** Wien bridge oscillator using a 741 op-amp

Ideas for Exploration: (i) The $R_{53}$ thermistor is difficult to find and appears to be no longer available. Use another approach to amplitude stabilization such as the low power incandescent lamp as shown in Fig. 12.42. In operation, potentiometer VR1 is adjusted for a maximum signal output of about 2 V. (ii) Examine a third approach to amplitude stabilization as shown in Fig. 12.43. Here the potentiometer is adjusted such that the output is just above zero. As signal amplitude build-up
takes place, eventually the diodes begin to conduct thereby limiting the amplifier gain and therefore constraining the signal amplitude.

Fig. 12.42 Amplitude stabilization using a low-power incandescent lamp

Fig. 12.43 Amplitude stabilization using signal diodes

12.8.3 Oscillator Using a JFET Input Amplifier
The Wien bridge oscillator shown in Fig. 12.44 uses discrete components with a MPF102 JFET at the input stage of the amplifier and is one of many configurations that can be used. The JFET presents a high input impedance to the Wien network thereby reducing damping on the Wein network and enabling the use of a high-value dual potentiometer for wide frequency variation (20 Hz–20 kHz) without capacitor switching. A ganged potentiometer $VR_a = 500$ kΩ is employed along with $R_a = 820$ Ω which sets a minimum value of $R$ in the Wien network. Capacitor $C = 0.01 \mu F$ in the Wien network gives a minimum frequency of 31 Hz and maximum frequency of 19.4 kHz. Potentiometer $VR_2 = 20$ kΩ sets the current in the JFET to a value that minimizes the distortion, and $C_4 = 100 \mu F$ bypasses this potentiometer for signals. In the absence of an R53 thermistor, amplitude stabilization is achieved using diodes in parallel with the feedback resistor.

![JFET Wien bridge oscillator circuit](image)

*Fig. 12.44*  JFET Wien bridge oscillator

*Ideas for Exploration:* (i) Design the oscillator using the JFET input amplifier of Fig. 7.54 in Chap. 7.
12.8.4 Wien Bridge Oscillator Using Two-Transistor Amplifier

The oscillator shown in Fig. 12.45 is based on the two-transistor feedback pair with gain discussed in Chap. 5. The design follows the principles discussed there and application of the Wien bridge oscillator principles. Transistors $Tr_1$ and $Tr_2$ constitute the feedback pair with the input at the base of $Tr_1$ and the output at the collector of $Tr_2$.

Potentiometer $VR_1 = 10 \, k$ along with bypass capacitor $C_1 = 100 \, \mu F$ and resistor $R_3 = 1.5 \, k$ sets the gain of the feedback pair at just over 3 for oscillation. The Wien network from output back to noninverting input comprises capacitors $C = 0.01 \, \mu F$ and resistor $R = 15 \, k$ which give frequency of oscillation $f_o = 1/2\pi \times 15 \times 10^3 \times 0.01 \times 10^{-6} = 1061$ Hz.

Note that point A is a signal ground. The voltage there is 1.4 V with current of about 1.4 mA supplied to the diodes by $R_1 = 5.6 \, k$. This is the approximate voltage applied at the base of $Tr_1$ with bias current to this transistor through one of the resistors $R = 15 \, k$ of the Wien network. (The base current through this resistor is small, and hence the voltage drop across this resistor is small.) The voltage at the emitter of $Tr_1$ is therefore 0.7 V. The current through $Tr_1$ is given by $0.7/R_2$. A value of $R_2 = 6.8 \, k$ gives a current through $Tr_1$ of 0.1 mA. The current through resistor $R_3 = 1.5 \, k$ (made up of currents of both transistors) is given by $0.7 \, V/1.5 \, k = 0.47$ mA. Therefore, the current through $Tr_2$ is $0.47-0.1 = 0.37$ mA. Noting that only the current of $Tr_2$ flows through the potentiometer, the voltage drop across the potentiometer is $0.37 \, mA \times 10 \, k = 3.7$ V. Hence, the DC voltage at the output is $0.7 + 3.7 = 4.4$ V which allows for maximum symmetrical swing. The low transistor currents in this circuit allow for operation from a 9 V battery.
I: Ideas for Exploration: (i) Introduce variable amplitude by including a 10 kΩ potentiometer after capacitor $C_2$ to ground with the output at the wiper; (ii) implement the circuit using the four-transistor amplifier of Chap. 7.

12.8.5 Phase-Shift Oscillator Using a JFET

The phase-shift oscillator shown in Fig. 12.46 uses a JFET in the common source mode at the input and an emitter follower at the output to provide a low-impedance drive capability. The JFET uses the self-bias mode with the quiescent current set at 1 mA by appropriate selection of $R_3$ with $VR_1 = 1$ kΩ. With a load resistor $R_1 = 6$ kΩ, the drain voltage is set at 9 V giving 8.3 V at the output of the emitter follower. Resistor $R_2 = 4.7$ kΩ sets a current of $8.3/4.7$ kΩ = 1.8 mA in the emitter follower. The potentiometer $VR_1 = 1$ kΩ enables variation of the gain such that oscillation results with minimum distortion. The phase-shift network uses $R = 6.5$ kΩ and $C = 0.01$ μF to give an oscillating frequency of 1 kHz.
**Ideas for Exploration:** (i) Examine the effect on distortion by introducing bootstrapping of the load resistor $R_1$. This would increase the gain of the JFET, and therefore the potentiometer would have to be adjusted to allow greater levels of local feedback in order to reduce the gain to just above 29.

### 12.8.6 Hartley Oscillator Using an Op-Amp

The circuit shown in Fig. 12.47 is a Hartley oscillator using a LF351 JFET op-amp in the inverting configuration. It is a simple application of the principle presented in Sect. 12.3.2. Here the input resistor $R_1$ is chosen to be 1 M to ensure a high input impedance as assumed in the
analysis of the oscillator. The feedback resistor $R_2 \approx 1M$ is chosen slightly greater than 1 M in order to enable oscillation. Using $f = \frac{1}{2\pi \sqrt{2LC}}$, then for $L = 10 \text{ mH}$ and $C = 0.001 \text{ } \mu\text{F}$, the frequency of oscillation is given by

$$f = \frac{1}{2\pi \sqrt{2 \times 10 \times 10^{-3} \times 0.001 \times 10^{-6}}} = 35.6 \text{ kHz}.$$ 

Fig. 12.47  Hartley oscillator using op-amp

Ideas for Exploration: (i) Explore the use of amplitude stabilization techniques in this circuit.

12.8.7 Colpitts Oscillator Using an Op-Amp
The circuit shown in Fig. 12.48 is a Colpitts oscillator using a LF351 JFET op-amp in the inverting configuration. It is also a simple application of the principle presented in Sect. 12.3.2. The input resistor $R_1$ is chosen to be 1 M to ensure a high input impedance as assumed in the theory of the oscillator and the feedback resistor $R_2 \approx 1M$ is chosen slightly greater than 1 M to ensure that oscillation results. Using $f = \frac{\sqrt{2}}{2\pi \sqrt{LC}}$, then for $L = 10 \text{ mH}$ and $C = 0.005 \text{ } \mu\text{F}$, the frequency of oscillation is given by

$$f = \frac{\sqrt{2}}{2\pi \sqrt{10 \times 10^{-3} \times 0.005 \times 10^{-6}}} = 31.8 \text{ kHz}.$$
Ideas for Exploration: (i) Explore the use of amplitude stabilization techniques in this circuit.

12.8.8 LC Resonant Oscillator Using a BJT
The circuit shown in Fig. 12.49 is an LC resonant oscillator implemented using a BJT. The lower input impedance of the BJT compared with the JFET means that the analysis of Sect. 12.3.1 needs to be modified to take this into account. Here, the transistor is biased by \( R_1 = 47 \, k \) and \( R_2 = 22 \, k \) which set the voltage at the base of the transistor at 4.7 V. This along with \( R_3 = 1 \, k \) sets the quiescent current in the BJT at 4 mA. With \( L = 100 \, mH \) and \( C = 100 \, pF \), the resonant frequency is given by \( f = \frac{1}{2\pi \sqrt{LC}} = 1.59 \, MHz \). The high transconductance of the BJT compared with the JFET ensures that oscillation occurs. Note that coupling capacitor \( C_2 \) and decoupling capacitors \( C_1 \) and \( C_3 \) can be smaller (typically 0.1 \( \mu F \) and less) because of the high frequency of operation.
Ideas for Exploration: (i) Replace $C$ by a variable trimmer capacitor and investigate the frequency variation that can be achieved.

12.8.9 Hartley Oscillator Using a BJT

The circuit shown in Fig. 12.50 is a Hartley oscillator implemented using a BJT. Again, the lower input impedance of the BJT compared with the JFET means that the analysis of Sect. 12.3.2 should be adjusted to accommodate this. Here, the transistor is biased using collector–base feedback biasing with $R_1 = 470 \text{k}$ and $R_2 = 4.7 \text{k}$. Capacitor $C_1 = 0.1 \text{µF}$ couples the output of the LC network to the input of the transistor while capacitor $C_2 = 0.1 \text{µF}$ couples the output of the transistor to the input of the network. With $L = 10 \text{mH}$ and $C = 1 \text{nF}$, the oscillating frequency is given by $f = \frac{1}{2\pi} \sqrt{2LC} = 32 \text{ kHz}$. 
Ideas for Exploration: (i) Replace the network capacitor $C$ by a variable trimmer capacitor and investigate the frequency variation that can be achieved.

12.8.10 Colpitts Oscillator Using a BJT

The circuit shown in Fig. 12.51 is a Colpitts oscillator implemented using a BJT. Here, the transistor is again biased using collector–base feedback biasing with $R_1 = 470$ k and $R_2 = 4.7$ k. Capacitor $C_1 = 0.1$ μF couples the output of the transistor amplifier to the input of the LC network. The output of the network is directly connected to the input of the transistor with no coupling capacitor being necessary. With $L = 10$ mH and $C = 5$ nF, the oscillating frequency is given by

$$f = \frac{\sqrt{2}}{2\pi} \sqrt{LC} = 31 \text{ kHz}.$$
Ideas for Exploration: (i) Examine the possibility of frequency variation by using a variable inductor. (ii) Introduce a capacitor in series with the inductor thereby converting the system into a Clapp oscillator. Compare the performance of the two systems. (iii) Replace the inductor by a series-resonant crystal (crystal-controlled Clapp oscillator), and examine the performance.

12.8.11 Crystal Oscillator 1
The circuit in Fig. 12.52 is an oscillator that employs a series-resonant crystal in a positive feedback loop around two transistor stages. The first stage around $Tr_1$ is a common base amplifier with the output of the crystal feeding into the transistor emitter. The output at the collector of $Tr_1$ is fed into the emitter follower stage $Tr_2$, the output of which feeds into the series-resonant crystal. Thus, at resonance the impedance of the crystal is at a minimum, and positive feedback is at a maximum. At all other frequencies, the impedance is higher and therefore oscillation occurs at the series-resonant frequency of the crystal. Resistors $R_1 = 47$ k and $R_2 = 12$ k set the base voltage of $Tr_1$ at 3 V. Therefore, with $R_4 = 1.2$ k, the current in the first stage is $2.3/1.2$ k = 1.9 mA. With
\( R_3 = 2.2 \, \text{k} \), the voltage at the base of the emitter follower is \( 15 - (1.9 \, \text{mA} \times 2.2 \, \text{k}) = 10.8 \, \text{V} \). Resistor \( R_5 = 2.2 \, \text{k} \) sets the current in \( \text{Tr}_2 \) at \( 10.1/2.2 \, \text{k} = 4.6 \, \text{mA} \). Capacitor \( C_2 \) works in conjunction with the crystal and is typically about 100 pF. This circuit operates with a wide range of crystals from 100 kHz to 10 MHz.

![Circuit Diagram](image)

*Fig. 12.52* Crystal oscillator using common base and common emitter amplifiers

*Ideas for Exploration:* (i) Try a range of crystals to test the functionality of this circuit.

### 12.8.12 Crystal Oscillator 2

The circuit in Fig. 12.53 is a Colpitts oscillator that employs a series-resonant crystal working into the Colpitts network. The tuned circuit is designed to resonate at the series-resonant frequency of the crystal, thereby ensuring stable oscillation at a single frequency. Here, the biasing arrangement is the same as before with \( R_1 = 470 \, \text{k} \) and \( R_2 = 4.7 \, \text{k} \). The output of the transistor amplifier drives the crystal which is connected to the input of the LC network. The output of the network is directly connected to the input of the transistor. The crystal frequency \( f_c \) is used in choosing \( L \) and \( C \) according to \( f_c = \sqrt{2/2\pi \sqrt{LC}} \).
Ideas for Exploration: (i) Try a range of crystals to test the functionality of this circuit.

12.8.13 Phase-Shift Oscillator Using a BJT

The circuit of Fig. 12.54 demonstrates a phase-shift oscillator using a BJT. The BJT is in the common emitter mode and is biased by \( R_1 = 43 \, \text{k} \) and \( R_2 = 10 \, \text{k} \), these setting a base voltage of 1.7 V. This base voltage in conjunction with \( VR_1 = 1 \, \text{k} \) sets the quiescent current at 1 mA. Collector resistor \( R_L = 3.9 \, \text{k} \) gives the circuit close to maximum symmetrical swing. The output at the collector drives the phase-shift network. Note that the last resistor of the network is made up of \( R_2 \) in parallel with \( R_1 \) and the input impedance at the transistor base. The potentiometer is adjusted for minimum visual distortion of the signal when viewed on an oscilloscope. This adjustment changes the gain of the amplifier so that it is just greater than 29.
Ideas for Exploration: (i) Introduce a direct coupled emitter follower at the output in order to drive low-impedance loads and not affect the gain of the system. Drive the phase-shift network from the output of the emitter follower. This should improve the accuracy of the frequency of oscillation given by $f_c = 1/2\pi \sqrt{6CR}$.

12.8.14 Research Project 1: Sinusoidal Oscillator Using the Twin-T Network

The twin-T oscillator shown in Fig. 12.55 utilizes a twin-T network comprising parallel networks $R_1 - R_2 - C_3$ and $C_1 - C_2 - R_3$. Under the
conditions $R_1 = R_2 = 2R_3 = R$ and $C_1 = C_2 = C_3/2 = C$, straightforward circuit analysis yields the transfer function for this network given by

$$\frac{V_o}{V_i} = \frac{1+(sCR)^2}{1+4sCR+(sCR)^2}.$$  

By setting $s = j\omega$, this can be written as

$$\frac{V_o}{V_i}(j\omega) = \frac{1-(\omega CR)^2}{1-(\omega CR)^2+4j\omega CR}.$$  

At $\omega = \omega_o$ where $\omega_o = 1/RC$, i.e., $f_o = 1/2\pi RC$, the magnitude of this transfer function is given by

$$\left|\frac{V_o}{V_i}(j\omega)\right|_{\omega=\omega_o} = \frac{1-1}{\sqrt{(1-1)^2+4^2}} = 0.$$  

Thus, at $\omega = 1/RC$ corresponding to $f = 1/2\pi RC$, the signal transmission through the network is zero. Therefore, at this single frequency, there is no negative feedback around the op-amp, and the positive feedback around the system produces oscillation at this frequency. At all other frequencies, the network produces an output such that negative feedback signal is applied to the amplifier. Thus, the condition $A\beta \geq 1$ around the positive feedback loop is operational at $f_o = 1/2\pi RC$ where $A$ is the amplifier gain at $f_o$ and $\beta = R_A/(R_B + R_A)$. Using $R = 2$ k and $C = 0.01 \mu F$, the oscillating frequency is given by

$$f_o = 1/2\pi RC = 1/2\pi \times 2000 \times 0.01 \times 10^{-6} = 8 \text{ kHz.}$$  

For sustained oscillation, $R_A = 1 \text{ k}$ and $R_B = 10 \text{ k}$ giving $\beta = 1 \text{ k}/((1 \text{ k} + 10 \text{ k}) = 0.09$. This value may have to be adjusted, but increasing values of $\beta$ will generally result in increased distortion of the signal.
Ideas for Exploration: (i) Investigate amplitude stabilization techniques for this circuit; (ii) When there is a slight imbalance in the network resulting from $R_3$ being slightly less than $R/2$, there is a small but nonzero output from the network with phase inverted relative to the input signal. In these circumstances, it is possible to sustain a sinusoidal output from the amplifier without any positive feedback. This occurs since the finite and inverted output signal from the network into the inverting terminal of the amplifier results in zero phase shift around the system and with amplification satisfies $A\beta \geq 1$. Use the circuit shown in Fig. 12.56 where there is no positive feedback with adjustable $R_3$ in order to produce oscillation.
12.8.15 Research Project 2: Sinusoidal Oscillator Using an Inverter

The oscillator shown in Fig. 12.57 satisfies the Barkhausen criterion by using a NAND gate connected as an inverter producing 180° phase shift along with amplification. The output of the NAND gate drives a phase-lag network that produces the additional 180° phase shift. The result is continuous oscillation. The square wave out of the inverter is filtered by the three-stage RC phase-shift network thereby removing harmonics and producing a sine-wave output. The frequency of the sine wave is

\[ f = \frac{\sqrt{6}}{2\pi RC}, \]

and the amplitude of this signal is given by

\[ V_{\text{sin}} = 4V_{\text{sq}}/29\pi \]

which for 5 V logic gate is

\[ V_{\text{sin}} = 4 \times 5 \text{ V}/29 \times \pi = 220 \text{ mV}. \]
Ideas for Exploration: (i) Replace the gate by a single transistor common emitter amplifier circuit and examine the operation; (ii) reduce the gain of the circuit to close to 29 by introducing local feedback such that the output at the collector becomes a low-distortion sine wave (phase-shift oscillator).

12.8.16 Research Project 3: Crystal Oscillator Using Emitter Follower

The requirement is to investigate the crystal oscillator circuit in Fig. 12.58. It is a Colpitts oscillator implemented in an emitter follower that employs a parallel-resonant crystal in place of an inductor. The idea is that at the oscillating frequency, the circuit gives zero phase shift and the tuned circuit with the crystal provides the necessary signal gain to ensure oscillation. $R_1 = 470$ k and $R_2 = 4.7$ k will adequately bias the transistor which can be a 2N3904.
Fig. 12.58  Crystal oscillator using emitter follower

Ideas for Exploration: (i) Try a range of crystals to test the functionality of this circuit; (ii) use this circuit to design a crystal tester as shown in Fig. 12.59. Capacitors $C_3 = 1 \text{nF}$ and $C_4 = 0.0047 \text{\mu F}$ along with diodes $D_1$ and $D_2$ form a voltage multiplier. If the crystal is in good condition, the multiplied output drives transistor $Tr_2$ on and the LED lights. The diodes should be germanium or Schottky diodes since these have low turn-on voltages.
12.8.17 Research Project 4-Modified Twin-T Oscillator

In this project, an oscillator must be designed using the network shown in Fig. 12.60, with $m = n = 1$. 

![Modified twin-T network](image)
This network was previously shown to have a transfer function given in Eq. (12.105) by:

\[
\frac{V_o(s)}{V_i(s)} = \frac{nsCR(m+n+1)}{n(sCR)^2 + sCR(mn+n^2+m+1)+n}
\]

Settings = \(j\omega\), then at a frequency \(\omega_o = 1/RC\) corresponding to \(f_o = 1/2\pi RC\) and with \(m = n = 1\), the transfer function becomes

\[
\frac{V_o}{V_i}(f_o) = \frac{n(1+m+n)}{1+m+mn+n^2} = \frac{1+1+1}{1+1+1+1} = \frac{3}{4}
\]

This indicates that the phase shift introduced by the network is zero at \(f_o\). A suitable oscillator circuit utilizing this network is shown in Fig. 12.61. Using the Barhausen criterion for oscillation, the loop gain at \(f_o\) is given by \(A\beta = A \cdot \frac{3}{4} = 1\). From this, it follows that \(A = 4/3\). For the circuit, \(A = 1 + R_2/R_1\). Therefore, \(1 + R_2/R_1 = 4/3\) giving \(R_1 = 3R_2\). A potentiometer of suitable value can be included in series with either \(R_1\) or \(R_2\) in order to set the loop gain for minimum distortion while sustaining oscillation.

![Modified twin-T oscillator](image)

*Fig. 12.61*  Modified twin-T oscillator
Ideas for Exploration: (i) Implement the circuit for different values of $m$ and $n$, determining the frequency of oscillation and the required amplifier gain.

Problems

1. State the Barkhausen criterion and discuss its meaning with respect to producing oscillation in a system.

2. For the network shown in Fig. 12.62, determine the frequency at which phase shift through the network is zero and the magnitude of the associated transfer function at that frequency. Using this network, design an oscillator to oscillate at a frequency of 15 kHz.

3. Design a Wien bridge oscillator to oscillate at 10 kHz, and explain how a low-power incandescent lamp can be used to achieve amplitude stabilization.

4. For the circuit shown in Fig. 12.63, find the frequency at which the output signal $V_o$ is in phase with the input signal $V_i$ and the transfer function value at this frequency. Hence, design an oscillator using this circuit to have an oscillating frequency of 7 kHz.

Fig. 12.62 Circuit for Question 1
5. Draw the circuit of a phase shift lead oscillator, and describe its operation, referring to the Barkhausen criterion.

6. Design a phase shift lead oscillator to oscillate at 5 kHz, and explain why this circuit is not suitable for a variable frequency oscillator.

7. For the circuit shown in Fig. 12.64, determine showing all analysis the ratio \( R_B/R_A \) in order to achieve oscillation and the frequency of the oscillation. Hence, design an oscillator using this circuit to have an oscillating frequency of 15 kHz.
8. For the circuit shown in Fig. 12.65, determine the inverting amplifier low-frequency gain in order to produce oscillation and the frequency of that oscillation. Hence, design an oscillator using this circuit to have an oscillating frequency of 9 kHz.

![Circuit for Question 8](image)

Fig. 12.65 Circuit for Question 8

9. Draw the circuit of the Meacham oscillator, and briefly explain its operation. Using an operational amplifier, design a Meacham oscillator having an oscillating frequency of 6 kHz, and explain how oscillation can be maintained.

10. Draw the circuit of a crystal oscillator using an operational amplifier as the active element. If the crystal is replaced by an inductor and capacitor in parallel, determine the condition for oscillation and the oscillating frequency of the circuit.

11. For the circuit shown in Fig. 12.66, determine the ratio $R_B/R_A$ for oscillation and the frequency of that oscillation. Using this circuit, design an oscillator with an oscillating frequency of 18 kHz.
12. For the circuit shown in Fig. 12.67, determine the ratio \( R_2/R_1 \) in order to produce oscillation and the frequency of that oscillation. Hence, design an oscillator using this circuit to oscillate at a frequency of 15 kHz.
13. Design an LC resonant oscillator to operate at 50 kHz. Use a 2 N3819 JFET and a 20-V supply.

14. Design an LC resonant oscillator using the AD844 to operate at 15 kHz.

15. Explain the operation of the Hartley oscillator. Design a Hartley oscillator to operate at 50 kHz using a 2 N3819 JFET. Use a supply voltage of 24 V.

16. Explain the operation of the Colpitts oscillator. Design a Colpitts oscillator to oscillate at 50 kHz using a 2 N3819 JFET. Use a supply voltage of 24 V.

17. Determine the required capacitor, $C_T$, to adjust the frequency of the Colpitts oscillators in Question 16 to 55 kHz.

18. Using the circuit in Fig. 12.24, design a simple LC oscillator to oscillate at a frequency of 5 kHz.

19. Design a crystal oscillator to oscillate at 75 kHz using an OP42 operational amplifier.

20. Design a Miller oscillator using a 2 N3918 JFET to oscillate at 110 kHz. Use a 25-volt supply.

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**Bibliography**


U. Tietze, C. Schenk, *Advanced Electronic Circuits* (Springer-Verlag, Berlin, 1978) [Crossref]
In this chapter, we consider circuits that involve the nonlinear operation of the operational amplifier. These can be used to realize waveform generators which are circuits that produce a variety of nonsinusoidal waveforms. They are fundamentally instrumentation building blocks used for signal generation and test and measurement. Typically, waveform generators produce square waves, triangular waves, pulses, and in some cases arbitrary waveforms over a range of frequencies with constant amplitude. Here, we discuss comparators, op-amp-based free-running (astable), and one-shot (monostable) multivibrator circuits as well as precision rectifiers and other nonlinear circuits. At the end of the chapter, the student will be able to:

- Explain the operation of several nonlinear circuits
- Explain the operation of a wide range of waveform generators
- Design a wide range of nonlinear circuits and waveform generators

13.1 The Comparator
A comparator is very similar to an op-amp except that the differential gain is made larger with the addition of internal positive feedback circuitry. As a result, the output has two states $V_{omx}$ and $V_{omn}$ whose values typically approach the comparator supply rails $V_{CC}$ and $-V_{SS}$, respectively. The symbol for a comparator is also identical to an op-amp. In fact, because of its high open-loop gain, an op-amp can operate as a comparator by omitting feedback. To understand the operation of a comparator, consider the circuit shown in Fig. 13.1.

![Fig. 13.1 A comparator with input $V_i$ and reference voltage $V_R$](image)

Here, $V_i$, the input voltage, is applied at the inverting input, while the reference voltage $V_R$ is applied at the noninverting input of the comparator. If $V_i < V_R$, then the differential voltage $V_D = V_i - V_R$ is negative, and hence the output of the comparator is positive, i.e., $V_o = V_{omx}$, and if $V_i > V_R$, then $V_D = V_i - V_R$ is positive and the output of the comparator is negative, i.e., $V_o = V_{omn}$. This comparator would be operating in the inverting mode. If the input terminals are reversed such that $V_i$ is applied at the noninverting input while the reference voltage $V_R$ is applied at the inverting input of the comparator, then if $V_i < V_R$, then the differential voltage $V_D = V_i - V_R$ is negative, and hence the output of the comparator is negative, i.e., $V_o = V_{omn}$, and if $V_i > V_R$, then $V_D = V_i - V_R$ is positive and the output of the comparator is positive, i.e., $V_o = V_{omx}$. This comparator would be operating in the noninverting mode.

If $V_R = 0$, then the comparator is referred to as an inverting or noninverting zero-crossing detector. This action for $V_R = 0$ for a triangular wave input is shown in Fig. 13.2 for a noninverting comparator and in Fig. 13.3 for an inverting comparator.
Example 13.1  An op-amp is connected as a comparator with the inverting terminal held at 1 V. Describe the action of the circuit when the noninverting input is below and above 1 V.

Solution  With the inverting input at 1 V, when the noninverting input is less than 1 V, then the high amplification causes the output to saturate negatively giving \( V_o = -V_{sat} \). When the voltage at the noninverting input is greater than 1 V, the high amplification causes the output to saturate positively giving \( V_o = +V_{sat} \).

Example 13.2  An op-amp is connected as a comparator with the noninverting terminal held at 1 V. Describe the action of the circuit when the inverting input is below and above 1 V.
**Solution**  With the noninverting input at 1 V, when the inverting input is less than 1 V, then the high amplification causes the output to saturate positively giving $V_o = +V_{sat}$. When the voltage at the inverting input is greater than 1 V, the high amplification causes the output to saturate negatively giving $V_o = -V_{sat}$.

One straightforward but useful application of the comparator is in an over-temperature alarm system. The basic system is shown in Fig. 13.4. Here, an LM35 temperature sensor produces an output voltage that is proportional to the ambient temperature given by $V_o = 10T \text{ mV}$ where $T$ is Celsius temperature. This output is connected to the noninverting input of an op-amp. The inverting input is supplied with a reference voltage via a potential divider which sets the reference threshold. The op-amp can be powered by a single-ended power supply since both inputs will have voltages at values between the ground and the supply voltage. Under normal temperature conditions, the output voltage of the temperature transducer falls below the reference voltage, and the op-amp output is, therefore, saturated at close to zero. When the temperature rises above some specific value, the output of the sensor exceeds the reference voltage, and the op-amp output saturates at close to the supply voltage. This output is used to switch on an indicator using a relay.
Example 13.3 Using the basic circuit shown in Fig. 13.4, design a system to turn on a fan when the ambient temperature in a room exceeds 35 °C.

Solution Here, an op-amp is connected as a comparator. The output of the LM35 temperature sensor drives the noninverting input of the op-amp, while the inverting terminal is connected to the output of a potential divider arrangement comprising $R_1 = 10 \, k\Omega$ and $VR_1 = 2 \, k\Omega$. With a 12 V supply, this means that the wiper of the potentiometer can be varied from 0 to 2 V. For a threshold temperature of 35 °C, the potentiometer is set to $10 \, mV \times 35 = 350 \, mV$. When the temperature is below 35 °C, the output of the sensor will be less than 350 mV, and therefore, the output of the op-amp will be low. Therefore, the green LED will be on with current limited by $R_2 = 1 \, k\Omega$ to about 10 mA, and the red LED will be off. The base of the transistor will also be at a low voltage, and therefore, the transistor will be off. When the temperature is above 35 °C, the output of the op-amp will be high. Therefore, the red LED will be on with current limited by $R_3 = 1 \, k\Omega$ to about 10 mA, and the green LED will be off. The high op-amp output will turn on the...
transistor, thereby causing the relay to switch on power to the fan. Resistor $R_4 = 10\,\text{k}$ ensures transistor saturation.

If noise is present on the input signal, this can lead to spurious or false switching of the comparator. In order to overcome this and other potential problems, the comparator's performance can be enhanced if positive feedback is added in the form of resistors $R_a$ and $R_b$ as shown in Fig. 13.5.

![Fig. 13.5 A comparator with positive feedback](image)

For this circuit, the output voltage $V_o$ in terms of the input $V_i$ can be determined by writing the equation

$$V_o = A_d \left( \frac{R_a}{R_a + R_b} V_o - V_i \right)$$

where $A_d$ is the differential gain of the comparator. Solving for $V_o$ gives

$$V_o = \frac{A_d}{A_d \beta - 1} V_i$$

where $\beta$, a constant, is defined as $\beta = \frac{R_a}{R_a + R_b}$. Since $\beta$ is always less than one, it follows that the denominator of (13.2) could be less than one or greater than one. For the case $0 \leq A_d \beta \leq 1$, the gain of the comparator is negative and larger than $A_d$ which corresponds to the case of the simple
comparator in Fig. 13.1. When $A_d\beta = 0$ which corresponds to setting $R_a = 0$ or $R_b \to \infty$, $V_R = 0$ and the comparator has the transfer characteristic shown in Fig. 13.6. For values of $0 \leq A_d\beta \leq 1$, the slope of the transfer characteristic is $-\frac{A_d}{1-\beta A_d} > -A_d$.

![Fig. 13.6 Transfer characteristic of the comparator when $\beta = 0$](image)

For $A_d\beta > 1$, the situation changes as the slope of the transfer characteristic becomes positive and less than $A_d$. Under this condition, the comparator is referred to as a Schmitt trigger with a transfer characteristic shown in Fig. 13.7. From Fig. 13.7, the transfer characteristic has a unique shape in that for $V_i > V_{imx}$ the output voltage is $V_o = V_{omn}$. However, if $V_i$ starts off being greater than $V_{imx}$ and is decreased to $V_{imx}$ and less, the output remains at $V_{omn}$ until $V_i < V_{imn}$ is reached. When this occurs, $V_o = V_{omx}$. The converse is true, i.e., if we start with $V_i$ being less than $V_{imn}$ and increasing to $V_i$ and greater, the output will eventually switch from $V_{omx}$ to $V_{omn}$. Thus, the Schmitt trigger has two distinct switching points, $V_{imx}$ and $V_{imn}$ given by...
Fig. 13.7 Transfer characteristic of the Schmitt trigger

\[ V_{imx} = \frac{A_d \beta - 1}{A_d} V_{omx} \]  \hspace{1cm} (13.3)

and

\[ V_{inn} = \frac{A_d \beta - 1}{A_d} V_{omn} \]  \hspace{1cm} (13.4)

Note that if a voltage \( V_R \) is applied to the grounded end of resistor \( R_a \) by removing it from the ground, the transfer characteristic of Fig. 13.7 shifts to the right by an amount \( V_R \) if \( V_R > 0 \) and to the left by an equal amount if \( V_R < 0 \). The new switching points can be found by adding \( V_R \) to Eqs. (13.3) and (13.4). Finally, an op-amp can function as a comparator or a Schmitt trigger. However, its switching times between output states will typically not be as good as a dedicated comparator.
Example 13.4  Design a Schmitt trigger circuit with a switching threshold of ±5 V using the LF411 op-amp powered by ±15 V supplies. For the op-amp, assume $|V_{omx}| = |V_{omn}| = 14.2$ V and $A_d = 200,000$. Verify your result using PSPICE with an input signal $V_i = 10 \sin(2\pi 10^3 t) V$.

Solution  To find $\beta$, we use Eq. (13.3) with $V_{imx} = 5$ V. Solving yields $\beta = 0.352$. Choosing $R_a = 1$ k yields $R_b = 1.84$ k. The PSPICE simulation result is shown in Fig. 13.8 verifying that the circuit triggers at ±5 V.

![PSPICE simulation](image)

**Fig. 13.8**  PSPICE simulation

### 13.2 Square-Wave Generation

A simple square-wave generator is shown in Fig. 13.9. It consists of a single amplifier $A_1$ which may be an op-amp or a comparator configured as a Schmitt trigger. Because of the positive feedback, upon switch on the output of the op-amp saturates to either the positive rail $+V_{sat}$ or the negative rail $-V_{sat}$. Assuming that on applying power, the system goes to the positive rail $V_o = +V_{sat}$ then the voltage at the inverting input terminal is, therefore, $+\beta V_o$ where the resistive feedback factor $\beta$ is given by $\beta = \frac{R_a}{R_a + R_b}$. This voltage acts as a threshold voltage. If
the capacitor $C_1$ is initially uncharged, then it begins to charge from zero volts with its voltage $V_c$ increasing toward $+V_{sat}$ with a time constant $\tau = R_1C_1$. Eventually, $V_c$ at the inverting terminal reaches and slightly exceeds the threshold voltage $+\beta V_o$ set at the noninverting terminal and the output of $A_1$ switches to the negative saturation voltage $-V_{sat}$. The capacitor $C_1$ will now begin to charge toward the negative rail, and once again the output will switch to the positive rail when the new threshold $-\beta V_o$ is exceeded. The process is then repeated indefinitely as shown in Fig. 13.9b.

![Fig. 13.9](image1)

In practice, the value of $V_{sat}$ is imprecise and, therefore, leads to inaccuracy in the calculation of the waveform characteristics which depend on its value. In order to improve the accuracy, the output $V_o$ of $A_1$ is clamped by two back-to-back Zener diodes so that instead of $V_o$ being $V_o = \pm V_{sat}$ we have $V_o = \pm(V_Z + V_D)$ where $V_Z$ is the Zener voltage and $V_D = 0.7$ V. Resistor $R$ limits the current through the Zener diodes. To determine the period of oscillation, we may arbitrarily assign $t = 0$ as the starting point at which the capacitor voltage is $-\beta V_o$. The time domain response of the capacitor voltage from basic circuit theory is then given by

$$V_{c_1}(t) = -\beta V_o + (1 + \beta) V_o \left[1 - e^{-\frac{t}{\tau}}\right]$$  (13.5)
for $0 \leq t \leq T/2$. At $t = T/2$, the half-cycle is completed as $V_{c_1}(T/2)$ = $+\beta V_o$ is reached. Substituting in (13.5) yields

$$+\beta V_o = -\beta V_o + (1 + \beta) V_o \left[ 1 - e^{-\frac{t}{\tau}} \right]$$

(13.6)

and solving for the period $T$ gives the result

$$T = \frac{1}{f_{osc}} = 2\tau \ln \left( \frac{1 + \beta}{1 - \beta} \right) = 2\tau \ln \left[ 1 + 2 \left( \frac{R_a}{R_b} \right) \right]$$

(13.7)

Note that the period $T$ is independent of the supply voltage and the output voltage $V_o$ and is comprised of two equal periods $T_1$ and $T_2$. If an unsymmetrical waveform is desired, the network of Fig. 13.10 can be used in place of $R_1$. It consists of two resistors of unequal value. The diodes ensure that only one resistor is enabled in the circuit during a given cycle. Hence during the positive half-cycle as $V_c(t)$ increases, $D_2$ is on while $D_1$ is off. For this half-cycle, the time constant $\tau_1 = R_1aC_1$. Conversely for the negative half-cycle $D_1$ is on while $D_2$ is off, and the time constant is now $\tau_2 = R_1bC_1$. The expression for the periods $T_1$ and $T_2$ are, therefore, given by

$$T_1 = \tau_1 \ln \left( \frac{1 + \beta}{1 - \beta} \right) = \tau_1 \ln \left[ 1 + 2 \left( \frac{R_a}{R_b} \right) \right]$$

(13.8)

$$T_1 = \tau_1 \ln \left( \frac{1 + \beta}{1 - \beta} \right) = \tau_1 \ln \left[ 1 + 2 \left( \frac{R_a}{R_b} \right) \right]$$

(13.9)

![Fig. 13.10](image-url) A method to obtain an unsymmetrical square wave using diodes
The only disadvantage to using the diodes in this manner is that the output voltage is reduced by one diode drop. As a general rule of thumb, the square-wave generator is useful to frequencies of about one tenth of the Gain Bandwidth Product (GBP) of the amplifier used. As the frequency is increased beyond that slew rate effects and the capacitance seen at the output of $A_1$ due to Zener diodes alters the output rise and fall times. The effect of slew rate limitations can be minimized by using a comparator for $A_1$ in place of an op-amp. Since the comparator is designed for high gain and not in a feedback configuration, its slew rates can be very high. Also, as a general rule of thumb, if the output of the square-wave generator is required to have a particular rise time $t_r$, then it is related to the amplifiers slew rate by

$$t_r = 0.8 \times \frac{2V_o}{SR}$$

(13.10)

Here, rise time is defined as the time it takes the output to get from 10% to 90% of the asymptote. To minimize the capacitance, two back-to-back diode-connected transistors can be employed in place of the Zener diodes. The effective Zener voltage is then set by the emitter-base breakdown voltage of the transistors used, and the nodal capacitance is considerably less than that of commercial Zener diodes.

An alternative method of generating unsymmetrical square waves is to remove the lower end of resistor $R_a$ from the ground and apply a voltage $V_R$ to the lower end of resistor $R_a$. For this configuration, show that the new periods $T_1$ and $T_2$ are given by

$$T_1 = \tau \ln\left[\frac{(1 + \beta) - \alpha (1 - \beta)}{(1 - \beta) - \alpha (1 - \beta)}\right]$$

(13.11)

and

$$T_1 = \tau \ln\left[\frac{(1 + \beta) - \alpha (1 - \beta)}{(1 - \beta) - \alpha (1 - \beta)}\right]$$

(13.12)

where $\alpha = V_R/V_o$ is a constant whose magnitude is less than one but greater than zero. Note that for $\alpha = 0$, the equation above reverts to Eq.
(13.7) and for $0 < \alpha < 1$, $T_1 > T_2$ and for $-1 < \alpha < 0$, $T_2 > T_1$.

**Example 13.5** Design a square-wave oscillator to have an oscillation frequency of 100 kHz, with an output of ±5 V using a ±12 V bipolar supply.

**Solution** To clamp the outputs to ±5 V, we begin by choosing appropriate Zener diodes. Let us choose the 1N437A Zener diode which has a $V_Z = 4.3$ V. The reason for choosing this value is due to the fact that $V_o = V_Z + V_D$. With $V_D = 0.7$ V the solution to this equation yields $V_Z = 4.3$ V. To satisfy the frequency of oscillation, let us choose $R_a = 10$ k and $R_b = 39$ k yielding $\beta = 10/39$. If we let $C_1 = 1200$ pF, then from (13.7) $R_1 = 10$ k. For the amplifier, we may choose an op-amp or a dedicated comparator. We choose the LM111 comparator for its reasonable response time of 200 ns and its operation over a wide voltage range. The final circuit is shown in Fig. 13.11. Note the presence of the 4 kΩ resistor which is there because the LM111 has an open collector output. A PSPICE simulation of the output waveform is shown in Fig. 13.12.

![Circuit for Example 13.5](imageURL)

*Fig. 13.11* Circuit for Example 13.5
Example 13.6  Modify the previous design so that the circuit now operates from a single 12 V supply and generates a 5 V Transistor Transistor Logic (TTL) output at the same frequency.

Solution  To accomplish this, we recognized that the original circuit oscillates about zero volts. Therefore, for single-supply operation, the new circuit must oscillate about a new virtual ground which in this case must be $V_0/2$ or 2.5 V. The lower plate of $C_1$ must therefore, be supplied with 2.5 V by the buffer. At this point, the designer has several options open to them. If the 2.5 V source is readily available, the design is complete. If not, then one must improvise. One simple method is to use a potential divider comprising of the 1 k and the 3.8 k resistor to generate the desired voltage that is then buffered. Such a solution is shown in Fig. 13.13. If the number of components is an important factor, the circuit of Fig. 13.13 will also work if the op-amp is removed and the potential divider directly connected to the 1200 pF capacitor and the 10 k resistor, but virtual “2.5 V” will oscillate. Low resistor values will reduce the oscillation, but they increase the power consumption of the circuit. If the buffer is employed, the resistor values can be increased to reduce the power consumption. The PSPICE simulation of the output waveform is shown in Fig. 13.14.
13.2.1 Sine Wave Generation from a Square-Wave Input
Low distortion sine waves can be easily generated from a square-wave input by using a simple bandpass filter to extract the fundamental frequency. To understand why we recall from the Fourier series that a square wave is made up of the sum of sinusoidal waves. That is, the output voltage $V_o(t)$ of Fig. 13.9 can be described by

$$V_o(t) = \frac{4A}{\pi} \left( \sin \omega_0 t + \frac{1}{3} \sin 3\omega_0 t + \frac{1}{5} \sin 5\omega_0 t + \frac{1}{7} \sin 7\omega_0 t + \cdots \right)$$ \hspace{1cm} (13.13)

where $A$ is the peak amplitude of the square wave. Examining the Eq. (13.13) closely shows us that the third harmonic has an attenuation $\alpha_{v_o}(3\omega_0) = 9.54$ dB greater than the fundamental. We only need to consider the third harmonic since the fifth and seventh harmonics, etc. have greater attenuation. For a unity gain, second-order bandpass filter tuned to $\omega_0$, the attenuation for a given $Q$ to the third harmonic is

$$\alpha_{BP}(3\omega_0) = -20 \log_{10} \left( \frac{3}{\sqrt{9 + 64Q^2}} \right)$$ \hspace{1cm} (13.14)

If $V_o(t)$ is now passed through the bandpass filter, the total attenuation of the third harmonic is now

$$\alpha_T(3\omega_0) = \alpha_{v_o}(3\omega_0) + \alpha_{BP}(3\omega_0)$$.

Table 13.1 shows the attenuation for the third harmonic as a function of $Q$.

<table>
<thead>
<tr>
<th>$Q$</th>
<th>$\alpha_{BP}(3\omega_0)$</th>
<th>$\alpha_{v_o}(3\omega_0)$</th>
<th>$\alpha_T(3\omega_0)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>28.25</td>
<td>9.54</td>
<td>38.07</td>
</tr>
<tr>
<td>15</td>
<td>32.04</td>
<td>9.54</td>
<td>41.60</td>
</tr>
<tr>
<td>20</td>
<td>34.54</td>
<td>9.54</td>
<td>44.08</td>
</tr>
</tbody>
</table>

Hence it can be seen that only a $Q$ of about 10 is sufficient to achieve almost 40 dB of attenuation for the third harmonic. Thus, a state variable filter could be used to generate a low distortion sine wave. Finally, note that the resulting sine wave will have an amplitude that is
$4/\pi$ times that of the input signal. An example of the filtering action of the second-order bandpass filter is shown as the MATLAB simulation in Fig. 13.15 where a square wave of input frequency 1 kHz and 1 V peak-to-peak is the input and the output is a sine wave of amplitude 1.27 V.

![Figure 13.15 MATLAB simulation](image)

### 13.3 Triangular Wave Generation

In the previous section, we noted that the capacitor voltage was exponential with a time constant. To generate a triangular waveform that has a constant slope, the current charging or discharging of the capacitor must be constant so that the voltage developed across the capacitor is the integral of a constant. Hence a current source whose current is a function of the output will generate a triangular output waveform. An example of this is shown in Fig. 13.16. Here, transistors $Q_1$ and $Q_2$ which could be bipolar or CMOS act as current sources and current sinks. The operation of this circuit is, therefore, conceptually similar to that of Fig. 13.9. That is, during the positive upswing diode, $D_2$ is forward-biased ($D_1$ is reversed-biased) so that transistor $Q_2$ is effectively off. Transistor $Q_1$, therefore, acts as a current source charging $C_1$ with a constant current $R_{CL} = \left(\frac{75}{I_{LM}} - 7.5\right)$ kΩ. When the capacitor voltage $V_c(t)$ reaches the threshold voltage $+\beta V_o$, the output of
A_1 \text{ goes negative and } D_1 \text{ becomes forward-biased with } D_2 \text{ now reversed-biased. Transistor } Q_1, \text{ therefore, switches off and } Q_2 \text{ switches on acting as a current sink connected to } C_1 \text{ with a constant current }
\begin{align*}
R_{CL} &= \left( \frac{75}{I_{LM}} - 7.5 \right) \text{k}\Omega.
\end{align*}
Eventually, the capacitor voltage \( V_c(t) \) reaches the threshold voltage \(-\beta V_o\) and the output of the amplifier \( A_1 \) goes positive and the cycle repeats as shown in Fig. 13.17. The role of diodes \( D_1 \) and \( D_2 \) is, therefore, to steer the current source or sink depending on the output state. Resistor \( R \) serves to limit the current through Zener diodes \( Z_1 \) and \( Z_2 \). To compute the period of oscillation, we need to evaluate each half-cycle period. Assigning \( t = 0 \) as the starting point at which the capacitor voltage is \(-\beta V_o\), the voltage across the capacitor \( V_c(t) \) is given by
\begin{equation}
V_c(t) = \frac{1}{C} \int_0^t I_{C1} dt
\end{equation}
for \( 0 \leq t \leq T_1 \). At \( t = T_1 \) the half-cycle is completed as \( V_{c1} (T_1) = +\beta V_o \) is reached. But from (13.15)
\begin{equation}
V_c(T_1) = \frac{T_1}{C} \left( \frac{V_{Z3} - V_{BE1}}{R_1} \right) - \beta V_o
\end{equation}
Fig. 13.16 Triangular Waveform Generator

Fig. 13.17 Output waveform of Fig. 13.16
Solving for $T_1$ yields

$$T_1 = 2C\beta V_o \left( \frac{R_1}{V_{Z3}-V_{BE1}} \right).$$

In a similar manner half-cycle period $T_2$ can be solved as

$$T_1 = 2C\beta V_o \left( \frac{R_1}{V_{Z3}-V_{BE1}} \right).$$

The total period $T = T_1 + T_2$ and hence the frequency of oscillation is, therefore, given by

$$T = \frac{1}{f_{osc}} = 2C\beta V_o \left( \frac{R_1}{V_{Z3}-V_{BE1}} + \frac{R_2}{V_{Z4}-V_{BE2}} \right)$$

(13.17)

If $V_2 = BV_1$, $V_{BE1} \approx V_{BE2}$ and $R_1 = R_2$, then

$$f_{osc} = \frac{V_{Z3}-V_{BE}}{4C\beta V_o R_1}$$

(13.18)

If $T_1 \neq T_2$ either by setting $R_1 \neq R_2$ or $V_2 = BV_1$, a sawtooth waveform can be generated. Note that buffering at the capacitor node is required to drive any load so as not to disturb the nodal currents as illustrated by the dashed op-amp.

**Example 13.7**  Design a square-wave/sawtooth oscillator that oscillates at a frequency of 3.2 kHz.

**Solution**  We begin, by choosing a typical op-amp, the TL082 which has a bandwidth of 1.4 MHz. Next we choose $V_{Z3} = V_{Z4} = 4.7$ V using the 1N750 Zener diodes and $R_1 = R_2 = 1$ k. Since the average Zener diode current is about 20 mA, we can choose $R_3 = 2$ k, which limits the Zener diode current to approximately 10 mA. Diodes $D_1$ and $D_2$ can be regular 1N4148 diodes, and we can set $R_4$ and $R_5$ to both be 1 k. Next, we choose $C_1 = 0.22$ μF, and with $V_o \approx 13.4$ V, it follows that

$$\beta = \frac{V_{Z3}-V_{BE}}{4CV_o R_1 f_{osc}}$$

or $\beta \approx 0.1$. Since $\beta = \frac{R_a}{R_a+R_b}$, let us choose $R_a = 1$ k which results in $R_b = 9$ k. To observe the triangular waveform, we add a simple buffer to
the capacitor voltage to allow it to drive an output. The value of that output is $\beta V_o$ or 1.38 V.

A circuit that is capable of driving low impedance loads and simultaneously generating triangular or square waves is shown in Fig. 13.18. Here amplifier $A_2$, a dedicated op-amp functions as a lossless integrator to replace the Zener diode/transistor arrangement of Fig. 13.16. Conceptually Figs. 13.16 and 13.18 are the same as op-amp $A_2$ integrates the input voltage $V_{o1}$ to yield a constant slope triangular waveform. $V_R$ and $V_S$ represent control voltages. For the moment, let us assume that $V_S = 0$. Later, we shall see it serves to control the duty cycle of the oscillations. To further understand the operation of this circuit, we need to look at the noninverting node of amplifier $A_1$. By superposition the voltage $V_x$ at this node is given by

$$V_x = -V_{o1}\beta + V_{o2} (1 - \beta) \tag{13.19}$$

where $\beta$ was previously defined as $R_a/(R_a + R_b)$. At a switching point, the voltage $V_x$ must be equal to the reference voltage $V_R$ so that the op-amp output voltage $V_{o2}$ can be computed from (13.19) as

$$V_{o2} = \frac{V_R}{1 - \beta} + V_{o1} \frac{\beta}{1 - \beta} \tag{13.20}$$

![Fig. 13.18](image-url) A variation on the triangular wave generator that uses all op-amps.
However, the output voltage $V_{o1}$ alternates between $\pm V_o$, and therefore, (13.20) can be rewritten as

$$V_{o2} = V_R \frac{R_a + R_b}{R_b} \pm \frac{R_a}{R_b} V_o$$

(13.21)

From (13.21), it can be seen that the integrator output swings between $\pm \frac{R_a}{R_b} V_o$ with an average value of $V_R(R_a + R_b)/R_b$. This point is illustrated in Fig. 13.19. Hence by controlling $V_R$, we can control the offset of the triangular waveform, while the output amplitude can be controlled by varying the ratio $R_a/R_b$. To determine the frequency of operation, we note that $V_{o2} = -\frac{1}{R_1C_1} \int V_{o1} dt$. Using $t = 0$ as the starting point, we note that at $t = T_1$ or at the end of the first half-cycle

$$V_{o2}(T_1) = -\frac{1}{R_1C_1} \int_0^{T_1} V_{o1}(t) dt + V_{o2}(0) = -\frac{1}{R_1C_1} [V_{o1}(T_1) T_1] + V_{o2}(0)$$

(13.22)
But \( V_{o2}(T_1) = -\frac{R_a}{R_b}V_o + V_R\frac{R_a+R_b}{R_b}, \ V_{o1}(0) = \frac{R_a}{R_b}V_o + V_R\frac{R_a+R_b}{R_b}, \) and \( V_{o1}(T_1) = V_o. \) Substituting in (13.22) and solving for \( T_1 \) yields

\[ T_1 = \frac{2R_1C_1R_a}{R_b} \]  

(13.23)

Similar analysis applied to the second period \( T_2 \) will also yield

\[ T_1 = \frac{2R_1C_1R_a}{R_b} \]  

(13.24)
With $T_1 = T_2 = T/2 = 1/2f_{osc}$, the frequency of oscillation is, therefore, given by

$$f_{osc} = \frac{R_b}{4R_1C_1R_a} \quad (13.25)$$

The resulting composite waveforms are shown in Fig. 13.19. Clearly from (13.25), the frequency of oscillation can be controlled by varying $R_1$ (or $C_1$) and is independent of $V_o$. Usually decades of frequency change are obtained by changing $C$ by a factor of 10 and within a decade by varying $R$ continuously. In terms of high frequency limitations, this waveform generator is limited by either the slew rate of the op-amp $A_2$ used or its maximum output current.

**Example 13.8**  Design a sawtooth/square oscillator using the alternative structure of Fig. 13.18 that oscillates at $f_{osc} = 15$ kHz.

**Solution**  Let us begin the design of this oscillator by setting $V_R = V_S = 0$ V and by choosing $C_1 = 0.1$ μF and $R_1 = 1$ k. This implies from (13.25) that $\frac{R_b}{R_a} = 6$. Choosing $R_a = 1$ k yields $R_b = 6$ k. Note that the integrator output swings between $\pm \frac{1}{6}V_o$ and roughly 2.2 V with an average value of zero volts.

**Exercise 13.1**  An alternative method of frequency control in this waveform generator is to use the potentiometer arrangement as shown in Fig. 13.20. If $\alpha V_{o1}(\alpha \leq 1)$ represents the portion of the output signal $V_{o1}$ that supplies the integrator, show that the frequency of oscillation of this circuit is given by

$$f_{osc} = \frac{\alpha R_b}{4C_1R_a [R_1 + \alpha (1 - \alpha) R_C]} \approx \frac{\alpha R_b}{4R_1C_1R_a} \quad (13.26)$$

if $R_1 \gg R_C$ where $R_C$ is the total potentiometer resistance.
**13.3.1 Duty Cycle Modulation**

In the previous section, a 50% duty cycle square-wave/triangular wave generator was introduced. Here, we define duty cycle $\delta$ as the ratio $T_1/T \times 100\%$. To be able to vary the duty cycle of the circuit of Fig. 13.18, we must set $V_S \neq 0$. To see why we first note that with $V_S \neq 0$, $V_{o2} = \frac{1}{R_1C_1} \int (V_S - V_{o1}) \, dt + V_S \delta (-\infty)$. That is, the slope of the integrator is now $(V_S \pm V_o)/R_1C_1$ depending on the value of the output $V_{o1}(\pm V_o)$ in the cycle. The impulse function is present in the above equation only for mathematical completeness and disappears after power-up. Assigning $t = 0$ once again as an arbitrary starting point and following the logic used earlier in deriving (13.22)–(13.24), the periods $T_1$ and $T_2$ are now given by

$$T_1 = \frac{2R_1C_1R_a}{R_b} \frac{V_o}{(V_S - V_o)} \quad (13.27)$$

$$T_2 = \frac{2R_1C_1R_a}{R_b} \frac{V_o}{(V_S - V_o)} \quad (13.28)$$

Therefore, the duty cycle $\delta$ of the square wave or the triangular wave is given by

$$\delta \equiv \frac{T_1}{T} = \frac{T_1}{T_1 + T_2} = \frac{1}{2} \left(1 + \frac{V_S}{V_o}\right) \quad (13.29)$$
Hence the duty cycle varies from 0 when $V_s = -V_o$ to 50% when $V_s = 0$ to 100% when $V_s = +V_o$. In practice, the extremities of the duty cycle are never achieved. Note that the frequency of oscillation can be easily deduced to be

$$f_{osc} = \frac{R_b}{4R_1C_1R_a} \left[ 1 - \left( \frac{V_s}{V_o} \right)^2 \right]$$  \hspace{1cm} (13.30)

which is a nonlinear function of frequency.

**Example 13.9** Determine the frequency of oscillation of Fig. 13.18 if the control voltage changes from $V_s = 0$, 2, 3 V. You may assume that $C_1 = 0.1 \mu F$, $R_1 = 1 \text{ k}$, and $\frac{R_b}{R_a} = 6$.

**Solution** With $V_o \approx 13.4 \text{ V}$, $f_{osc} = \frac{6}{4 \times 1000 \times 0.1 \times 10^{-6}} \left[ 1 - \frac{V_s}{13.4} \right]$. For $V_s = 0 \text{ V}$, $f_{osc} = 15 \text{ kHz}$. For $V_s = 2 \text{ V}$, 

$$f_{osc} = \frac{6}{4 \times 1000 \times 0.1 \times 10^{-6}} \left[ 1 - \frac{2}{13.4} \right] = 14.66 \text{ kHz}.$$  \hspace{1cm} Finally, for $V_s = 3 \text{ V}$,

$$f_{osc} = \frac{6}{4 \times 1000 \times 0.1 \times 10^{-6}} \left[ 1 - \frac{2}{13.4} \right] = 14.66 \text{ kHz}.$$

### 13.3.2 Sawtooth Generation

A natural extension of the triangular wave generator is that of a sawtooth waveform. Sawtooth waveforms are used where a repeatable ramp function whose single positive or negative slope has a predefined period $T$. In fact, the sawtooth waveform can be regarded as a triangular waveform with one slope of the triangular waveform being set at $\pm \infty$. That is either $T_1 = 0$ or $T_2 = 0$. As such, the triangular wave generator of Fig. 13.18 can be used, but its duty cycle must be set to near 0% for a positive-going sawtooth waveform and near 100% for a negative-going sawtooth waveform.

**Example 13.10** Design a triangular wave generator to generate a positive-going sawtooth wave of 5 V pk–pk amplitude with a frequency
of 5 kHz of a 15 V supply.

**Solution**  We first note that for a positive ramp function, $V_s$ must be negative. Since we require the output $V_o = \pm 5$ V, we can employ 1N437 Zener diodes for $D_1$ and $D_2$ as before to clamp the output to the desired value. Furthermore let us choose $V_s = -4.8$ V so that according to (13.29), $\delta = 2\%$ and hence $T_1 \ll T_2$. Employing Eq. (13.30) with $f_{osc} = 5$ kHz, let us choose $R_a = R_b = 10$ k. Hence, we can solve for the time constant $R_1 C_1 = 3.92$ µs. Choosing $C_1 = 1000$ pF yields $R_1 = 3.92$ k. We can use a 3.9 k resistor. The last step involves the choice of amplifiers. If the design application is not critical, then a general purpose op-amps such as the LF411 op-amp can be employed for $A_1$ and $A_2$. The final circuit and PSPICE simulation results are shown in Figs. 13.21 and 13.22. Note that the output of the generator has a negative DC offset. Why?

![Fig. 13.21](image)  Final circuit for Example 13.10
Another means of altering the duty cycle is to employ the circuit of Fig. 13.23 which uses the circuit of Fig. 13.10 to alter the time constants. Here, we choose $R_{1b} \gg R_{1a}$ so that the integrator time constant during the positive cycle is more.

![Fig. 13.22](image)

**Fig. 13.22** PSPICE simulation for Example 13.10

**Fig. 13.23** An alternative sawtooth waveform generator

### 13.3.3 Voltage-Controlled Oscillators

A voltage-controlled oscillator (VCO) is a circuit whose frequency of oscillation can be directly controlled by a voltage. Note in some cases, the controlling signal can be a current. VCOs can be of two types: those
that produce square and/or triangular waveforms and those that produce sinusoidal waveforms. In regards to multivibrators that produce square/triangular waveforms, the circuit of Fig. 13.20 can be considered a VCO since its frequency is dependent on $V_S$ albeit nonlinearly. Sinusoidal VCOs are usually realized using a tuned circuit in a feedback connection or using a sinewave shaper. The tuned circuit could be RC, LC, or crystal based. The sinewave shaper exploits the logarithmic characteristic between $V_{be}$ and the collector current in a bipolar transistor to smooth a triangular wave.

In this section, we describe a simple square/triangular waveform VCO and two sinusoidal VCOs. VCOs that generate square waveforms can be built using ring oscillators, but they will not be discussed here.

### 13.3.3.1 A Square/Triangular Waveform VCO

Consider the circuit of Fig. 13.24 which represents a modification of Fig. 13.18. Two differences are immediately observed. The first is that the amplifier is now configured as a Schmitt trigger by grounding $R_a$. Secondly, a CMOS version of a single pole double throw (SPDT) switch has been introduced between the comparator and the integrator. The effect of the SPDT is to provide the integrator with a sweep speed of $\pm V_o/RC$ depending on the sign of $V_{o1}$. Hence when $V_{o1} = +V_o$, $M_2$ is on while $M_1$ is off, and the integrator receives a voltage of $-V_M$. Conversely, when $V_{o1} = -V_o$, $M_1$ is on while $M_2$ is off, and the input voltage to the integrator is now $+V_M$. The Schmitt trigger functions as before, switching when $V_{o2}$ exceeds the variable threshold $\pm \beta V_o$. The waveforms produced by the circuit of Fig. 13.24 are, therefore, identical to those shown in Fig. 13.17 with identical half cycles. Using Fig. 13.17 as a guide, during the positive sweep,

$$V_{o2}(t) = -\frac{1}{R_1C_1}\int_{0}^{\frac{t}{T}} (-V_M)\, dt - \beta V_o$$

(13.31)
But $V_{o2}\left(\frac{T}{2}\right) = +\beta V_o$ and, therefore, the period can be solved as

$$T = \frac{4\beta V_o R_1 C_1}{V_M}$$

The frequency of oscillation is, therefore,

$$f_{osc} = \frac{R_a + R_b}{4 R_a R_1 C_1} \cdot \frac{V_M}{V_o}$$

From (13.33), it can be seen that the frequency varies linearly with the control voltage $V_M$. It has been reported that several decades of frequency are available with this type of VCO making it useful for frequency modulation.

**Example 13.11** Design an oscillator whose frequency of oscillation is variable from $f_{osc} = 5.3$ kHz to $f_{osc} = 10.63$ kHz. You may assume that $C_1 = 0.1$ μF, $R_1 = R_a = 1$ k and $R_b = 4.7$ k.

**Solution** With $V_o \cong 13.4$ V,

$$f_{osc} = \frac{1}{4 \times 1 \times k \times 1000 \times 0.1 \times 10^{-6}} \cdot \frac{V_M}{13.4} = 1063.43 \cdot \frac{V_M}{V_o}$$

Hence when $f_{osc} = 5.3$ kHz, $V_M = 5$ V and when $f_{osc} = 10.63$ kHz, $V_M = 10$ V.
13.3.3.2 A Sinusoidal VCO

The circuit of Fig. 13.24 can be used to generate sinewaves and hence a sinusoidal VCO if we use its triangular waveform output to drive the sinewave shaper circuit shown in the bottom half of Fig. 13.25. This circuit functions by exploiting the $I_c/V_{BE}$ characteristics of transistors $Q_1$ and $Q_2$ to approximate the sine function over a limited input range. It can be recognized that transistors $Q_1 - Q_4$ form a differential amplifier with the inverting terminal grounded and a significantly reduced input signal applied to $Q_1$. Here, the 47 Ω resistors act as degeneration resistors, and transistors $Q_{3,4}$ form a current mirror that copies the collect current of $Q_1$ and subtracts it from the collector current of $Q_2$. The 100 Ω resistor forces the node labeled $a$ to be low impedance and converts the output current to a voltage that is then amplified by amplifier $A_5$. Two variable resistors are included that offer symmetry adjustment and wave shaping. The value of the wave-shaping resistor is crucial because it determines the distortion levels of the sine wave produced. Note in Fig. 13.25, amplifier $A_4$ generates $-V_M$ for MOS switches $M_1$ and $M_2$. It is equally possible to use JFETs instead of MOS transistors with the addition of some bias circuitry. Figure 13.26 shows the outcome of a PSPICE simulation of the circuit of Fig. 13.25 using LF411 op-amps, $R_1 = 10$ k, $C_1 = 12$ nF and transistors $Q_{1,2}$ and $Q_{3,4}$ as general purpose 2N3904/2N3906 transistors. Input voltage $V_M$ is varied from 1 to 10 V.
Fig. 13.25  A sinusoidal/triangular/square-wave VCO
A direct alternative means to construct a linear sinusoidal VCO requires designing a system whose imaginary axis poles move linearly with a control voltage $V_c$. Most such commercial VCOs are made using transconductors connected in a filter configuration whose poles are controlled via a transconductance amplifiers. To better understand this, suppose the characteristic equation of a system or a bandpass filter was of the form $s^2 + a_1 s + a_0$. Next, we arrange it so that $a_1 = 0$ and then set $a_0 = K V_c^2$, where $K$ is a constant. Setting $a_1 = 0$ ensures that the poles are on the $j\omega$ axis, resulting in a frequency of oscillation $f_{osc} = \frac{1}{2\pi} V_c \sqrt{K}$. A simple circuit that accomplishes this is shown in Fig. 13.27 consisting of an op-amp and two multipliers. Each multiplier is assumed to have a multiplier constant $K_i$, $i = 1, 2$. The two multipliers are needed to generate the term $V_c^2$. If only one multiplier was used, then the frequency of oscillation would vary with the square root of $V_c$. To determine the frequency of oscillation, we must compute the loop gain and set it equal to one. Breaking the loop at the point indicated by the $\times$ the loop gain of this circuit can be computed as
If $R_1 = R$ then the characteristic equation is given by

$$LG = \frac{K_1 K_2 V_c^2}{C_1 C_2 R_1 R_2 s^2 + (C_1 R_1 R - C_2 R^2) s + R_1 - R} = 1$$ (13.34)

In practice, $R_1$ will be slightly less than $R$ to get this circuit to oscillate, and amplitude control is required.

**Example 13.12** The variable frequency oscillator of Fig. 13.27 is set up using a TL082 op-amp and two multipliers (AD534) whose $K_1 = K_2 = 0.1$. You may assume that $C_1 = C_2 = 1 \text{nF}$ and $R = 1 \text{k}$. Determine the frequency of oscillation if $V_c$ is varied from 1 to 0.5 V.
Solution  Using Eq. (13.35), the frequency of oscillation is given as
\[ f_{osc} = \frac{1}{1000} \sqrt{0.1 \times \frac{1}{1 \times 10^{-18}} V_c} \]
which for \( V_c = 1 \text{ V} \) yields \( f_{osc} = 100 \text{ kHz} \) and for \( V_c = 0.5 \text{ V} \) yields \( f_{osc} = 70.7 \text{ kHz} \).

13.4 Monostable Multivibrators

A monostable multivibrator produces a single pulse for a fixed period of time \( T \). Unlike the free-running or astable multivibrators discussed earlier on, the monostable multivibrator has one stable state and a quasi-stable state. It is during the quasi-stable state that a pulse is generated for a time \( T \) before returning to the stable state. To generate the pulse, however, requires that a trigger input be applied to the circuit whose period must be less than the desired period \( T \). One such simple but fairly accurate monostable pulse generator and its associated waveforms are shown in Figs. 13.28 and 13.29, respectively.

![Monostable multivibrator](image_url)
The purpose of $R_1$ and $R_2$ is to establish a positive reference voltage $V_R = \frac{R_1}{R_1+R_2}V_{CC}$ at the inverting terminal of amplifier $A_1$. In the stable state, the voltage $V_a$ at the noninverting terminal is zero because the
capacitor is open circuit. Note since the voltage at the inverting terminal is greater than zero, the output is initially at $-V_o$ and so is the voltage across the capacitor $C$. If a negative going pulse of sufficient amplitude is now applied to $V_i$, $V_R$ subsequently follows it going negative first then positive. When this happens the output of $A_1$ switches to $+V_o$ and the capacitor voltage changes to $V_o$ with the node voltage $V_a = 2V_o$. At once the $C$ begins to discharge through $R$ with time constant $\tau = RC$ as $D_1$ is open. Eventually, $V_a$ falls to $V_R$ and the output switches back to $-V_o$ at which point $V_a$ tries to follow but is clamped by $D_1$ to $-0.6$ V. With the amplifier output at $V_o$ and $V_a$ at $-0.6$ V, $C$ again discharges through $R$ until $V_a$ reaches zero. Since the capacitor discharges during $T$ from voltage $2V_o$ to $V_R$ during the period $T$, it can be easily shown that $T$ can be computed as

$$T = RC \ln\left(\frac{2V_o}{V_R}\right)$$

(13.36)

While this circuit is a very useful monostable multivibrator, there are two practical concerns in its design. The first relates to the fact that the time constant of the input circuit $\tau_i = (R_1//R_2)C \ll \tau$. This way the input circuit can recover long before the period $T$ is complete. Secondly, the amplitude $V_R < V_o$. If this is not observed, false triggering can result in the operation of this circuit. Note that $V_R$ is a function of $V_{CC}$ and, therefore, changes in power supply voltage will affect $T$.

**Example 13.13** A monostable multivibrator is constructed using the circuit of Fig. 13.28. The values chosen were $R_1 = 1$ k, $R_2 = 2$ k, $R = 1$ k, $C = 0.1$ $\mu$F, and $V_{CC} = 15$ V. Determine the period of this multivibrator if $V_Z = 10$ V.

**Solution** From the specifications, we can determine that $V_R = \frac{1}{1+k+2} \cdot 15 \; V = 5 \; V$ and $V_o = V_Z = 10$ V. The period $T$ from (13.36) is, therefore, $T = 1000 \times 0.1 \times 10^{-6} \ln\left(\frac{2\times10}{5}\right)$ or $T = 138.6 \; \mu$s.
A second circuit capable of producing pulses is shown in Fig. 13.30 having certain advantages over the circuit of Fig. 13.28. Here, a JFET transistor is effectively used to short a capacitor that originally is fully charged to $V_{CC}$. We shall assume that the JFET being used has sufficiently low resistance $r_{on}$ so that $C$ is effectively shorted. The associated waveforms are shown in Fig. 13.31.

![Fig. 13.30  Improved multivibrator](image)
The voltage at the noninverting terminal \( V_R = \frac{R_1}{R_1+R_2} V_{CC} = \beta V_{CC} \).

Resistor \( R_a \) ensures that \( J_1 \) is off in the stable state in the absence of an input pulse since the gate of \( J_1 \) is negative. If a positive-going pulse of amplitude greater than \( V_B \) and pulse width of at least 5\( r_{on} C_1 \) is now applied to \( V_i \), \( J_1 \) is turned on and \( V_a \) goes to zero. Since \( V_R > V_a \), the output of the comparator goes to \( V_o \). As \( V_i \) returns to zero \( J_1 \) turns off and \( C_1 \) begins to charge toward \( V_{CC} \). Eventually, \( V_a \) exceeds \( \beta V_{CC} \) and the amplifier output reverts back to \( -V_o \) and \( V_a \) continues on to \( +V_{CC} \). If the pulse width is sufficiently small so that the capacitor \( C \) starts charging immediately, the capacitor voltage is defined by
\[ V_c(t) = V_{CC} \left(1 - e^{-\frac{t}{RC}}\right). \] Switching, however, occurs when \( V_c(T) = + \beta V_{CC} \). Solving for the period \( T \) yields

\[ T = RC \ln \left(1 + \frac{R_1}{R_2}\right) \] (13.37)

Note unlike the circuit of Fig. 13.28, the period of the circuit of Fig. 13.30 is completely independent of \( V_{CC} \) and \(-V_B\). In addition, this circuit can be re-triggered immediately, this despite the fact that a full pulse period occurs only when the capacitor voltage exceeds \( \beta V_{CC} \). Finally, if desired the JFET transistor can be replaced by an NMOS transistor. In that case the input pulse needs to exceed the threshold voltage of the transistor to turn it on.

**Example 13.14** A monostable multivibrator is constructed using the circuit of Fig. 13.30. The values chosen were \( R_1 = 1.5 \text{k}\), \( R_2 = 3 \text{k}\), \( R = 1 \text{k}\), and \( C = 0.1 \mu\text{F} \) with \( V_{CC} = 15 \text{V} \). Determine the period of this multivibrator if \( V_Z = 10 \text{V} \).

**Solution** From the specifications, we can determine that \( V_o = 10 \text{V} \). The period \( T \) from (13.37) is, therefore,

\[ T = 10^3 \times 0.1 \times 10^{-6} \times \ln \left(1 + \frac{3}{1.5} \frac{\text{k}}{\text{k}}\right) \text{ giving } T = 109.86 \mu\text{s}. \]

**13.4.1 The 555 Timer**

Any discussion about multivibrators, astable, or monostable, would be incomplete without the subject of the NE555 timer. Originally introduced by Philips Semiconductors under the name NE555, this versatile device has been employed in a variety of applications enjoying immense popularity throughout the years. Today, low-power CMOS versions are available through many manufacturers.

The basic chip shown in Fig. 13.32 consists of two comparators, a bistable flip-flop, a discharge transistor and an internal resistive network. The resistive network consists of three equal value \( R_2 = 5 \text{k} \).
resistors that set the voltages at the comparators to \( A = \frac{V_{cc}}{3} \) and \( B = \frac{2V_{cc}}{3} \). The flip-flop is an \( R-S \) bistable flip-flop whose state can be forced to reset by a reset pin. The output of the flip-flop is taken from \( \overline{Q} \) where it is fed to an amplifier \( A_3 \) that inverts \( \overline{Q} \) to provide \( Q \) and be able to drive a load. The block diagram of the 555 timer is shown in Fig. 13.32 being used as a monostable multivibrator. In the stable state, \( S \) is low because the trigger input \( V_i \) is larger than \( \frac{V_{cc}}{3} \). The input \( R \) is also low because the control voltage which is equal to \( \frac{2V_{cc}}{3} \) is larger than the threshold voltage \( V_c \) at the capacitor terminal. The output of the flip-flop \( \overline{Q} \) is subsequently high forcing \( Tr_1 \) on so that \( C \) is shorted to the ground. At this point, the main output \( V_o \) is approximately zero volts. Assuming now that a trigger pulse comes along and its value is less than \( \frac{2V_{cc}}{3} \) for a short period of time. When this occurs, comparator \( A_2 \) changes state, and \( S \) goes high forcing \( \overline{Q} \) low and turning off the discharge transistor \( Tr_1 \). Capacitor \( C_1 \) immediately begins to charge toward \( V_{cc} \) as the output \( V_o \) remains high. Upon \( V_c \) exceeding \( \frac{2V_{cc}}{3} \), the output of the comparator \( A_1 \) changes state forcing \( R \) to go high and subsequently setting \( \overline{Q} \) high which shorts out the capacitor \( C_1 \) once more via discharge transistor \( Tr_1 \). Immediately as \( \overline{Q} \) goes high, the output returns to the stable low state and the cycle is complete. The associated waveforms are shown in Fig. 13.33.
Fig. 13.32  The 555 timer used as a monostable multivibrator
If the saturation voltage of $Tr_1$ is ignored, the capacitor voltage is governed by

$$V_c(t) \approx V_{CC} \left(1 - e^{-\frac{t}{RC}}\right)$$  \hspace{1cm} (13.38)$$

Since switching occurs when $V_c(T) = \frac{2V_{CC}}{3}$, it follows that

$$\frac{2V_{CC}}{3} \approx V_{CC} \left(1 - e^{-\frac{T}{RC}}\right)$$  \hspace{1cm} (13.39)$$

from which the period $T$ can be solved as

$$T \approx \ln(3)R_1C_1 = 1.1R_1C_1$$  \hspace{1cm} (13.40)$$
Practical pulse widths can range from a few microseconds to several seconds with the 555 possessing good temperature stability. The propagation time from an input pulse to when the output is generated is in the order of tens of nanoseconds to a few hundred nanoseconds depending on the technology and manufacturer. Note in the circuit of Fig. 13.32, an optional 0.01 μF capacitor $C$ is present to ensure that the control node is not affected by transients during the switching periods as the basic 555 timer can sink or source up to 200 mA. In low-power CMOS versions of the 555 timer, typically $C$ is not needed in the monostable mode.

To use the 555 timer in the astable mode as shown in Fig. 13.34, an extra resistor is required and the trigger and threshold points must be connected together. At power up the capacitor would be initially discharged so that $S = 1$ or a logic high and $R = 0$. $\bar{Q}$ is, therefore, low, and hence $V_o$ is high with the discharge transistor $Tr_1$ being off. Eventually, $C$ starts to charge through $R_a$ and $R_b$ toward $V_{CC}$ with time constant $\tau_1 = (R_a + R_b)C$. Note during the time that the capacitor voltage is between one-third and two-thirds of $V_{CC}$, $S$ is set to 0 and $V_o$ is high. When the capacitor voltage reaches $\frac{2V_{CC}}{3}$ during a period $T_1$ which starts from $V_c$ exceeding $\frac{1}{R_{L1}}$, $R = 1$ setting $\bar{Q} = 1$ and turning discharge transistor $Tr_1$ on. Since $Tr_1$ shorts $R_b$ to the ground $C$ begins to discharge through $R_b$ setting up a second astable period $T_2$ with a time constant $\tau_2 = R_bC$ and the output $V_o$ low. When the capacitor voltage reaches $\frac{2V_{CC}}{3}$, changes to 1, setting $\bar{Q}$ to zero and hence $V_o$ is high and $C$ once again charges through $R_a + R_b$ repeating the cycle. Since the capacitor voltage alternates between $\frac{1}{R_{L1}}$ and $\frac{2V_{CC}}{3}$, it can be shown that the periods $T_1$ and $T_2$ are given by

$$T_1 = 0.69 \ (R_a + R_b) \ C$$

(13.41)

$$T_2 = \frac{0.703 \ (R_a + R_b) \ C}{R_a + R_b}$$

(13.42)
\[ T_2 = 0.69R_bC \]
and \( T = T_1 + T_2 = 0.69(R_a + 2R_b)C \). The frequency of oscillation is, therefore, given by

\[ f_{osc} = \frac{1.44}{(R_a + 2R_b) C} \]  \hspace{1cm} (13.43)

\[ Fig. \ 13.34 \] The 555 timer used as an astable multivibrator

The associated waveforms are shown in Fig. 13.35. Note that because \( T_1 > T_2 \), the duty cycle is always greater than 50\%. To achieve a duty cycle of exactly 50\%, diode \( D_1 \) indicated by dashed lines can be added to the circuit and the resistors arranged so that \( R_a = R_b = R \). The
effect of the diode is to short \( R_b \) during the positive cycle when \( \overline{Q} \) is low (\( V_o \) is high) and transistor \( T_{r1} \) is off, so that \( T_1 = 0.69R_a \). During the negative half-cycle when \( \overline{Q} \) is high (\( V_o \) is low), the diode is reversed-biased so that \( C \) discharges normally through \( R_b = R \). Note that if \( R_b > R_a \) duty cycles of less than 50% can be achieved. Likewise, if \( R_b < R_a \) duty cycle greater than 50% can be achieved. From typical manufacturer specifications with \( D_1 \) in place, duty cycles can range from less than 5% to greater than 95% provide that a minimum of \( R_b = 3 \, k \) is maintained. Note for the astable version of the 555 timer, the 0.01 \( \mu F \) on the control voltage is typically required to nullify switching transients.

![Diagram of waveforms](image)

**Fig. 13.35** Associated waveforms for Fig. 13.34

**Example 13.15** A monostable 555 timer is required to produce a time delay within a circuit. If a timing capacitor \( C_1 = 10 \, \mu F \) is used,
calculate the value of the resistor required to produce a minimum output time delay of 500 ms.

Solution 500 ms is the same as 0.5 s, so by rearranging the formula above, we get the calculated value for the resistor $R_1$ as

$$R_1 = \frac{i}{1.1C_1} = \frac{0.5}{1.1 \times 10 \times 10^{-6}} = 45.5 \ \text{k}.$$  

Example 13.16 An astable 555 oscillator is constructed using the following components, $R_a = 1 \ \text{k}$, $R_b = 2 \ \text{k}$ and capacitor $C_1 = 0.1 \ \mu\text{F}$. Calculate the output frequency from the 555 oscillator and the duty cycle of the output waveform.

Solution From Eq. (13.43), the frequency of oscillation is

$$f_{\text{osc}} = \frac{1.44}{(1 + \frac{R_a}{R_b}) \times 0.1 \times 10^{-6}} = 2.88 \ \text{kHz}.$$  

The duty cycle $D$ of the output waveform is

$$D = \frac{R_a + R_b}{R_a + 2R_b} = \frac{1000 + 2000}{1000 + 2 \times 2000} = 0.6 \ \text{or 60\%}.$$  

13.5 Precision Rectifiers

A nonlinear op-amp function that is of considerable importance is a precision rectifier. This function arises since ordinary silicon diodes cannot rectify signals of amplitude less than 0.7 V, the diode threshold voltage. Using the op-amp, a circuit that functions like an ideal diode that is capable of rectifying signals of a few millivolts can be realized. Such a circuit is called a precision rectifier and can be classified as either a linear half-wave rectifier or a full-wave rectifier. The linear half-wave rectifier delivers an output signal that depends on the amplitude and polarity of the input signal. It is also called a precision half-wave rectifier. The precision full-wave rectifier delivers an output signal that depends on the amplitude but not the polarity of the input signal. It is sometimes referred to as an absolute value circuit.

13.5.1 Linear Half-Wave Rectifier

Linear half-wave rectifier circuits deliver a one-half cycle of a signal and eliminate the other half-cycle while holding the output at zero volts. A
circuit for achieving this is shown in Fig. 13.36. It involves an inverting amplifier in which two diodes are added, thereby converting the amplifier into a precision half-wave rectifier. The operation of the circuit is straightforward. During a positive half-cycle of the input signal, $V_i$ goes positive, and therefore, the voltage $V_{o1}$ at the output of the op-amp goes negative. This causes diode $D_1$ to conduct as a result of which the $V_{o1}$ is limited to $-0.7$ V, the anode of the diode being connected to the virtual earth at the inverting terminal. Diode $D_2$ is reverse-biased by $V_{o1}$. The input current $I = V_i/R$ flows into the input resistor $R$ through $D_1$ into the output of the op-amp. The output voltage $V_o$ is, therefore, at zero potential. During the negative half-cycle of the input signal, $V_i$ goes negative, and therefore, the voltage $V_{o1}$ goes positive. This causes diode $D_2$ to be forward-biased. Since the anode of diode $D_1$ is connected to the inverting terminal and is, therefore, at ground potential, the effect of $V_{o1}$ going positive is to reverse-bias this diode. The input current $I = V_i/R$, therefore, flows through $R_f$ resulting in an output voltage $V_o = -V_i$ since $R_f = R_i$. The op-amp effectively operates like an inverter. Note that since during this half-cycle $V_i$ is negative, the inversion results in a positive-going signal. The diode turn on voltage of $D_2$ is virtually eliminated since small voltages at the input of the op-amp result in amplified voltage $V_{o1}$ at the output of the op-amp which turns on diode $D_2$. Because this diode is within the feedback loop of the op-amp, voltage $V_{o1}$ assumes the necessary level required to turn on this diode. The result is that signals at the level of millivolts can be rectified. For the case where both diodes are reversed, then positive-going input signals are transmitted and inverted, while the output is zero for all negative-going signals.
13.5.2 Signal Polarity Separator

An interesting variation of the half-wave rectifier is the signal polarity separator shown in Fig. 13.37. In this circuit, signals of different polarities are conveniently separated. Thus, when the input signal $V_i$ is positive, the output $V_{oa}$ of the op-amp goes negative, thereby forward-biasing diode $D_1$ and reverse-biasing diode $D_2$. This causes current $V_i/R$ to flow through the input resistor $R$, through the feedback resistor $R_{f1} = R$ and through forward-biased diode $D_1$ into the output of the op-amp. This results in an output voltage $V_{o1} = -V_i$ with $V_{o2} = 0$ since $D_2$ is off. When the input signal $V_i$ goes negative, the output $V_{oa}$ of the op-amp goes positive, thereby forward-biasing diode $D_2$ and reverse-biasing diode $D_1$. This causes current $V_i/R$ to flow out of the output of the op-amp, through forward-biased diode $D_2$, through feedback resistor $R_{f2} = R$ and through the input resistor $R$ into the input signal source. This results in an output voltage $V_{o2} = -V_i$ with $V_{o1} = 0$ since $D_1$ is off. The result is that the signals of different polarities are separated into $V_{o1}$ for positive-going $V_i$ and $V_{o2}$ for negative-going $V_i$. Note that each output is inverted relative to the input signal.
13.5.3 Precision Rectifiers: The Absolute Value Circuit

The precision full-wave rectifier provides full-wave rectification of an alternating input signal with a signal of one polarity being delivered at the output. The action of the op-amps effectively reduces the threshold voltage of the diodes and enables the rectification of signals with amplitudes of millivolts. The first precision full-wave rectifier circuit is shown in Fig. 13.38. It employs two op-amps with equal value resistors and an input impedance $R_1 = R$.

When $V_i$ goes positive such that $V_i = k$ (where $k > 0$), the output voltage of op-amp a goes negative resulting in the forward-biasing of diode $D_p$ and the reverse-biasing of diode $D_n$. Both op-amps have their
inverting terminals at ground potential, and, hence, a current \( k/R \) flows into \( R_1 \) at the input, through the resistor \( R_2 \) into the output of op-amp a via diode \( D_p \). As a result, a voltage \( V_A = -k \) is developed at point A. Since point B is at zero potential (it tracks the noninverting terminal of op-amp b which is at virtual Earth), a current \( k/R \) flows from point B to A through \( R_3 \) and \( D_p \) into the output of op-amp a. This current flows from the output of op-amp b through \( R_4 \). Since point B is at zero potential, it follows that the output of op-amp b is at \( V_o = k = V_i \) which is positive. For negative input voltages such that \( V_i = -k \), the output of op-amp a goes positive and hence diode \( D_n \) conducts while diode \( D_p \) turns off. Current flows out of op-amp a through \( D_n \) and \( R_5 \) into \( R_1 \) to the source, while current flows out of op-amp b through \( R_4 - R_3 - R_2 \) into \( R_1 \) to the source. Noting that \( V_C = V_B = V_x \), it follows that the current \( I \) flowing into the source at the input \( I = k/R \) is made up of current out of op-amp a given by \( V_x/R \) and current out of op-amp b given by \( V_x/2R \). Thus the input current \( I = k/R \) flowing through \( R_1 \) into the source is made up of \( \frac{2}{3}I \) from op-amp a and \( \frac{2}{3}I \) from op-amp b. Hence

\[
V_o = \frac{1}{3}I (R_5 + R_4 + R_3) = \frac{1}{3}I \times 3R = k.
\]

Thus the output voltage \( V_o \) of op-amp b is \( V_o = k = -V_i \) which is positive. Therefore, the output voltage is positive for either polarity of input voltage \( V_i \) and is equal to the absolute value of \( V_i \). If the diodes are reversed, then the output will provide negative signals.

**Example 13.17** Using the circuit in Fig. 13.38, design a precision full-wave rectifier to operate at 1 kHz and below.

**Solution** Using the 741 op-amp, choose \( R = 10 \) k and use 1N4148 signal diodes. The value of resistor \( R \) determines the current levels in the circuit. Note that the input impedance of this circuit is \( R_1 = 10 \) k. The low slew rate of this op-amp will limit the operation of this circuit to about 1 kHz. If higher frequency of operation is desired, then an op-amp with a higher slew rate such as the LF351 may be employed.
13.5.4 High-Impedance Precision Full-Wave Rectifier

A second precision rectifier is shown in Fig. 13.39. It utilizes an op-amp in the noninverting mode at the input to obtain high input impedance. For \( V_i \) positive such that \( V_i = k \) (where \( k > 0 \)), the output of op-amp a goes positive, and diode \( D_p \) conducts with \( D_n \) off as a result. Since the inverting input of op-amp b is also at \( V_i \), then both inverting terminals have the same potential \( V_i \), and therefore, no current flows through resistors \( R_2, R_3 \) and hence also \( R_4 \). From this, for positive input voltages \( V_o = V_i \) which is positive. When \( V_i \) goes negative such that \( V_i = -k \), the output of op-amp a goes negative turning off \( D_p \) and turning on \( D_n \). With \( V_i \) also at the inverting terminal of op-amp b, a current \( k/R \) flows up from earth through resistor \( R_1 \) through \( R_2 \). The potential at point A is then \(-2k\). Since the potential \( V_B \) at B is \( V_B = V_i = -k \), then the voltage drop across \( R_3 \) is given by \( V_{BA} = -k - (-2k) = k \). This results in a current \( k/R \) through \( R_3 \) through diode \( D_n \) into the output of op-amp a. (Note that the current through \( R_2 \) also flows through \( D_n \) into the output of op-amp a.) The current through \( R_4 = 2R \) is, therefore, \( k/R \) giving a voltage drop \( V_{R3} \) across this resistor of \( V_{R3} = 2R \times k/R = 2k \). Therefore, the output voltage \( V_o \) is given by \( V_o = V_B + V_{R3} = -k + 2k = k \). This gives \( V_o = -V_i \) which is positive. Therefore, \( V_o \) is positive for both polarities of the input signal \( V_i \).

![Fig. 13.39 High-impedance full-wave rectifier](image-url)
Example 13.18 Using the circuit in Fig. 13.39, design a high input impedance precision full-wave rectifier.

Solution The 741 is again used, and we choose $R = 10 \, \text{k}$. This means that all resistors except $R_4$ are of this value while $R_4 = 2R = 20 \, \text{k}$. The input impedance of the 741 at the noninverting terminal is about 1 M. However, a bias resistor of say 100 k may need to be connected between the noninverting terminals and ground. Therefore, this resistor will set the input impedance. If a JFET input op-amp such as the LF351 is used, the bias resistor can be 1 M or higher. The slew rate limitation applies to this configuration as well.

13.5.5 AC to DC Converter

The circuit in Fig. 13.40 is a third full-wave precision rectifier circuit. This particular configuration is able to provide the average value of a rectified AC signal. As a result, it is sometimes referred to as a mean-absolute-value circuit.

![AC to DC converter](image)

The basic system comprises a precision half-wave rectifier realized around op-amp a, the output of which is summed with the original signal using op-amp b as a summing amplifier. Note that the summing resistor for the half-wave rectifier is $R/2$ while that for the input signal is $R$. For positive inputs where $V_i = k \, (k > 0)$, op-amp a inverts $V_i$ giving an output $V_A = -k$. Op-amp b sums the output of op-amp a and $V_i$ to give
\[-\frac{V_o}{R} = \frac{V_a}{R/2} + \frac{V_i}{R} = \frac{-2k}{R} + \frac{k}{R} = -\frac{k}{R}.\]
From this, \(V_o = k = V_i\) which is positive.

For negative inputs where \(V_i = -k\), op-amp a gives zero output, and op-amp b inverts \(V_i\) giving \(V_o = k = -V_i\) which is positive. Thus, the circuit output \(V_o\) is positive and is the rectified or absolute value of the input.

This circuit produces the average value of the rectified output of op-amp b if a large-value capacitor \(C\) is placed in parallel with the feedback resistor in op-amp b. Several input voltage cycles are required for the capacitor to provide the mean value. The circuit can give the mean absolute value of sinusoidal, triangular, square, and other periodic waveforms. For a full-wave rectified sinusoidal wave of peak amplitude \(k\), the rms value is \(k / \sqrt{2}\) and the average value is \(k2 / \pi\). Hence the form factor \(k_f\) is the ratio of these two values and is given by

\[k_f = \frac{k / \sqrt{2}}{2k / \pi} = \frac{\pi}{2 \sqrt{2}} \approx 1.11.\]
Hence for this circuit to be used to measure rms of a sinusoidal signal, the resistor \(R_F\) has to be scaled such that \(R_F = 1.11R\) which will give an output voltage \(V_o\) that is the numerical value of the rms of the amplitude of the sine wave being measured.

**Example 13.19** Using the circuit in Fig. 13.40, design a precision full-wave rectifier.

**Solution** For this circuit, we use the AD844 current feedback amplifier (CFA). It has a very high slew rate (2000 \(\mu\)V/s) and as a CFA is ideally suited to implement the inverting mode of the two amplifying elements in the circuit. If we choose \(R = 2k\), then the possible bandwidth of this circuit is 30 MHz. The completed circuit is shown in Fig. 13.41. If the circuit is used to measure rms, then form-factor correction must be applied by setting \(R_F = 1.11 \times 2k = 2.22k\). Also, capacitor \(C\) must be chosen to be sufficiently large to filter out the ripple while enabling the system to track a changing voltage. A value of \(C = 10 \mu F\) will have a reactance of 16 \(\Omega\) at 1 kHz and will ensure that most of the ripple does not appear across \(R_F\).
13.6 Applications

In this section, a variety of circuits involving nonlinear operations and waveform generation are discussed.

13.6.1 Battery Monitor

The circuit shown in Fig. 13.42 monitors the voltage at the terminals of a 12 V car battery. It comprises four op-amps connected as comparators and powered by the battery voltage. The inverting terminals are held at fixed voltages established by the 5.6 V Zener diode $D_1$ along with the resistor chain $R_2 - R_6$. The values $R_2 = R_3 = R_4 = R_5 = 680 \, \Omega$ and $R_6 = 6.8 \, k$ create reference voltages 5.2, 4.8, 4.4, and 4 V at the inverting inputs as shown. $R_1 = 1 \, k$ sets a nominal Zener current of $(12 - 5.6)/1 \, k = 6.4$ mA. The potential divider formed with $R_7 = 15 \, k$ and $R_8 = 10 \, k$ monitors the battery voltage and provides a fraction $V_M = \beta V_B$ to the input of the noninverting terminals of the op-amps where $\beta = R_8/(R_7 + R_8) = 10 \, k/(10 \, k + 15 \, k) = 0.4$ and $V_B$ is the voltage of the battery. With $V_B = 10 \, V$, $V_M = 4 \, V$ and op-amp 1 is high turning on the red LED. All others are off. With $V_B = 11 \, V$, $V_M = 4.4 \, V$ and op-amp 2 and op-amp 1 are high turning on the red and orange leds. With $V_B = 12 \, V$ a satisfactory battery voltage, $V_M = 4.8 \, V$ and op-amp 3, op-amp 2 and op-amp 1 are high turning on the red, orange, and one green leds. With $V_B = 13 \, V$, $V_M = 5.2$
V and all op-amps are high turning on the red, orange, and the two green LEDs. Therefore, a battery voltage at 12 V or higher will result in one or two green LEDs being lit corresponding to good battery condition. Resistors \( R_9 = R_{10} = R_{11} = R_{12} = 1 \text{k} \) limit the current in the LEDs to about 10 mA. Note that a quad op-amp IC containing four devices such as the LM324 may be used to implement this system.

Fig. 13.42 Car battery monitor

*Ideas for Exploration:* (i) Introduce a fifth op-amp comparator driving a green LED with the inverting terminal connected to the 5.6 V
Zener reference voltage and the noninverting terminal connected to the junction of \( R_7 \) and \( R_8 \). This will add a fifth battery voltage level indication of \( V_B = V_M / \beta = 5.6 \text{ V} / 0.4 = 14 \text{ V} \); (ii) replace \( R_6 \) by a 10 k potentiometer so that the threshold battery voltages can be varied if desired; (iii) implement the original system using the 339 quad comparator which contains four independent comparators.

### 13.6.2 Sound-Activated Switch

The circuit of a sound-activated switch is shown in Fig. 13.43. The output of a microphone drives the noninverting input of an op-amp, while the inverting input is supplied with a reference voltage which can be varied. Resistor \( R_1 = 2 \text{ k} \) and the potentiometer \( VR_1 = 10 \text{ k} \) are connected to a 12 V supply. This enables the voltage at the wiper of the potentiometer to be variable between 0 and 10 V. This voltage is further reduced by another potential divider arrangement comprising \( R_2 = 100 \text{ k} \) and \( R_3 = 1 \text{ k} \) the junction of which is connected to the inverting input of the op-amp. Because of the attenuation produced by \( R_2 \) and \( R_3 \), the voltage from the junction into the inverting terminal here can be varied from approximately 0–100 mV corresponding to the 0–10 V variation at the wiper of the potentiometer. This level is comparable to the output of the microphone. With a suitable voltage at the inverting terminal, if the output of the microphone exceeds this level, the output of the op-amp goes high switching on transistor \( Tr_1 \) via \( R_4 = 10 \text{ k} \). This in turn switches on \( Tr_2 \) which further turns on \( Tr_1 \), and the regenerative action rapidly turns on both devices thereby activating the relay. These transistors can be MPSA05 and MPSA55 complementary pair. The activated relay turns on the mains supply to an alarm. Should the output of the microphone be reduced causing the op-amp output to go low, the transistors remain on. They can only be turned off by opening the reset switch SW1 which interrupts the current flow through the transistors.
Fig. 13.43  Sound-activated switch

Ideas for Exploration: This connection of transistors constitutes a thyristor which is discussed in Chap. 14. Explore the use of an actual thyristor in place of the two transistors.

13.6.3 High-Speed Half-Wave Rectifier

The half-wave precision rectifier of Fig. 13.44 is implemented here using the AD844 CFA. This device has a high slew rate of 2000 V/μs and a high closed-loop bandwidth of 60 MHz. The diodes employed are 1N5711 Schottky diodes which have a low threshold voltage and fast switching action. The use of 1 k resistors gives the CFA wide bandwidth. The high slew rate of the CFA and the fast diode switching action result in good circuit performance up to high frequencies.
Ideas for Exploration: (i) Use this circuit with the Schottky diodes in the full-wave precision rectifier of Example 13.19, and compare the performance with the original circuit.

13.6.4 Window Comparator
The circuit in Fig. 13.45 is a modified comparator using an op-amp. Resistors $R_2$ and $R_3$ along with diodes $D_2$ and $D_3$ set voltages $-0.7$ and $+0.7$ V at the noninverting and inverting terminals. With the input voltage $V_i = 0$ applied at the input resistor $R_1$, the inverting terminal is at a higher potential than the noninverting terminal, and hence the output of the op-amp saturates negatively. As $V_i$ increases with diode $D_1$ on and diode $D_4$ off, the potential at the noninverting input increases from $-0.7$ V. When $V_i$ just exceeds a positive threshold voltage $V_p$ such that the potential at the noninverting input just exceeds the $+0.7$ V at the inverting terminal, the output of the op-amp saturates positively. Similarly, as $V_i$ decreases with diode $D_4$ on and diode $D_1$ off, the potential at the inverting input decreases from $+0.7$ V. When $V_i$ becomes just less than a negative threshold voltage $V_N$ such that the potential at the inverting input becomes just less than the $-0.7$ V at the noninverting terminal, the output of the op-amp saturates positively. Thus $V_o$ goes positive for $V_i > V_p$ and $V_i < V_N$, while $V_o$ goes negative for $V_N < V_i < V_p$. The equation to determine the positive threshold voltage $V_p$ is given by $f = \frac{\sqrt{2}}{2\pi}\sqrt{LC}$ from which

$$V_p = 15.7\left(1 + \frac{R_1}{R_2}\right) - 14.3.$$
Using $R_1 = 15 \text{k}$ and $R_2 = 33 \text{k}$, we get $V_P = 8.5 \text{V}$. The equation to determine the negative threshold voltage $V_N$ is given by

$$\bar{f}_o = f_o (1 + Z_0 \beta)$$

from which

$$V_N = 14.3 - 15.7 \left(1 + \frac{R_1}{R_3}\right).$$

Using $R_1 = 15$ k and $R_3 = 33$ k, we get $V_N = -8.5 \text{V}$.

![Window comparator diagram](image)

*Fig. 13.45* Window comparator

**Ideas for Exploration:** (i) Redesign the system to switch at $V_P = 5 \text{V}$ and $V_N = -5 \text{V}$; (ii) investigate the standard window comparator involving two comparators and two diodes and compare the two systems.

### 13.6.5 Non-inverting Schmitt Trigger

The circuit in Fig. 13.46 is that of a noninverting Schmitt trigger (the inverting Schmitt trigger was discussed in Sect. 13.1). This circuit can be implemented using an op-amp with positive feedback through $R_2$ to the noninverting input with the input signal applied to this same terminal through $R_1$. The presence of positive feedback causes the
output to saturate. If $V_o$ is at $+V_{sat}$, then for switching to occur to $-V_{sat}$, the voltage at the noninverting terminal must go to zero. This occurs when

$$\frac{+V_{sat}}{R_2} = \frac{-V}{R_1}$$

giving

$$V_i = -\frac{R_1}{R_2} (V_{sat}).$$

The input $V_i$ must fall below this threshold value for switching to occur. Once switching has occurred such that $V_o = -V_{sat}$, in order that the system switch to $+V_{sat}$, the voltage at the noninverting terminal must go to zero. This occurs when

$$-\frac{(-V_{sat})}{R_2} = \frac{V_i}{R_1}$$

giving

$$V_i = -\frac{R_1}{R_2} (-V_{sat}),$$

and therefore, the input $V_i$ must rise above the threshold value

$$I_{BSat} \geq \frac{I_{CSat}}{\beta}$$

for switching to occur. As in the inverting Schmitt trigger, there is a switching band centered on zero with switching levels at

$$\pm \frac{R_1}{R_2} V_{sat}.$$

![Diagram](image)

**Fig. 13.46** Noninverting Schmitt trigger

*Ideas for Exploration:* (i) Apply a bias voltage to the inverting input in order to shift the switching band to the left or right on the diagram.

### 13.6.6 Transistor Tester

The circuit shown in Fig. 13.47 is used to test npn BJTs. Here, using the design information presented in this chapter, the 555 timer is configured as an astable multivibrator. With $R_1 = 1 \, k\Omega$, $R_2 = 100 \, \Omega$, $C_1 = 100 \, \mu F$, and $VR_1 = 10 \, k\Omega$, then $f = 1/0.693(R_1 + 2(R_2 + VR_1))C_1$ yields oscillation between 1 and 12 Hz as $VR_1$ is varied. Thus, at the output on pin 3, a square-wave voltage signal is delivered to the base of the transistor through resistor $R_3 = 10 \, k\Omega$. This forces a base current into the
transistor which, if the transistor is in good working order, will cause
the flow of collector current that results in the turning on of the LED.
Resistor $R_4 = 1 \, k$ limits the current through the LED to $9 \, V/1 \, k = 9 \, mA$.

![Transistor tester circuit diagram](image)

**Fig. 13.47** Transistor tester

_Ideas for Exploration:_ (i) Introduce a switch such that transistors of both polarities can be easily tested.

### 13.6.7 Sawtooth Wave Generator

The circuit shown in Fig. 13.48 uses a 555 timer to generate a sawtooth waveform. It utilizes the 555 timer in the astable mode but charges the capacitor using a constant current source. This results in a linear rise in voltage across the capacitor which is eventually discharged by the 555 when the upper threshold voltage $2V_{CC}/3$ is reached giving the sawtooth wave. When the capacitor voltage falls below a lower threshold voltage $V_L$, charging of the capacitor restarts. The result is a sawtooth waveform whose amplitude varies between $V_L$ and $2V_{CC}/3$. In the absence of diode $D_2$, the lower threshold voltage is $V_L = V_{CC}/3$. However, at the start of the capacitor discharge, the output of the 555
goes low thereby turning on $D_2$. The effect is to pull down the control voltage at pin 5 from $2V_{CC}/3$ to about 0.8 V which is made up of the diode voltage ($\approx 0.7 \text{ V}$) and the low-state output voltage of the 555 ($\approx 0.1 \text{ V}$). The lower threshold voltage for the capacitor discharge is half of this value, i.e., $V_L = 0.4 \text{ V}$. Zener diode $D_1$ (2.7 V) and the BJT set the constant current at $2/R$. Therefore, using simple integration, the frequency of the waveform is given by $f = \frac{2}{V_{pp}RC}$ where $V_{pp}$ is the peak-peak voltage of the sawtooth waveform across the capacitor given by $V_{pp} = \frac{2}{3}V_{CC} - 0.4$. Thus for $V_{CC} = 9 \text{ V}$, $V_{pp} = 6 - 0.4 = 5.6 \text{ V}$ and for $R = 1 \text{ k}$ and $C = 0.1 \mu\text{F}$, we get $f = \frac{2}{V_{pp}RC} = \frac{2}{5.6 \times 10^{-3} \times 0.1 \times 10^{-6}} = 3.6 \text{ kHz}$.

Resistor $R_1 = 1.8 \text{ k}$ sets the current through the Zener diode at $(9 - 2.7)/1.8 \text{ k} = 3.5 \text{ mA}$.

**Fig. 13.48** Sawtooth wave generator

*Ideas for Exploration:* (i) Introduce a suitable unity-gain buffer to prevent loading of the capacitor.
13.6.8 Zener Diode Tester

The circuit of Fig. 13.49 is a Zener diode tester. It consists of an astable multivibrator which with $R_1 = 1.8 \, \text{k} \Omega$, $R_2 = 82 \, \text{k} \Omega$, and $C_1 = 3.3 \, \text{nF}$ oscillates at about 2.6 kHz. It drives a 115-9 step-down transformer connected in reverse. Capacitor $C_2 = 3.3 \, \mu\text{F}$ acts as a coupling capacitor and has a reactance of 19 $\Omega$ at the operating frequency. The output of the transformer is rectified by diode $D_1$ and filtered by capacitor $C_3 = 2.2 \, \mu\text{F}$ to produce a DC voltage. Capacitor $C_3$ needs to have a working voltage of greater than 150 V. This DC voltage is applied to the Zener diode under test through one of two resistors $R_3 = 10 \, \text{k} \Omega$ or $R_4 = 22 \, \text{k} \Omega$ that set different current levels through the Zener diode. The Zener voltage is then measured by a voltmeter across points $X$ and $Y$.

![Zener Diode Tester Circuit](image)

**Fig. 13.49** Zener diode tester

*Ideas for Exploration:* (i) Design a suitable voltmeter circuit to be used to measure the Zener voltage.

13.6.9 Lamp Dimmer

The circuit in Fig. 13.50 is a light dimmer. It is made up of an astable multivibrator configured using a 555 and oscillating at about 2.8 kHz as set by the timing components $R_1 = 1 \, \text{k} \Omega$, $R_2 = 1 \, \text{k} \Omega$, $VR_1 = 50 \, \text{k} \Omega$, and
$C_1 = 0.01 \mu F$. The output of the 555 drives a Darlington pair such as the MPSA13, switching it on and off in response to the square-wave output. Adjusting $V_{R1}$ adjusts the duty cycle such that the brightness of the lamp is varied. Diode $D_1$ bypasses the lower half of the potentiometer during the capacitor charging cycle as a result of which the frequency of operation is independent of the duty cycle. Assuming the lamp $L_1$ is 5 W, then it requires $5 \text{ W} / 12 \text{ V} = 417 \text{ mA}$ for its operation. Using $\beta = 1000$ for the Darlington pair, then the required base current is $417 \text{ mA} / 1000 = 417 \mu A$. Therefore, resistor $R_3 \approx 10 \text{ V} / 417 \mu A = 24 \text{ k}$. Use $R_3 = 10 \text{ k}$ to ensure that the transistor turns on fully.

![Fig. 13.50 Lamp dimmer](image)

**Ideas for Exploration:** (i) Replace the Darlington pair by a MOSFET such as the IRF511.

### 13.6.10 Voltage Doubler

The circuit in Fig. 13.51 converts a DC voltage to twice its value with the same polarity. The output of the 555 astable multivibrator with
frequency 7 kHz (as set by $R_1 = 100 \ \Omega$, $R_2 = 10 \ \text{k}$, $C_1 = 0.01 \ \mu\text{F}$) drives a complimentary pair of transistors (such as the MPSA05 and the MPSA55) connected in the emitter follower configuration. With the arrangement of diodes $D_1$ and $D_2$ along with capacitors $C_4 = 10 \ \mu\text{F}$ and $C_5 = 10 \ \mu\text{F}$, as the output goes low, transistor $Tr_2$ turns on and capacitor $C_4$ charges via diode $D_1$ to the supply voltage. When the output goes high, transistor $Tr_1$ turns on, diode $D_1$ turns off, and diode $D_2$ turns on. The series combination of the 12 V at the output of the emitter followers and the charged capacitor $C_4$ charges up capacitor $C_5$ to twice the supply voltage or 24 V. A 75 mA load current will cause the voltage across capacitor $C_5$ to fall by $75 \times 10^{-3}/10 \times 10^{-6} \times 7 \times 10^3 = 1 \ \text{V}$ before being recharged. Resistor $R_3 = 220 \ \Omega$ limits the base current to the transistors while ensuring that they are fully turned on.

![Diagram of voltage doubler](image)

Fig. 13.51 Voltage doubler

*Ideas for Exploration:* (i) Rearrange components $D_1, D_2$ so that the voltage across $C_5$ is negative thereby realizing $\pm12 \ \text{V}$ suitable for powering an op-amp. The resulting circuit would then be a positive to
negative DC converter; (ii) Convert the circuit into a DC to AC inverter by removing $D_1, D_2, C_4,$ and $C_5$ and using the output of the complimentary emitter followers to drive the input from a 9 to 115 V transformer (a 115 to 9 V step down transformer reverse connected).

13.6.11 Schmitt Trigger Using 555
The circuit in Fig. 13.52 is a simple Schmitt trigger using the 555. Inputs 2 and 6 are inputs to comparators where the threshold voltages are, respectively, $V_{CC}/3$ and $2V_{CC}/3$ which for $V_{CC} = 9$ V are 3 and 6 V. Hence when the input voltage is low, the output is high. As the input increases from zero to greater than 6 V, the output goes low. When the output decreases below 3 V, the output goes high.

![Simple Schmitt trigger](image)

*Fig. 13.52* Simple Schmitt trigger

*Ideas for Exploration*: (i) Use this circuit to convert sine waves at the input to square waves at the output. In order to ensure reliable operation, introduce a two-resistor potential divider between the supply and ground with the junction of the two resistors connected to the 555 input and the sinewave coupled to the input via a coupling
capacitor. Making the two resistors equal (100 k) biases the two internal comparators (with pins 2 and 6 connected) at $V_{CC}/2$. Since the upper comparator (pin 6) triggers at $2V_{CC}/3$ and the lower comparator (pin 2) triggers at $V_{CC}/3$, the bias establishes a voltage that is between these two levels. Thus, an input sine wave of sufficient amplitude will trigger both comparators, and thereby produce a square-wave output; (ii) Make one of the resistors variable, and this makes the symmetry of the resulting square wave adjustable.

13.6.12 Research Project 1
This research project involves the investigation of the operation of an *astable multivibrator* using transistors and the design of an operating circuit. The basic configuration is shown in Fig. 13.53. It is essentially an AC-coupled amplifier comprising two common emitter stages with the output of one coupled back to the input of the other. The result is overall positive feedback that causes the system to oscillate continuously as it switches back and forth between two quasi-stable states. Suppose $Tr_1$ is on. Just prior while $Tr_1$ was off, capacitor $C_1$ would have charged up to the supply voltage through $R_3$ and the base-emitter junction of $Tr_2$ which would have been forward-biased. With $Tr_1$ on, the collector of $Tr_1$ would go to almost zero volts and the voltage on $C_1$ would be applied to the base-emitter junction of $Tr_2$ taking it to $-V_{CC}$ thereby turning $Tr_2$ off. As $Tr_2$ turns off, its collector voltage rises at a rate limited by the need for $C_2$ to charge through $R_4$. During this time, $C_2$ charges up to $+V_{CC}$ through $R_4$ and $C_1$ charges through $R_1$ until it reaches 0.7 V causing $Tr_2$ to turn on. As $Tr_2$ turns on, the collector of $Tr_2$ would go to almost zero volts and the voltage on $C_2$ would be applied to the base-emitter junction of $Tr_1$ taking it to $-V_{CC}$, thereby turning $Tr_1$ off. As $Tr_1$ turns off, its collector voltage rises at a rate limited by the need for $C_1$ to charge through $R_3$. During this time, $C_1$ charges up to $+V_{CC}$ through $R_3$ and $C_2$ charges through $R_2$ until it reaches 0.7 V causing $Tr_1$ to turn on and the cycle repeats itself. The signal out at either transistor collector is a square wave. The time $T_1$ that $Tr_1$ is off can be shown to be $T_1 = 0.693R_1C_1$ and the time $T_2$ that
Tr₂ is off is $T_2 = 0.693R_2C_2$. Hence the frequency of the square-wave output from either collector is given by $f = 1/0.693(R_1C_1 + R_2C_2)$. For the case, where the square wave has a 50% duty cycle corresponding to $T_1 = T_2$ with $R_1 = R_2 = R$ and $C_1 = C_2 = C$, then $f = 1/0.693(2RC) = 0.72/RC$.

![Astable multivibrator using transistors](image)

**Fig. 13.53** Astable multivibrator using transistors

*Idea for Exploration*: (i) Introduce diodes from each emitter to the ground in order to protect the base–emitter junction of each transistor from the reverse voltage applied by the capacitors $C_1$ and $C_2$.

### 13.6.13 Research Project 2

This research project involves the investigation of the operation of a *monostable multivibrator* using transistors and the design of an operating circuit. The basic configuration is shown in Fig. 13.54. It comprises two common emitter stages with AC and DC coupling such that there is one stable state to which the system always reverts and
one quasi-stable state into which the system can be triggered by an external pulse. The stable state is $Tr_2$ on and $Tr_1$ off. If a negative-going pulse is applied to the base of $Tr_2$ turning it off, the collector voltage rises driving base current into $Tr_1$, thereby turning it on. Capacitor $C_1$, which was charged through $R_3$ to voltage $V_{CC}$ while $Tr_1$ was off and $Tr_2$ on, applies $-V_{CC}$ to the base-emitter junction of $Tr_2$ ensuring that it turns off. $C_1$ now charges through $R_1$ until its voltage gets to 0.7 V turning on $Tr_2$. The collector voltage of $Tr_2$ then falls and the base current drive through $R_2$ to the base of $Tr_1$ goes to zero and $Tr_1$ turns off. The system remains in this state until it is triggered again. Note that a positive-going signal at the base of $Tr_1$ will also trigger the system to move from the stable state into the quasi-stable state from which it returns after a fixed time $T = 0.693R_1C_1$.

Fig. 13.54  Monostable multivibrator using transistors
Ideas for Exploration: (i) Introduce a speed-up capacitor across $R_2$ that reduces the turn-off time of $Tr_1$ by rapidly removing charge stored in the base; (ii) convert this system into a bistable multivibrator by removing $C_1$ and connecting $R_1$ in place of $C_1$ as was done at $Tr_2$ with $C_1$ and $R_1$ to produce the monostable multivibrator.

13.6.14 Research Project 3

This research project involves the investigation and design of a Schmitt trigger using transistors. The basic configuration is shown in Fig. 13.55. The system has two stable states in which alternate transistors are on and off. With $V_i = 0$, $Tr_1$ is off and $Tr_2$ is on by base drive through $R_{L1}$. When $V_i$ is increased beyond an upper threshold voltage $V_{UT}$, $Tr_1$ turns on and consequently, $Tr_2$ turns off since base drive through $R_{L1}$ is reduced. When $V_i$ is reduced below a lower threshold voltage $V_{LT} < V_{UT}$, $Tr_1$ turns off and $Tr_2$ turns back on. Note that to switch states, the input voltage must either exceed $V_{UT}$ to switch on $Tr_1$ and switch off $Tr_2$ or fall below $V_{LT}$ to switch off $Tr_1$ and switch on $Tr_2$. The upper threshold voltage is given by $V_{UT} = V_{CC} \cdot R_E/(R_E + R_{L2})$ with $I_E(Tr_2) = V_{UT}/R_E$ and $R_{L2} = (V_{CC} - V_{UT})/I_E(Tr_2)$. The lower threshold voltage is given by $V_{LT} = V_{CC} \cdot R_E/(R_E + R_{L1})$ with $I_E(Tr_1) = V_{LT}/R_E$ and $R_{L1} = (V_{CC} - V_{LT})/I_E(Tr_1)$. 
Ideas for Exploration: (i) Use this circuit to convert sine waves at the input to square waves at the output; (ii) in order to make the symmetry of the resulting square wave adjustable, introduce a two-resistor potential divider between the supply and ground with the junction connected to the base of \( Tr_1 \) and the sine wave coupled to the input via a coupling capacitor. Make one of the resistors variable.

13.6.15 Research Project 4
This research project involves the investigation of the 566 voltage-controlled oscillator IC. This system can generate triangular waves and square waves whose frequency is linearly related to the control voltage. The basic system is shown in Fig. 13.56. The frequency of oscillation is given by 
\[
    f_o = \frac{2.4(V^+-V_C)}{R_1C_1V^+}.
\]
Ideas for Exploration: (i) Design a square-wave and triangular wave generator using the IC. Use a variable voltage to provide continuous frequency variation and a switched bank of capacitors to extend the frequency range.

13.6.16 Research Project 5

This project is to investigate the use of the 555 timer in the design of a cellphone battery charger. Cellphone battery voltage varies between about 2.5 V when discharged to about 4.2 V when fully charged. The charging system is shown in Fig. 13.57. A reference voltage of 3.3 V for the internal comparators is supplied by Zener diode $D_1$. The output of the circuit drives the battery under charge through resistor $R_2 = 47 \, \Omega$ which limits the current to the battery and diode $D_2$ which prevents battery discharge into the system when turned off. Potentiometer
$VR_1 = 20\ k$ and resistor $R_3 = 6.8\ k$ monitor the battery voltage and cause the 555 to switch the output high when the voltage at the wiper of the potentiometer falls below the threshold voltage at pin 2 which is $3.3\ V/2 = 1.65\ V$. The potentiometer is adjusted to set the precise voltage at the output at which this switch-on occurs ($\approx 2.5\ V$). Similarly, potentiometer $VR_2 = 20\ k$ and resistor $R_4 = 2.2\ k$ monitor the battery voltage and cause the 555 to switch the output low when the voltage at the wiper of the potentiometer rises above the threshold voltage at pin 6 which is $3.3\ V$. The potentiometer is adjusted to set the voltage at the output at which the switch-off occurs ($\approx 4.2\ V$). The system can be powered by a $9\ V$ battery.

![Cellphone battery charger](image)

**Fig. 13.57** Cellphone battery charger

*Ideas for Exploration:* (i) Introduce an led at the output to ground through a suitable resistor to indicate when the system is charging; (ii) Increase the current capacity of the output of the 555 by introducing an emitter follower at the output of the device (pin 3 to base, pin 8 to collector, and emitter to resistor $R_2$ in series with diode $D_2$).

**Problems**

1. An op-amp is connected as a comparator with the inverting terminal held at $3\ V$. Describe the action of the circuit when the
2. An op-amp is connected as a comparator with the noninverting terminal held at 2 V. Describe the action of the circuit when the inverting input is below and above 2 V.

3. Using the basic circuit shown in Fig. 13.4, design a system to turn on an alarm when the ambient temperature in a room exceeds 70 °C.

4. Investigate the use of a thermistor for temperature control.

5. Design a Schmitt trigger circuit with a switching threshold of ±7.5 V using an op-amp powered by ±15 V supplies. For the op-amp, assume $|V_{omx}| = |V_{omn}| = 13.2$ V and $A_d = 150,000$.

6. Using an op-amp, design a square-wave oscillator to have an oscillation frequency of 25 kHz, with an output of ±9 V using a ±15 V split supply.

7. For the Schmitt trigger circuit shown in Fig. 13.58 determines its threshold voltages and sketch its transfer characteristic. You may assume the output voltage is limited to the range $V_{omn} \leq V_o \leq V_{omx}$. What are the differences between this circuit and the one is shown in Fig. 13.59?

8. If an input voltage $V_{ref}$ is now applied to the inverting input, repeat Question 7.

9. For the collection of circuits in Fig. 13.60, determine their threshold voltages and sketch their transfer characteristics. The output level of the comparator is ±10 V. For Fig. 13.60, you may assume $\alpha = 0.3, 0.5, \text{ and } 0.8$.

10. In the circuit of Fig. 13.61, let $R_1 = 220$ kΩ, $C_1 = 2.2$ nF, $R_a = 10$ kΩ, $R_b = 20$ kΩ, and the circuit be supplied with ±15 V supplies. For this circuit determine $f_{osc}$.
11. An alternative method of duty cycle control for the free-running multivibrator is shown in Fig. 13.62. Determine an expression for $f_{osc}$ and the duty cycle, $D$, expressed as $D = \frac{T_1}{T_1+T_2} \times 100\%$ in terms of $v_{ctrl}$.

12. Design a square-wave/sawtooth oscillator that oscillates at a frequency of 1 kHz.

13. Design a triangular wave generator to generate a positive-going sawtooth wave of 8 V pk–pk amplitude with a frequency of 500 Hz with a ±15 V supply.

14. Describe the operation of a square/triangular voltage-controlled oscillator and derive an expression for the frequency of operation.

15. The variable frequency oscillator of Fig. 13.63 is set up using a TL082 op-amp and two multipliers (AD534) whose $K_1 = K_2 = 0.2$. You may assume that $C_1 = C_2 = 0.003 \mu F$ and $R_2 = 2.5 \, k$. Determine the frequency of oscillation if $V_c$ is varied from 1 to 0.4 V.

16. A monostable multivibrator is constructed using the circuit of Fig. 13.64. The values chosen were $R_1 = 2 \, k$, $R_2 = 3 \, k$, $R = 1 \, k$, $C = 0.3 \, \mu F$, and $V_{CC} = 15 \, V$. Determine the period of this multivibrator if the voltage of each Zener diode is $V_Z = 8.2 \, V$.

17. Show how a JFET can be used to improve the operation of the monostable multivibrator in Fig. 13.64.

18. Describe the operation of the 555 timer and its use as an astable multivibrator. Hence design an astable multivibrator using the 555 to oscillate at 10 kHz. Show how a diode can be used to achieve 50% duty cycle.

19. An astable 555 oscillator is constructed using $R_a = 5 \, k$, $R_b = 5 \, k$ and capacitor $C = 0.01 \, \mu F$. Calculate the output frequency of the
20. Discuss the use of the 555 timer as a monostable multivibrator.

21. A monostable 555 timer is required to produce a specified time delay in a circuit. If a 3.3 \( \mu \)F timing capacitor is used, calculate the value of the resistor required to produce a minimum output time delay of 120 ms.

22. Explain the operation of the half-wave rectifier shown in Fig. 13.65, and determine the polarity of the output signal.

23. For the precision full-wave rectifier shown in Fig. 13.66, describe the operation of the system and determine the polarity of the output signal.

24. Using the circuit in Fig. 13.66, design a precision full-wave rectifier to operate at 10 kHz and below.

25. Using the circuit in Fig. 13.67, design a high input impedance precision full-wave rectifier.

26. Using the circuit in Fig. 13.68, design a precision full-wave rectifier.

![Circuit for Question 7](image)
Fig. 13.59  Circuit for Question 7

Fig. 13.60  Circuits for Question 9
Fig. 13.61  Circuit for Question 10

Fig. 13.62  Circuit for Question 11
**Fig. 13.63** Circuit for Question 15

![Circuit Diagram for Question 15](image1)

**Fig. 13.64** Circuit for Question 16

![Circuit Diagram for Question 16](image2)

**Fig. 13.65** Circuit for Question 22

![Circuit Diagram for Question 22](image3)
Fig. 13.66  Circuit for Question 23

Fig. 13.67  Circuit for Question 25

Fig. 13.68  Circuit for Question 26
14. Special Devices

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In previous chapters, we discussed several semiconductor devices including the diode, the BJT, the FET, the operational amplifier, and the current feedback amplifier. There are several other devices that are available to the designer, and we will discuss some of these in this chapter. At the end of the chapter, the student will be able to:

- Demonstrate knowledge of a variety of special devices
- Use these devices in a range of circuits

14.1 Light-Dependent Resistor

A light-dependent resistor (LDR) or photoresistor is a resistor that is sensitive to light. Specifically, the device lowers its resistance significantly in response to exposure to light. It is sometimes referred to as a photoconductor, cadmium sulphide cell or photocell. It is made up of a semiconductor of high resistance. Energy absorption from incident light stimulates bound electrons into the conduction band such that the resulting electron-hole pairs increase the conductivity of the material and consequently lower the resistance. They are used in many applications including camera light meters, streetlights, clock radios, security alarms, and outdoor clocks. An example of an LDR is the
ORP12. This device has a dark resistance of about 1 M which falls to about 5 k in bright light. The symbol for the LDR is shown in Fig. 14.1.

One specification of the device is the sensitivity which is the resistance at a specified illumination level. A typical curve containing this information is shown in Fig. 14.2, where resistance is plotted against light intensity expressed in lux. For applications involving ON–OFF responses such as fire detectors, cells with steep slopes are suitable since then a small change in illumination results in a large change in resistance.
For applications involving signals of varying levels such as exposure control for cameras, cells with low slopes are more appropriate. Another specification is the dark resistance — the resistance of the cell under zero illumination. This establishes the maximum current that can be expected for a given voltage applied to the cell. This parameter is typically in the range 500 k–20 M. The power rating of the cell in Watts is yet another specification, and maximum cell voltage lies between 100 and 300 V. This voltage must never be exceeded.

Typical applications of the photoconductive cell are shown in Fig. 14.3. The circuit in Fig. 14.3a produces an increasing output voltage level for increasing light intensity levels and is suitable for ambient light measurement systems used in camera exposure meters and brightness control circuits. The circuit in Fig. 14.3b is a DC relay system that can be utilized in a range of applications including smoke detectors and night lights. The light above a certain intensity causes the resistance of the LDR to fall sufficiently such that the voltage across the base–emitter junction of the transistor falls below 0.7 V thereby turning OFF the transistor. If the light falls below this intensity, the resistance of the LDR increases thereby turning ON the transistor and activating the relay that can be used to switch ON the desired system.
Example 14.1  Design a system using a photocell and an op-amp as a comparator to switch ON light when ambient light falls below a certain level.

Solution  One approach using a photocell is shown in Fig. 14.4. The potentiometer $VR_1 = 20 \, k\Omega$ in conjunction with the light-dependent resistor sets a potential at the noninverting input of an op-amp. The op-amp is powered from the single-ended $+15 \, V$ supply. A reference potential $V_{REF} = 7.5 \, V$ is set by $R_1 = 10 \, k\Omega$ and $R_2 = 10 \, k\Omega$ at the inverting input. When the light is sufficiently bright, the resistance of the LDR is low, and the voltage $V_X$ is less than the reference potential $V_{REF}$. 
The output of the op-amp saturates negatively, and the diode $D_1$ is reverse-biased, thereby ensuring that the relay remains inactive. When the light intensity falls, the resistance of the LDR increases such that $V_X > V_{REF}$. The output of the op-amp then saturates positively switching ON the diode and activating the relay, thereby turning ON the light. The light level at which the system switches may be set by adjusting the potentiometer.

**Example 14.2**  Design a system using a photocell and a transistor to switch ON a light-emitting diode (LED) when ambient light falls below a certain level. Indicate the changes needed for the system to indicate the presence rather than the absence of light.

**Solution**  The basic system is shown in Fig. 14.5 and follows the approach of Fig. 14.3b. The LDR is placed between the base terminal and ground, and a potentiometer $VR_1 = 50 \, k$ is connected between the base and the supply voltage. This is used to set the reduced light level at which the system is activated and its value is not critical since from Fig. 14.2, the resistance change of the LDR in response to varying light intensity is between about $1 \, k$ and $1 \, M$. Resistor $R_1 = 1 \, k$ limits the current through the led when the transistor turns ON to less than $9 \, V/1 \, k = 9 \, mA$. Of course, other supply voltage levels can be used. For
the system to indicate the presence instead of the absence of light, the positions of the LDR and potentiometer must be interchanged such that the system will turn ON the LED when sufficient light falls on the LDR instead of when there is reduced light.

**Fig. 14.5** Circuit for Example 14.2

### 14.2 Photodiode

The cadmium sulphide light-dependent resistor discussed above is sensitive to light but responds slowly to changes in light intensity. It is, therefore, suitable for slow-acting light-intensity-sensing applications only. For use as optical sensors in medium- to high-speed applications, the photodiode and the phototransistor are more suitable.

A photodiode is a diode that generates a current or a voltage when exposed to light. Its symbol is shown in Fig. 14.6. It operates as a reverse-biased pn junction and therefore experiences a reverse current arising from thermally generated carriers. As the reverse-biased voltage is increased, this current increases to its saturation value when
the current flow equals the rate of thermal generation of the carriers. When such a junction is exposed to increased illumination, additional electron–hole pairs are generated which result in an increased reverse saturation current. This current is approximately proportional to the intensity of the light. The current vs voltage characteristic of the photodiode in the dark state is essentially that of a conventional diode, as shown in curve 1 of Fig. 14.7. Upon illumination, however, the characteristic shifts downward to curve 2 and then to curve 3 as light intensity increases. These curves do not pass through the origin since the reverse saturation current arising from exposure to incident light continues to flow for zero reverse-biased. In curves 2 and 3 for short-circuited diode terminals, a photo current $I_{SC}$ that is proportional to the light intensity flows through the diode while for open-circuited terminals, a voltage $V_{OC}$ appears across the diode terminals. $I_{SC}$ and $V_{OC}$ are shown in Fig. 14.7.

![Fig. 14.6 Symbol of photodiode](image-url)
As is evident from the curves, the reverse current increases as the incident luminous flux increases. For a constant level of illumination, the reverse current increases only slightly with increasing reverse-biased indicating that the reverse current is largely independent of the reverse-biased voltage. It can also be seen from the curve that reverse current flows even as the reverse-biased is reduced to zero and then to a small forward-biased up to about 0.3 V. Forward-biased above this value causes the reverse current to fall, and it goes to zero when the forward-biased is approximately 0.5 V. “Dark current” is the reverse saturation current of the device in the absence of incident light.

The short-circuit current has a very linear relationship with incident light intensity. A typical reverse (short-circuit) current vs illumination characteristic for this device is shown in Fig. 14.8. Here luminous flux is the total amount of light emitted or received by a surface, and its unit of measurement is the lumen (lm) where 1 lm = 1.46 mW. The luminous flux incident on a surface is measured in
lux (lx) or in mW/m², where 1 lx = 1 mW/m². The specifications of a photodiode include the following:

- Responsivity in $A/W$ is the ratio of generated photo current to incident light power.
- Sensitivity is the reverse current in amperes resulting from unit incident luminous flux. It is generally quoted for a reverse-biased that is less than the maximum allowable value. A typical sensitivity specification is 100 nA/lx at reverse-biased of 12 V with a maximum reverse-biased of 15 V.
- The maximum reverse-biased voltage and current, e.g., 22 V and 18 mA.
- Maximum forward current, typically 8 mA.

![Graph](image)

**Fig. 14.8** Typical reverse current vs illuminance for photodiode

The spectral response relating sensitivity or responsivity to the wavelength of incident light is shown in Fig. 14.9.
Photodiodes provide excellent linearity with respect to incident light, low noise, and wide spectral response. Additionally, the device is mechanically rugged, compact, and lightweight, and has a long life. They are used in consumer electronic devices such as smoke detectors and the receivers in remote controllers for electronic and other home appliances.

Photodiodes can be operated in either the zero-biased or reverse-biased state. A typical application in the zero-biased state is shown in Fig. 14.10. The circuit is a light meter using an op-amp in the transimpedance mode. As light falls on the photodiode, the current is generated. This current flows into the inverting input of the op-amp thereby producing a voltage at the output of the op-amp that is proportional to the light intensity. The various values of resistors allow a nominal output voltage of 100 mV for different light intensity. Thus, the ranges correspond to 1, 10, 100, 1000, and 10,000 lx for the highest range. The higher resistance values correspond to lower lux ranges.
which enable detection of reduced light intensity. In actual use, \( VR_1 = 2 \, k \) is adjusted to give full-scale deflection for \( V_o = 100 \, mV \) on a 100 \( \mu \text{A} \) microammeter.

**Fig. 14.10** Light meter using photodiode

A light meter can be constructed using the photodiode in the reverse mode. Such a system is shown in Fig. 14.11. Here the photodiode is connected in series with a resistor \( R_1 = 10 \, k \) and a reverse bias applied to the system using a 5 V supply. When light falls on the photodiode, reverse current flows through the resistor thereby developing a voltage across the resistor. The specifications for the BPW34 photodiode indicate that the output voltage \( V_o \) across the resistor is related to the lux of the light falling on the photodiode by:

\[
\text{lux} = 1333 \, V_o
\]  

(14.1)
Thus, a light intensity of 1000 lx corresponds to an output voltage of $V_o = \frac{1000}{1333}$ V. If this voltage is scaled up by a factor 1.333, then $V_o = \frac{1000}{1333} \times 1.333 = 1$ V. Therefore, a 1 V output now corresponds to 1000 lx. This amplification factor is provided by the noninverting amplifier which has a gain of 1.33. The output drives a 1 mA milliammeter through a potentiometer $VR_1 = 2$ k which is adjusted such that 1 V out results in full-scale deflection of the milliammeter.

**Example 14.3** Design a light-activated relay system using the photodiode that switches ON a light when the ambient light level is low and switches OFF the light when ambient light rises above a certain level.

**Solution** One solution is shown in Fig. 14.12, where the photodiode is used in the reverse-biased mode. When light falls on the diode, a reverse current flows through the diode causing a voltage drop across the resistor $VR_1 = 10$ k. This lowers the base voltage of the transistor causing it to switch OFF, deactivating the relay. When the light level falls, current flow through the diode drops and the voltage across the base–emitter junction of the transistor increases thereby turning ON
the transistor and activating the relay. This switches ON the light. The potentiometer $VR_1 = 10 \, k$ adjusts the sensitivity of the system to the light level at which switching occurs.

**Fig. 14.12** Circuit for Example 14.3

**Example 14.4** Design the system in Example 14.3 using an op-amp driving a LED.

**Solution** One solution is shown in Fig. 14.13. Here the photodiode $D_1$ is again operated in the reverse-biased mode. The diode and resistor $R_1 = 1 \, M$ sets a voltage $V_x$ at the inverting input of the op-amp, while the wiper of potentiometer $VR_1 = 100 \, k$ sets a variable reference voltage $V_{REF}$ at the noninverting terminal. When light falls on the diode, current flow through the diode increases, and the voltage $V_x$ falls below $V_{REF}$. This causes the op-amp output voltage to go high, turning OFF the LED. When the light level falls, the diode current falls and $V_x$ exceeds $V_{REF}$. The op-amp, therefore, goes low, turning ON the LED $D_2$. The potentiometer $VR_1 = 100 \, k$ adjusts the light level at which switching occurs. In order to limit the current in the LED to about $10 \, mA$, set $R_2 = 1 \, k$. 
The phototransistor, the symbol for which is shown in Fig. 14.14, is a transistor that is sensitive to light. It is essentially a transistor which includes a transparent window that allows light to fall on the collector-base junction. The collector-base junction of the device is photosensitive, and therefore exposure to light generates electron-hole pairs resulting in a small base current.

The phototransistor may have an external base lead that is usually left unconnected. Even though the base is open, the light-induced base current results in a collector leakage current \( I_{CEO} = \beta I_{CBO} \). Thus, light exposure causes a proportional flow of collector leakage current. The response to light intensity changes is much faster than the light-

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**Fig. 14.13** Circuit for Example 14.4

**Fig. 14.14** Phototransistor
dependent resistor. Typical output characteristics are shown in Fig. 14.15. Here the varying parameter producing the different curves is light flux density. These characteristics are very similar to those of the normal bipolar junction transistor with light flux density instead of base current being the changing parameter. A small collector current flows even in the absence of light and is referred to as a dark current. Its value is of the order of 100 nA and is temperature dependent. Phototransistors respond only to the light of specific frequencies. The spectral response factor is normalized at the frequency of maximum response, and the device sensitivity is also stated at this frequency. It should be noted that while the current through the photodiode is linear over about eight decades of light intensity, the collector current of the phototransistor is linear over only about four decades of illumination. It follows therefore that the photodiode is preferred in linear applications while the phototransistor does especially well in switching applications.

![Phototransistor output characteristics](image)

*Fig. 14.15* Phototransistor output characteristics
The phototransistor can be applied in a wide variety of circuits including those associated with the normal transistor. Two basic applications are shown in Fig. 14.16. In the first (Fig. 14.16a), the phototransistor is connected as a common emitter amplifier with a resistor connecting the transistor collector to the power supply. The circuit produces an output at the collector that transitions continuously from a high state to a low state when light in the near-infrared frequency falls on the phototransistor. A Schmitt trigger such as the 74LS14 can be added at the output to eliminate multiple switching for changing light levels that are close to the detection threshold. In the second circuit shown in Fig. 14.16b, the phototransistor is connected in the emitter follower configuration with a resistor connecting the emitter to the ground.

![Diagram](image)

*Fig. 14.16 (a, b) Two applications of a phototransistor*

The circuit in Fig. 14.17 is another simple application. Here light falling on the phototransistor causes it to conduct. The current flow through the resistor results in a low voltage at the collector of the phototransistor, and hence $Tr_2$ is turned OFF. As darkness falls and
there is reduced light on the phototransistor, the reduced current causes the collector voltage to rise thereby turning ON $Tr_2$ and lighting the LED.

![Simple phototransistor application](image)

**Fig. 14.17** Simple phototransistor application

The phototransistor like the photodiode can also be used in a transimpedance amplifier. The basic circuit is shown in Fig. 14.18. It is very similar to the photodiode application except that the phototransistor requires a negative-biased voltage $-V_R$, as shown. The circuit output is given by $V_O = I_CR_F$ and is a linear function of the light intensity falling on the phototransistor.

![Phototransistor transimpedance amplifier](image)

**Fig. 14.18** Phototransistor transimpedance amplifier
Similar to the phototransistor, there is the photofet which is a light-sensitive JFET. An example of this is the LS627 from Linear Systems. This device, like the phototransistor, can also be used in a variety of applications involving light activation.

**Example 14.5** Use the photodiode and the phototransistor to design a system that provides an entry alarm at a doorway.

**Solution** The system shown in Fig. 14.19 comprises three infrared LEDs $D_1$ positioned on one side of a doorway and an opto-transistor receiver $Tr_1$ positioned on the other side. Resistor $R_1 = 220 \, \Omega$ sets the current through these LEDs. Both are positioned such that radiation from the LEDs falls on the phototransistor thereby activating it. The current flow turns ON the green LED $D_2$ in the emitter circuit of the phototransistor. This pulls the base of $Tr_2$ low, and this transistor turns OFF the red LED $D_3$ in its emitter circuit. The potentiometer $VR_1 = 2 \, k$ is adjusted to ensure that $Tr_2$ is OFF under normal conditions. If the infrared radiation is interrupted by entry through the doorway, then the opto-transistor turns OFF causing the green LED to go OFF. The base of $Tr_2$ goes high causing $Tr_2$ to turn ON and switching ON the red LED. Resistor $R_2 = 1 \, k$ limits the current in the red LED. A buzzer may be included between the emitter and ground of $Tr_2$ to provide an audible alarm.
There is also the photodarlington which is a Darlington pair that is photosensitive. In such a device, the first transistor is photosensitive, and its emitter is connected to the base of the second transistor. The resulting gain is, therefore, higher than the normal phototransistor, but the response of the photodarlington is slower.

**14.4 Opto-isolator**

The opto-isolator or opto-coupler is an integrated circuit that incorporates a light-emitting diode along with a light-sensitive receiver, such as a photoresistor, a photodiode, a phototransistor, or a phototriac in the same package. They are used to isolate one part of a circuit from another. This may be to separate low-level signals from signals that may be potentially hazardous, or it may simply be to isolate circuits that have different grounds. When current flows through the LED, light emitted by the LED activates the photosensitive device and results in a changed current flow through the device.

**14.4.1 Photoresistor Opto-isolator**

This opto-isolator comprises an LED and a light-dependent resistor at the output, as shown in Fig. 14.20. This device provides low noise and a
continuously variable resistance that varies from 15 Ω to 50 MΩ in response to a current input. Its characteristics are typically an isolation voltage of 2500 V<sub>rms</sub>, an input current of 10 mA, and an output voltage of 30 V. Applications of this device include audio limiting and compression, automatic gain control, circuit isolation and logic interfacing, silicon-controlled rectifier (SCR) and TRIAC drivers, and noiseless switching.

Fig. 14.20 Opto-isolator using light-dependent resistor

One example, shown in Fig. 14.21, is a remote gain control system. Here the light-dependent resistor is used as the feedback resistor in an inverting amplifier. This enables the remote control of the gain of the circuit using the associated light-emitting diode. The light-dependent resistor is activated by light from the LED, and then the reduced resistance of the light-dependent resistor causes the magnitude of the output voltage of the amplifier to be reduced. Another application example is the switching circuit of Fig. 14.22. In this circuit, the light-dependent resistor is included in a potential divider arrangement with another resistor $R$ that is connected to a 5V supply. When a logic signal is applied to the LED, light from the LED falls on the LDR, and then the resistance of the LDR falls, hence so does the voltage at the junction of these two resistors. This voltage change causes the logic gate to change state.
Exercise 14.1  Explore the use of the photoresistor opto-coupler in the design of (i) a voltage-controlled Sallen–Key low-pass filter and (ii) a voltage-controlled Wien bridge oscillator. In both cases, two photoresistor opto-couplers would have to be used to simultaneously vary two resistors in these systems.
14.4.2 Photofet Opto-isolator

Another opto-isolator is one with a photofet at the output, as shown in the circuit of Fig. 14.23. An example of this is the H11F series from Fairchild Semiconductor. Each device contains a gallium–aluminium arsenide infrared-emitting diode coupled to a bidirectional photosensitive FET that responds as a light-dependent resistor. The arrangement functions as an isolated FET with a resistance variation from 100 Ω to 300 MΩ. Its characteristics include a maximum input diode forward current of 60 mA, isolation resistance of greater than 100 GΩ, continuous detector current of ±100 mA, and a breakdown voltage of 30 V.

The circuit element can function as a variable resistor as it has an extremely linear relationship between diode current and circuit resistance. It can also be used as an electronic switch. The bidirectional photofet and the optical isolation provided by the photodiode make this circuit element a very versatile solid-state relay. Two applications are shown in Fig. 14.24. They are both variable attenuators that allow complete isolation of the control signal.
14.4.3 Photodiode Opto-isolator

The photodiode opto-isolator, shown in Fig. 14.25, utilizes an LED as a light source in the same package as a photodiode as light sensor. When the photodiode is in the reverse-biased mode, current flow through the LED causes light to be emitted from the LED, and this increases the reverse current flow through the photodiode. This is the photoconductive mode. This current flow through a resistor is easily detected as a voltage. This opto-coupler responds very quickly to changes in the LED current and is useful where opto-coupling with high speed is required.

Example 14.6  Outline a system in which the photodiode opto-coupler is used in a linear opto-isolator system.

Solution  One IC that is designed for linear signal isolation is the IL300 linear opto-coupler from Vishay. It comprises an infrared (IR)
LED $D_3$ irradiating two photodiodes $D_1$ and $D_2$ in one package. Photodiode $D_1$ is used to generate a feedback control signal that is used to establish the IR LED drive current necessary to produce a linear signal output from photodiode $D_2$. A simple implementation is shown in Fig. 14.26. Here op-amp A is connected in a noninverting configuration and its output drives the IR LED $D_3$. Resistor $R_3$ assists in limiting the value of this current. The cathode of photodiode $D_1$ is connected to a reverse-biased supply $V_{CC1}$, and the anode is connected to feedback resistor $R_1$. Thus, an input voltage signal $V_i$ applied at the noninverting input of op-amp A drives the IR LED such that a reverse current flows through diode $D_1$ that develops a voltage across $R_1$ which, because of the feedback, is equal to $V_i$. Diode $D_2$ is similarly connected to a separate supply $V_{CC2} = V_{CC1}$ with the output connected to resistor $R_2 = R_1$ which is itself connected to a voltage follower op-amp B. The currents in diodes $D_1$ and $D_2$ are equal, and therefore the voltage developed across $R_2$ is equal to $V_i$ resulting in the voltage $V_o = V_i$.

![Circuit for Example 14.6](image)

**Fig. 14.26** Circuit for Example 14.6

### 14.4.4 Phototransistor Opto-isolator

The opto-isolator using a photo transistor is shown in Fig. 14.27. The light from the LED activates the phototransistor and causes it to conduct. An example of such a device is the 4N25 from Vishay.
Semiconductors. Opto-isolators using a photodarlington are also available. The 4N32 is an example. Such circuits are ideal for interfacing one family of logic circuits to another or for isolating an analog or digital system from the physical world. The current to the LED must as usual be limited by an external resistor in series with the LED. The LED can be driven from an AC source providing a diode is connected in series with the LED. Such a diode will protect the LED from reverse DC voltages. The current through the phototransistor can be converted to a voltage by connecting a resistor to either the collector or the emitter, as shown in Fig. 14.16.

![Phototransistor opto-isolator](image)

**Fig. 14.27** Phototransistor opto-isolator

A typical application is shown in Fig. 14.28. Here, the digital output of a microcontroller is coupled to the base of a transistor that drives the opto-coupler LED. When the transistor is switched ON by the microcontroller, the LED radiates and the opto-transistor is activated. This causes the output of the opto-transistor to go low, and this signal level is coupled to a separate circuit that can be completely electrically isolated from the microcontroller.
Example 14.7  Use the phototransistor opto-coupler to interface two analog audio systems.

Solution  One approach to isolating two audio systems is shown in Fig. 14.29. Here a quiescent current is established through the LED of the opto-transistor, and this current is modulated by a signal from the associated op-amp. The op-amp is operated from a single-ended 24 V supply with $R_1 = R_2 = 100$ k setting the voltage at the noninverting terminal at 12 V. The op-amp itself is connected in the voltage-follower mode with the LED of the opto-coupler inside the feedback loop. As a result, the voltage across resistor $R_3 = 5.6$ k follows the input voltage at the noninverting terminal. The quiescent current through the LED is given by $12\,\text{V}/5.6\,\text{k} = 2.1\,\text{mA}$. This produces a current $I_C$ in the opto-transistor depending on the transfer characteristics of the particular device used but may be about 1 mA. The opto-transistor is here connected in the emitter follower configuration and is powered by a separate supply $V_{CC}$. Potentiometer $VR_1 = 10$ k is adjusted to set the emitter of the opto-transistor to about half the separate power supply voltage in order to allow for maximum symmetrical swing. Coupling
capacitors $C_1$ and $C_2$ are necessary because of the DC at input and output.

**Fig. 14.29** Circuit for Example 14.7

### 14.4.5 Solid-State Relay

The electronic switch or solid-state relay is a generic bilateral device supplied by several manufacturers that switches an electrical signal. It is activated by a control input and is useful in signal gating, modulator, demodulator, and CMOS logic implementation. One device is the HSR312 solid-state relay from Fairchild Semiconductor shown in Fig. 14.30. A current through the diode connected between the terminals marked anode and cathode causes conduction between terminals 6 and 4. The device can be used as a direct replacement for mechanical relays. Solid-state relays are also available in the quad and higher packages as well as in a multiplexer formulation. A simple application involving the switching of AC is shown in Fig. 14.31. Closing switch $SW_1$ drives current through the LED. This closes the solid-state switch and therefore connects the load to the AC supply. Opening the switch results in the opening of the solid-state switch and hence the switching OFF of the supply. The HSR312 provides 4000 V$_{\text{rms}}$ isolation and can operate at 250 V. It can handle up to 190 mA and has an on-resistance of 10 Ω series (when series connected).
14.5 Silicon-Controlled Rectifier

The *silicon-controlled rectifier (SCR)* or thyristor is a three-terminal semiconductor device used in the control of large flows of electrical power. It consists of four layers of semiconductor material alternatively n-type and p-type, as shown in Fig. 14.32a. The outer p-type layer constitutes the anode while the outer n-type layer constitutes the cathode. The inner p-type layer forms a third terminal called the gate which is used to turn ON the device. The symbol is shown in Fig. 14.32b. In order to understand the operation of the thyristor, it is instructive to view the device as a pnp transistor and an npn transistor connected, as shown in Fig. 14.33. Application of a voltage across the device in the forward or reverse direction results in little or no current flow since both transistors are turned OFF until the voltage exceeds the
breakdown or breakover voltage which is of the order of hundreds of volts.

*Fig. 14.32*  Silicon controlled rectifier (a) structure and (b) symbol
In the reverse direction corresponding to the application of a negative voltage to the anode and a positive voltage to the cathode, the base–emitter junctions of $Tr_1$ and $Tr_3$ are reverse-biased as a result of which both transistors are OFF. The thyristor is in the reverse blocking region, and only a small leakage current flows. Apart from an increased leakage current, the device remains nonconducting with an increased reverse voltage until a threshold voltage called the reverse breakover or breakdown value is reached. At or above this voltage, avalanche breakdown occurs in the semiconductor material and significant current flow occurs which, if not limited, could result in the destruction of the thyristor.

In the forward direction corresponding to the application of a positive voltage on the anode and a negative voltage on the cathode, the base–emitter junctions of both transistors become forward-biased, but the collector–base junctions are reverse-biased and the thyristor is OFF. Thus, only a small leakage current flows and the device is in the forward blocking region. There is a gradual increase of this leakage current with increase of the applied forward voltage. However, the device remains effectively OFF until the forward voltage reaches a
threshold value referred to as the forward breakover voltage $V_S$. At or above this value, conduction increases rapidly with a consequent fall in the terminal voltage. The thyristor is now in the forward conduction region with a maximum current of hundreds of amperes. The resulting characteristic is shown in Fig. 14.34.

It is possible to reduce the effective forward breakover voltage by injecting a triggering current at the gate terminal $G$ corresponding to the base terminal of $Tr_2$. The effect of this current is to forward-biased the base–emitter junction of $Tr_2$ thereby producing an amplified current in the collector of $Tr_2$. This current flows out of the base of $Tr_1$ thereby resulting in a further amplified current flowing out of the collector of $Tr_1$. This then enters the gate or base of $Tr_1$ resulting in the regenerative switching ON of both transistors and hence conduction

![SCR Characteristic](image-url)
between the anode and the cathode terminals. This action results in the curves of Fig. 14.35.

From these curves, it can be seen that an increased gate current results in a reduced breakover voltage at which the thyristor switches ON. The gate current pulse must be of sufficient duration such that the thyristor current exceeds a minimum value called the holding current \( I_{th} \). This minimum value is that which enables the device to remain conducting even after the removal of the gate current. Cessation of the gate current before the holding current level is attained will cause the thyristor to turn OFF again. Once the thyristor is turned ON, the current must exceed the holding current in order to sustain the thyristor in the conducting state. In such circumstances, the device remains in the conducting state independently of the gate which no longer exercises
any control. The thyristor current may vary but must not fall below the holding current value. In the ON state, the forward voltage across the thyristor is typically around 1 V.

It is possible to turn ON a thyristor by applying a forward voltage whose rate of change \(dV/dt\) exceeds some critical value specified by the manufacturer. In this turn-on mode, the voltage across the device does not have to exceed the breakover voltage for switch ON to occur. At this critical value of \(dV/dt\), the rapid change of voltage across the SCR results in a flow of current through the internal junction capacitances. In particular, a flow of current to the gate terminal triggers the device. A snubber circuit consisting of a resistor of about 100 Ω in series with a capacitor of about 0.1 μF placed across the anode and cathode of the SCR can be used to protect against rapid increases in terminal voltage.

In order to turn OFF a thyristor, the current through the device must be reduced to a value below the holding current value. This can be accomplished by opening the thyristor circuit or short-circuiting the thyristor. If the thyristor is operated from an AC mains supply, then the voltage across the device periodically goes through zero and hence turns OFF the device. If the operating voltage is DC, then special turn-off arrangements become necessary. An example of an SCR is the 2N5064.

### 14.5.1 Gate Turn-On Methods

The SCR or thyristor can be switched ON in several ways. The method to be used in a particular situation depends on the requirements of the application as well as the triggering specifications of the SCR. It should be noted that excessive gate voltage or current drive may destroy the SCR while inadequate gate-triggering levels may result in less than optimal performance of the system.

#### 14.5.1.1 Static Switching

SCR static switching circuits use either a constant or varying DC signal for SCR turn-on for both DC and AC power control. One simple approach is the use of manual switching and a DC bias supply to turn ON the device, as shown in Fig. 14.36. The closure of normally OFF switch \(SW_1\) delivers a voltage to the gate of the SCR via the resistor \(R_G\) thereby turning it ON. Normally, ON switch \(SW_2\) is used to interrupt the
current to the SCR in order to turn it OFF. The DC-biased voltage may be removed and resistor $R_G$ returned to the supply voltage, as shown in Fig. 14.37. Several switches may be added in parallel with $SW_1$ so that the SCR can be turned ON from many locations. Switch $SW_1$ can be moved to a gate-ground position where it must be normally closed, as shown in Fig. 14.38. When opened, a triggering signal is applied through resistor $R_G$ to the gate of the SCR. Several switches can then be placed in series so that triggering can again take place at several locations.

![Static switching of SCR](image)

*Fig. 14.36* Static switching of SCR
Example 14.8  A thyristor has $I_G = 500 \mu A$, $V_{GC} = 0.7 V$, $V_{AC} = 0.2 V$, and $I_H = 10 \text{ mA}$. Using $V_{TRIG} = 3 V$ and $V_{CC} = 24 V$, determine the resistor $R_G$ in order to trigger the thyristor into conduction and the resulting anode current for a load $R_L = 100 \Omega$ in the circuit of Fig. 14.37.

Solution  From Kirchoff’s voltage law , $V_{TRIG} = I_G R_G + V_{GC}$ from which $R_G = (V_{TRIG} - V_{GC})/I_G = (3 - 0.7)/500 \mu A = 4.6 \text{ k}$. The anode current $I_A$ is found from $V_{CC} = I_A R_L + V_{AC}$. Hence, $I_A = (V_{CC} - V_{AC})/R_L = (24 - 0.2)/100 = 238 \text{ mA}$. 
A simple static switch for AC power control to a load is shown in Fig. 14.39. It is a basic half-wave circuit that is triggered by a signal through resistor $R_1$ to the gate of the SCR when $SW_1$ is closed. The SCR conducts for one half-cycle and turns OFF for the other half as the waveform goes through zero. The load waveform is therefore a half-wave rectified AC, as shown in Fig. 14.40. The reverse voltage rating of the SCR must exceed the peak reverse voltage to which it will be subjected. Diode $D_1$ prevents the gate cathode junction of the SCR from being subjected to reverse voltages. Again, the normally open switch $SW_1$ may be replaced by a normally closed switch between the gate and the cathode.

![Static AC power switch](image)

**Fig. 14.39** Static AC power switch
14.5.1.2 Phase Control Switching

The basic system can be modified to introduce phase control, as shown in Fig. 14.41. Here potentiometer \( VR_1 \) in conjunction with resistors \( R_1 \) and \( R_2 \) allows the adjustment of the triggering voltage to the SCR to switch the SCR at a specified point in the signal cycle. This is shown in Fig. 14.42 where phase adjustment from 0° to 90° can be effected corresponding to SCR conduction for 180° to 90° and the shaded area represents nonconduction. For phase adjustment from 0° to 180°, corresponding to SCR conduction for 180° to 0°, the circuit must be further modified by replacing \( R_2 \) with a capacitor \( C_1 \) and introducing another diode \( D_2 \), as shown in Fig. 14.43. The capacitor introduces a delay in the triggering of the SCR as \( C_1 \) charges via \( VR_1 \) and \( R_1 \) to the triggering voltage level. Since the voltage across the capacitor in a series RC network lags the driving AC voltage by an angle \( \theta \) given by

\[
\theta = \tan^{-1}\left(\frac{R}{X_C}\right)
\]  

(14.2)

where \( \theta \) is the lagging phase angle of the capacitor voltage in degrees, \( X_C \) is the capacitor reactance, and \( R \) is the resistance in series with the capacitor, Eq. (14.2) can be used to approximately determine component values. Diode \( D_2 \) is optional and allows the discharge of the capacitor through \( R_1 \) on the negative half-cycle. The resulting load waveform is shown in Fig. 14.44.
**Fig. 14.41** Phase control switching of SCR

**Fig. 14.42** Waveform resulting from phase control
Example 14.9  For an operating frequency of 60 Hz, find the capacitor value required to achieve a phase lag of 50° with a resistor of 12 k.

Solution  From Eq. (14.2), \( \tan 50° = 12 \times 10^3 \times 2 \times \pi \times 60 \times C \).

Therefore,
\[
C = \frac{\tan 50°}{12 \times 10^3 \times 2 \times \pi \times 60} = 0.26 \ \mu F.
\]
**Example 14.10** Design a static switch to control power to an AC load through the action of an SCR being powered by a 15 VAC supply.

**Solution** The basic system is shown in Fig. 14.39. It comprises an SCR in series with a load with the arrangement being connected to the mains supply. With the switch open, no activating pulse can be applied to the gate, and therefore the SCR remains OFF. If the switch is closed on the positive half-cycle, a current pulse is supplied to the gate through the resistor causing it to turn ON and thereby connect the load to the mains supply. The device will turn OFF during the negative half-cycle of the supply but will turn ON again on the positive half-cycle. The result is that the supply to the load is a half-wave supply. The diode ensures unidirectional gate current flow. The value of the resistor $R_1$ is calculated using the peak supply voltage say 4 V at which turn occurs and the gate current value required to trigger the thyristor. For the 2N3669, the trigger current has a maximum value of 40 mA giving

$$R = \frac{4}{40 \times 10^{-3}} = 100 \ \Omega.$$ 

This value of gate resistor allows for the unknown load resistance which will reduce the gate current below the 40 mA value used in the calculation.

### 14.5.1.3 Full-Wave Control

The circuit in Fig. 14.45 is designed to control AC power to a DC load using an SCR. The load and the SCR are connected after the diode bridge. Therefore, only unidirectional flow occurs through the load and SCR. As the rectified AC voltage rises across the resistor-potentiometer potential divider, the potentiometer is adjusted so that triggering of the SCR occurs at an appropriate point in the AC cycle thereby realizing phase control. The resulting load waveform is shown in Fig. 14.46. The potentiometer enables adjustment of the firing angle from 0° to 90° for each half-cycle. For phase adjustment from 0° to 180° corresponding to SCR conduction for 180° to 0°, the circuit must be modified by replacing $R_2$ with a capacitor $C_1$, as shown in Fig. 14.47. The capacitor introduces delay in the triggering of the SCR as $C_1$ charges via $VR_1$ and $R_1$ to the triggering voltage level. The resulting load waveform is shown in Fig. 14.48.
**Fig. 14.45** Phase control of AC power to a DC load

**Fig. 14.46** Waveform resulting from phase control of AC power to DC load
A simple application of this system is a temperature controller, as shown in Fig. 14.49. The diode bridge arrangement produces unidirectional current flow through the thyristor, while the resistor, capacitor, and thermostat together regulate the gate drive to the device. At low temperatures when the thermostat is open, for each half-cycle of the supply voltage, the capacitor is charged through the resistor to a potential that triggers the SCR, thereby allowing current flow to the heater. As the ambient temperature rises, the thermostat closes at a specific temperature and short circuits the gate–cathode terminals as a
result of which the SCR cannot be triggered. No power is then delivered to the heater and the temperature falls.

![Temperature controller diagram](image)

*Fig. 14.49* Temperature controller

The full-wave circuit in Fig. 14.50 is designed to control AC power to an AC load using an SCR. The load is connected before the diode bridge, whereas the SCR is connected after the bridge. Therefore, only unidirectional flow occurs through the SCR. As the full-wave rectified AC voltage rises across the resistor-potentiometer potential divider, the potentiometer is adjusted so that triggering of the SCR occurs at a specified point in the AC cycle thereby affecting phase control. The effect on the load waveform is shown in Fig. 14.51. Using the potentiometer, the firing angle can be varied from $0^\circ$ to $90^\circ$ for each half-cycle. Again, for phase adjustment from $0^\circ$ to $180^\circ$ corresponding to SCR conduction for $180^\circ$ to $0^\circ$, the circuit must be modified by replacing $R_2$ with a capacitor $C_1$. 
The symbol for the gate turn-off switch is shown in Fig. 14.52. This device is effectively an SCR that can be turned OFF (and ON) at the gate–cathode junction. This feature is very useful in many power-switching applications. This device can both be turned ON and OFF at the gate which results in a simplification of the associated circuitry.
14.5.3 Light-Activated SCR

The *light-activated SCR* is an SCR that conducts when exposed to light. The symbol for this device is shown in Fig. 14.53. These devices usually have the standard gate where they can also be triggered by an electrical pulse. Once turned ON, the LSCR will continue to conduct even though the light source is removed. Maximum sensitivity to light is achieved by having the gate open. However, the sensitivity can be adjusted by connecting a resistor from the gate to the cathode. The *photo-SCR opto-coupler* is a photosensitive SCR in a package with an LED, as shown in Fig. 14.54. The SCR can therefore be triggered into conduction by passing a current through the LED. It can be used to trigger high current SCRs supplying high power loads.

![Fig. 14.52 Gate turn-off switch](image)

![Fig. 14.53 Light-activated SCR](image)

![Fig. 14.54 Photo-SCR opto-coupler](image)

14.6 TRIAC
While a thyristor is a unidirectional device, the TRIAC allows current flow in either direction. It is a semiconductor device that can be viewed as two thyristors in parallel with the anode of one connected to the cathode of the other. The arrangement enables a large bidirectional current flow. It is used in the switching of AC power and for phase control of different loads. Only one gate terminal is utilized, and this is used to turn ON the TRIAC in either direction with a gate pulse of appropriate polarity. The symbol for the TRIAC is shown in Fig. 14.55, and construction of a typical TRIAC is shown in Fig. 14.56. The terminals $T_1$ and $T_2$ are connected to both p-type and n-type material as shown. This enables conventional current flow in either direction, i.e., from $T_1(+)$ to $T_2(–)$ via $p_1, n_3, p_2$, and $n_2$ and from $T_2(+) to T_1(–)$ via $p_2, n_3, p_1$, and $n_1$. The gate terminal $G$ is also connected to both semiconductor types namely $p_1$ and $n_4$, and this enables gate-$T_1$ voltage turn-on to be of either polarity. Like the thyristor, the current through the TRIAC must exceed the latching current before the cessation of the gate current if the device is to stay ON. When turned ON, the device current must not fall below the holding current. The static characteristic of the TRIAC is shown in Fig. 14.57. Again, similar to the thyristor, the forward breakover voltage falls as the gate trigger current is increased. The device operates in either the first quadrant when terminal $T_1$ is positive relative to terminal $T_2$ and in the third quadrant when $T_2$ is positive relative to $T_1$. 

![Triac Symbol](image)

*Fig. 14.55* TRIAC
Fig. 14.56 TRIAC construction
The TRIAC like the SCR will be turned ON if the rate of change of the terminal voltage exceeds a specified value. A snubber circuit can again be used to prevent turn-on by sharp voltage changes.

### 14.6.1 Triggering Methods

Several triggering methods are presented in this section.

#### 14.6.1.1 Static AC Switch

A popular application of the TRIAC is as a static AC switch for AC loads, as shown in Fig. 14.58. Closing the switch SW1 causes the TRIAC to be triggered by the flow of current through the gate. Resistor $R_1$ provides the gate current required to trigger the TRIAC, and its exact value determines where in the signal half-cycle turn-on actually occurs. Let the phase angle at turn-on be $\theta$ and the corresponding peak supply voltage be $V_T$. Then for $\theta = 2^\circ$, since $\sin \theta = V_T / 115 \sqrt{2}$, it follows that

$$V_T = 115 \sqrt{2} \sin 2^\circ = 5.7 \ \text{V}.$$ 

Let the gate current be $I_{GT}$ and the associated gate-to-terminal $T1$ voltage be $V_{GT}$. Therefore,

$$V_T = I_{GT}(R_L + R_1) + V_{GT},$$

where $R_L$ is the resistance of the load. Using $V_{GT} = 1 \ \text{V}, V_T = 5.7 \ \text{V}, I_{GT} = 20 \ \text{mA},$ and $R_L = 115 \ \text{V}/5 \ \text{A} = 23 \ \Omega$, we get

$$R_1 = \frac{5.7-1}{0.02} - 23 = 212 \ \Omega.$$ 

Once the TRIAC is ON, the full supply voltage is available across the load.

![Static AC switch diagram](image-url)
14.6.1.2 Phase Control Switching

The basic principle in TRIAC phase control circuits is to vary the firing angle of the TRIAC relative to the cycle of the supply and as a result, change the effective voltage across the circuit load. The simple resistive gate triggering circuit in Fig. 14.59 allows the variation of the firing angle from almost zero up to a maximum of 90°, as shown in Fig. 14.60. This is accomplished by simply varying the gate resistor value and hence the time in the half-cycle when the TRIAC switches ON. By adding a capacitor as shown in Fig. 14.61, the resulting RC phase-shifting network enables the increase of the firing angle to almost 180°, as shown in Fig. 14.62.

![TRIAC phase control circuit](image)
**Fig. 14.60** Gate firing angle up to 90° each half-cycle

**Fig. 14.61** TRIAC RC phase control circuit
The capacitor introduces delay in the triggering of the TRIAC as $C_1$ charges via $R_1$ and $VR_1$ to the triggering voltage level. Since the voltage across a capacitor in an RC network lags the input AC voltage by an angle $\theta$ given by:

$$\theta = \tan^{-1}\left(\frac{R}{X_C}\right)$$

(14.2)

where $\theta$ is the phase angle of the capacitor voltage in degrees, $X_C$ is the capacitor reactance, and $R$ is the sum of $R_1$ and $VR_1$, Eq. (14.2) can be used to approximately determine component values.

When driving inductive loads, a snubber circuit consisting of a resistor (100 $\Omega$) in series with a capacitor (0.1 $\mu$F) placed across the terminals of the TRIAC may be used to protect against the effects of rapid increases in terminal voltage.

### 14.6.2 Phototriac Opto-isolator
The symbol for a phototriac opto-isolator is shown in Fig. 14.63. This device consists of a LED packaged with a photosensitive TRIAC. The TRIAC can therefore be triggered into conduction by driving current through the LED. This device is particularly suited for triggering higher current TRIACs supplying high-power loads. An example of an application of the MOC 3011 phototriac opto-isolator is shown in Fig. 14.64. In this circuit, the input of the phototriac opto-coupler is driven by the digital output of a microcontroller or personal computer, represented here by a switch in series with a battery. Resistor $R_1$ is chosen to limit the current through the light-emitting diode, while resistor $R_2$ limits the current to the gate of the TRIAC. The output of the MOC 3011 is used to provide gate drive to the high-power TRIAC 2N6071 which is connected to the load and the mains supply. Thus, closing the switch to the input of the MOC 3011 triggers the internal TRIAC which in turn triggers the external 2N6071 TRIAC into conduction. The result is that the load is connected to the mains supply. This arrangement isolates the low-power computer circuit from the high-power load, thereby minimizing the risk of shock.

*Fig. 14.63* Phototriac opto-isolator

*Fig. 14.64* Remote control of AC load
Example 14.11  Design a system to remotely switch on a large (10 A) lighting load using the phototriac and a TRIAC.

Solution  The system is based on Fig. 14.64. The MOC3011 is connected through a resistor $R_2$, which provides the gate current required to trigger the TRIAC. Let the phase angle at turn-on be $\theta$ and the corresponding peak supply voltage be $V_T$. Then for $\theta = 2^\circ$, since 

$$\sin \theta = \frac{V_T}{115 \sqrt{2}}$$

it follows that $V_T = 115 \sqrt{2} \sin 2^\circ = 5.7$ V. Let the gate current be $I_{GT}$ and the associated gate-to-terminal $T_1$ voltage be $V_{GT}$. Therefore, $V_T = I_{GT}(R_L + R_2) + V_{GT}$, where $R_L$ is the resistance of the load. Using $V_{GT} = 1$ V, $V_T = 5.7$ V, $I_{GT} = 20$ mA, and $R_L = 115$ V/10 A = 11.5 $\Omega$, we get 

$$R_2 = \frac{5.7 - 1}{0.02} - 11.5 = 224 \ \Omega$$

Current to activate the diode in the phototriac is supplied via resistor $R_1$ and long low-voltage wiring with a 5 V source and a switch S1. If the required diode current is 15 mA, then resistor $R_1 = 5$ V/15 mA = 333 $\Omega$. Such wiring need not be in a conduit since it is at low voltage and therefore significant cost savings can be realized in installing a lighting system in commercial or residential buildings. Other loads such as motors, fans, or pumps can be switched, but a snubber circuit may be necessary.

14.7 Shockley Diode

The Shockley diode in Fig. 14.65 is essentially an SCR without the gate terminal. Its characteristic therefore corresponds to that of the SCR with zero gate current, as shown in Fig. 14.66. From this characteristic, it can be seen that for a voltage applied across the anode and the cathode, little or no current flows. In the case of a reverse voltage, a value exceeding the reverse breakdown voltage of the device (typically 10–20 V) causes the device to turn ON. It is not intended that the device operates in this mode. When the forward voltage is increased beyond the breakover voltage $V_{BR}$, current flow increases rapidly and the device turns ON when this current exceeds the latching value. The switching current at this point is $I_S$. The terminal voltage drops significantly to a
voltage $V_{MN}$, and conduction continues providing the current exceeds the holding current $I_H$. Once the device begins to conduct, it will continue until the anode current is reduced to a value less than the holding current. This device is generally designed for unidirectional operation and is often used in SCR triggering circuits.

**Fig. 14.65** Shockley diode symbol

![Shockley diode symbol](image)

**Fig. 14.66** Shockley diode characteristic

One simple application is in a relaxation oscillator, as shown in Fig. 14.67a. Closure of the switch results in the charging of the capacitor and increase of the voltage across the capacitor. When the voltage reaches the breakover voltage of the Shockley diode, the diode conducts thereby discharging the capacitor and the capacitor voltage
falls. Once the diode current drops below the holding current of the diode, the diode turns OFF and the capacitor begins to charge again. The capacitor waveform is shown in Fig. 14.67b. The rising waveform can be made linear by using a constant current source to charge the capacitor.

![Shockley diode circuit](image)

**Fig. 14.67** Shockley diode. (a) Relaxation oscillator and (b) output waveform

**Example 14.12** Design a relaxation oscillator to produce a linear waveform with a slope of 10 mV/μs. Use a Shockley diode having $V_{BR} = 12$ V, $V_{MN} = 1$ V, and $I_H = 2$ mA.

**Solution** One circuit for achieving this is shown in Fig. 14.68. Zener diode $D_1$ has $V_Z = 2.7$ V and with $R_2 = 2.2$ k, a current of $(15 - 2.7)/2.2 k = 5.6$ mA flows through the Zener diode. Transistor $Tr_1$ is connected as a constant current source delivering a constant current of $(2.7 - 0.7)/R_1$. For $R_1 = 2$ k the constant current is 1 mA. This constant current charges capacitor $C_1$ for which $I/C_1 = dV/dt$. Now $10$ mV/μs = $10^4$ V/s, and therefore $C_1 = I/dV/dt = 10^{-3} A/10^4 (V/s) = 0.1$ μF. A rail-to-rail op-amp such as the LMC6482 is used in the voltage follower mode to buffer the capacitor voltage and deliver an output voltage. The peak output voltage is $V_{BR} = 12$ V with a minimum value less than $V_{MN} = 1$ V.
14.8 DIAC

The DIAC in Fig. 14.69 is essentially a TRIAC without the gate terminal. Its behavior under an applied voltage, therefore, corresponds to the TRIAC characteristic for zero gate current. Thus, as the terminal voltage of the DIAC is increased, there is initially little or no current flow until the voltage attains the breakover value. At this point, the DIAC conducts heavily and the terminal voltage falls to a lower value. Its characteristic is shown in Fig. 14.70. The DIAC is often used for the reliable triggering of TRIACs. The two-phase control TRIAC circuits in Figs. 14.59 and 14.61 are rarely used in practice. This is because of variations of gate-trigger signal levels between TRIACs of the same type, quadrant of operation, and device case temperature. This variation prevents the reliable calibration of the phase control resistor for specified firing angles.
This basic problem is eliminated by using a DIAC as part of the triggering circuit, as shown in Fig. 14.71. Here the voltage across the capacitor must exceed the breakover voltage $V_{BO}$ of the DIAC. When this occurs, the DIAC turns ON, and the voltage across it falls to a lower voltage $V_D$. This presents a fast-rising trigger signal of amplitude $(V_{BO} - V_D)$ to the gate of the TRIAC which turns ON the TRIAC in a
reliable and predictable manner. This circuit provides excellent speed control for universal motors used in many shop tools and kitchen appliances, fans, sewing machines, and food blenders. It can also serve as a very effective light dimmer controller. An example of a DIAC is the 1N5758 with a 16–24 V breakover voltage.

With the potentiometer, the charging resistance $R$ can be varied from a minimum $R = R_1$ to a maximum $R = VR_1 + R_1$. At low values of charging resistance, the phase angle is small, and the capacitor voltage will be almost in phase with the supply voltage. At higher values of charging resistance, the phase lag increases. However, the amplitude of the voltage $V_C$ across the capacitor decreases relative to the amplitude of the supply voltage $V_S$. From circuit theory, the relationship is given by:

$$V_C = \frac{X_C}{\sqrt{R^2 + X_C^2}} V_S$$  \hspace{1cm} (14.3)

While this was not an issue before because of the lower triggering voltages involved, the introduction of the DIAC means that the capacitor voltage needs to rise to higher values such that the DIAC breakover voltage $V_{BO}$ can be overcome. Therefore, for TRIAC conduction, the charging resistance $R$ must be such that:

$$V_C = V_{BO}$$  \hspace{1cm} (14.4)
This means that this resistance cannot exceed a maximum value lest the TRIAC fail to be triggered.

**Example 14.13** Using the system in Fig. 14.71, design an AC motor speed controller.

**Solution** Let capacitor \( C_1 = 0.1 \, \mu F \) and use \( R_1 = 3.3 \, k \) with potentiometer \( VR_1 = 250 \, k \). Then the minimum value of \( R \) is \( R_{mn} = 3.3 \, k \), while the maximum value is \( R_{mx} = 250 \, k + 3.3 \, k = 253.3 \, k \). Noting that \( X_C = \frac{1}{2 \times \pi \times 60 \times 0.1 \times 10^{-6}} = 26.5 \times 10^3 \, \Omega \), the minimum phase lag is \( \theta = \tan^{-1}(R_{mn}/X_C) = \tan^{-1}(3.3 \times 10^3/26.5 \times 10^3) = 7^\circ \), and the maximum phase lag is \( \theta = \tan^{-1}(R_{mn}/X_C) = \tan^{-1}(253.3 \times 10^3/26.5 \times 10^3) = 84^\circ \).

The minimum value of \( V_C \) occurs when \( R = R_{mx} = 253.3 \, k \) and is given by

\[
V_{Cmn} = \frac{X_C}{\sqrt{R^2 + X_C^2}}V_S = \frac{26.5 \times 10^3}{\sqrt{(253.3)^2 + (26.5)^2}} = 0.1V_S.
\]

The peak value of the supply voltage is \( V_S(p_k) = 115\sqrt{2} = 162.6 \, V \). This gives

\[
V_{Cmn} = 0.1V_S = 16.3 \, V.
\]

Therefore, the DIAC breakover voltage \( V_{BO} \) must be less than 16.3 \, V if TRIAC triggering is to occur for all values of \( VR_1 \). A higher breakover voltage can of course be used, but the TRIAC will remain OFF for high settings of the potentiometer resistance.

Another application is a telephone beacon shown in Fig. 14.72. Here the appearance of ringing voltage on the telephone line causes a current to flow through the diode of the opto device. Diode \( D_1 \) ensures unidirectional current flow through \( D_2 \). This current flow causes the resistance of the LDR to fall thereby resulting in a voltage across the capacitor \( C_1 \). When the breakdown voltage of the DIAC is exceeded, a voltage is applied to the gate of the TRIAC, and conduction through this device results. This process turns ON the TRIAC, and the lamp is turned ON. When the ringing voltage stops and current through the LED ceases, the resistance of the LDR returns to a high value, and the voltage
applied to the DIAC falls. The DIAC turns OFF as a result, and this causes the voltage at the gate of the TRIAC to fall. The TRIAC then turns OFF as the AC passes through zero and thereby switches OFF the lamp.

![Fig. 14.72 Telephone beacon](image)

**Example 14.14** Using the configuration shown in Fig. 14.72, design the system to activate a 100 W lamp when there is ringing on the telephone system.

**Solution** Ringing voltage is typically about 105 V giving a peak voltage of about 150 V. Therefore, diode $D_1$ must have a PIV of at least 200 V, and the 1N4003 is suitable. Using $R_1 = 10 \, k$ allows about 10 mA to flow through the opto-coupler LED. This causes the resistance of the photoresistor to fall allowing $C_1$ to be charged through $R_2$. Let the DIAC breakover voltage be 20 V. Using $R_2 = 10 \, k$ and $C_1 = 0.1 \, \mu F$ ensures that the breakover voltage of the DIAC is reached early in the half-cycle thereby switching ON the TRIAC.

### 14.9 Unijunction Transistor

The unijunction transistor whose symbol is shown in Fig. 14.73 may be considered a special member of the thyristor family. It is made of a silicon lightly doped n-type silicon bar with contacts at either end as the base terminals. Like the JFET, some p-type material is positioned in an area between the base 1 and base 2 terminals, as shown in Fig. 14.74a and the associated terminal is referred to as the emitter. The equivalent circuit of this device is shown in Fig. 14.74b comprising a
variable resistor $R_{B1}$ and a fixed resistor $R_{B2}$ along with a silicon diode that represents the junction between the p-type region and n-type. The sum of these two resistors is known as the interbase resistance $R_{BB}$ given by $R_{BB} = R_{B1} + R_{B2}$.

![Unijunction transistor diagram](image)

**Fig. 14.73** Unijunction transistor

A potential $V_{BB}$ across the two base terminals $B_2, B_1$ with $B_2$ at the higher potential, as shown in Fig. 14.75 (under conditions of zero emitter current), will produce only a small current flow as a result of the light doping of the channel. The effective resistance then is of the order of units of kilo-ohms (4–9 k). An important UJT parameter $\eta$ referred to as the Intrinsic Standoff Ratio is defined as the ratio of the
resistor $R_{B1}$ to the interbase resistance $R_{BB}$ when the emitter current is zero, i.e., $\eta = R_{B1}/R_{BB}$. Its value varies from about 0.5 to 0.8.

![Diagram of UJT operating configuration]

**Fig. 14.75** UJT operating configuration

Now if the emitter is at zero potential, the voltage drop along the channel will result in a voltage $V_{RB1}$ across $R_{B1}$ given by

$$V_{RB1} = \frac{R_{B1}}{R_{BB}} V_{BB} = \eta V_{BB}$$

which is at the cathode of the diode. This voltage $V_{RB1}$ reverse biases the pn junction $D_1$ as occurs in an n-channel JFET, and there is no emitter current flow. As the emitter voltage $V_E$ rises, only a tiny emitter current of a few microamps flows. When it eventually exceeds $V_{RB1}$ by an amount equal to the diode threshold voltage 0.7 V, then the diode becomes forward-biased resulting in an emitter current flow into the base 1 region comprising majority carrier holes into the light-doped n-channel. These positive charge carriers are attracted to the terminal $B_1$, this causing the effective resistance of $R_{B1}$ to fall. This results in an increase in current which causes a further reduction in resistance in a
regenerative action. This action constitutes a negative resistance since a reduction in voltage is associated with an increase in current. The device goes into saturation as the resistance $R_{B1}$ falls to its lowest value of about 50 Ω referred to as saturation resistance. This low resistance results in a reduced voltage drop with a consequent fall in the emitter voltage to a value less than 1 V. This is shown in Fig. 14.76.

![Characteristic of unijunction transistor](image)

Fig. 14.76  Characteristic of unijunction transistor

The UJT is now triggered (sometimes referred to as the ON state), and the maximum current flows through the channel. When the emitter voltage falls to a sufficiently low value, the diode turns OFF and the effective resistance of $R_{B1}$ rises to its former value. While the triggering action of the UJT involves the channel region close to $B_1$ that is represented by resistor $R_{B1}$, the channel region close to $B_2$ that is represented by resistor $R_{B2}$ is largely unaffected by this action and the associated emitter current flow. The emitter voltage that results in the forward-biasing of the pn junction and the flow of an emitter current is usually designated $V_P$ and is given by:
\[ C = \frac{1}{(2\pi f_L R_B)} \] (14.6)

From Fig. 14.76 at the peak point, the peak emitter voltage \( V_p \) is associated with a peak emitter current \( I_p \), while at the valley point, the minimum emitter voltage \( V_v \) is associated with a minimum emitter current \( I_v \).

**Example 14.15**  A UJT with \( \eta = 0.75 \) is powered by a 10V supply. If the emitter is at zero potential, determine the reverse bias across the pn junction.

**Solution**  From Eq. (14.5), \( V_{RB1} = \eta V_{BB} = 0.75 \times 10 = 7.5 \text{ V} \). Hence, the reverse-bias across the pn junction is 7.5 V.

Unijunction transistors are available in power ratings up to about 500 mW with voltage ratings up to about 60 V and peak currents ranging between 50 mA and 2 A. A very common application of this device is in a relaxation oscillator. The basic system using the widely available 2N2646 UJT is shown in Fig. 14.77.

**Fig. 14.77**  Relaxation oscillator using UJT
When the switch is closed, the capacitor charges exponentially through resistor $R_1$ with a time constant $R_1C_1$. As a result, the voltage at the emitter rises. When $V_E = V_P$, the unijunction is triggered and the capacitor discharges through the emitter through $R_{B1}$ and $R_2$ with time constant $(R_{B1} + R_2)C_1$ that is usually much smaller than $R_1C_1$. Therefore, the charge time is usually much larger than the discharge time. When the capacitor voltage falls to $V_E = V_V$, the diode turns OFF, the UJT returns to its original state, capacitor charging again commences, and the cycle is repeated. The waveform at the emitter and at $B_1$ is shown in Fig. 14.78. The former results from the capacitor charge and is an approximate sawtooth wave. The latter signal results from the current flow through resistor $R_2$ during the discharge process and is a short duration pulse.
The peak value of the voltage at the emitter is $V_p$ while the peak value of the voltage at $B_1$ is given by:

$$R_{if} = \frac{V_i}{I_s} = \frac{V_i}{I_i (1 + \beta A_I)} = \frac{R_i}{1 + \beta A_I} \quad (14.7)$$

where $R_{BB(mn)}$ is the minimum value of the ON-state resistance between $B_1$ and $B_2$ given approximately by $R_{BB(mn)} \approx \eta R_{BB}$. The time $t_1$ to charge the capacitor $C$ using $V_{BB}$ through resistor $R_1$ from an initial voltage of $V_V$ to a final voltage of $V_p$ is given by

$$t_1 = R_1 C \ln \left( \frac{V_{BB} - V_V}{V_{BB} - V_p} \right) = R_1 C \ln \left( \frac{V_{BB} - V_{BB}/10}{V_{BB} - \eta V_{BB}} \right) = R_1 C \ln \left( \frac{0.9}{1 - \eta} \right) \quad (14.8)$$

where $V_V \approx V_{BB}/10$ is used. The period is given by $T = t_1 + t_2$ where $t_2$ is the discharge time. Since $t_1 \gg t_2$, the period is approximately equal to $t_1$, and hence:

$$T = R_1 C \ln \left( \frac{0.9}{1 - \eta} \right) \quad (14.9)$$

giving:

$$|A_V|_{dB} = 20 \log \left( \frac{h_{fe} R_L}{h_{ie}} \right) \quad (14.10)$$

**Example 14.16** Using the 2N2926 unijunction transistor, design a relaxation oscillator with a frequency of oscillation of 1 kHz and operating from a 9V supply.

**Solution** The 2N2926 has $\eta = 0.56 - 0.75$, $I_p(mx) = 5 \mu A$ and $I_V(mx) = 4 mA$. Now resistor $R_1$ must allow the emitter current to rise to $I_p$ when the emitter voltage equals $V_p$ and limit the current to less than $I_V$ when the emitter voltage falls to $V_V$. From this, we can find the
maximum value of \( R_1 \) as \( R_{1mx} = (V_{BB} - V_p)/I_p \) and the minimum value of \( R_1 \) as \( R_{1mn} = (V_{BB} - V_V)/I_V \). Using the average value of \( \eta \) which is 
\[ \eta_{avg} = (0.56 + 0.75)/2 = 0.66, \]
the peak voltage \( V_p \) is given by 
\[ V_p = \eta V_{BB} + 0.7 = 0.66 \times 9 + 0.7 = 6.6 \text{ V}. \]
Assuming \( V_V \approx V_{BB}/10 = 0.9 \text{ V}, \) then \( R_{1mx} = (9 - 6.6)/5 \times 10^{-6} = 480 \text{ k} \) and \( R_{1mn} = (9 - 0.9)/4 \text{ mA} = 2 \text{ k}. \)
An intermediate value \( R_1 = 10 \text{ k} \) can be chosen. From (14.10),
\[ f = 1/R_1C \ln \left( \frac{0.9}{1-\eta} \right) = 1/R_1C \ln \left( \frac{0.9}{1-0.66} \right) \approx 1/R_1C. \]
This gives 
\[ C = \frac{1/R_1 f}{1/10 \times 10^3 \times 10^3} = 0.1 \mu\text{F}. \]
A small resistor \( R_2 = 100 \Omega \) enables a pulse voltage out while not affecting \( V_p \). Resistor \( R_3 \) limits the dissipation in the unijunction transistor and can be set to a value \( R_3 = 1 \text{ k}. \)

14.10 Programmable Unijunction Transistor

The programmable unijunction transistor (PUT), shown in Fig. 14.79, has three terminals designated: anode, cathode, and gate. It has a four-layer semiconductor structure similar to the thyristor but with the gate connected to the (n-type) layer close to the (p-type) anode and not to the (p-type) layer close to the (n-type) cathode. Its operational characteristics are similar to those of the UJT except that the intrinsic stand-off ratio \( \eta \) can be externally programmed using a potential divider connected to the gate. This enables the control of the peak value \( V_p \) of the anode voltage. Examples of PUTs are the 2N6027 and 2N6028 from ON semiconductor.
The system operation can be described using Fig. 14.80 where a variable voltage $V_{AK}$ is applied to the anode of the PUT. Here, the potential divider $R_1 - R_2$ holds the gate at a fixed voltage:

$$V_{R1} = \frac{R_1}{R_1 + R_2}V_{BB} = \eta V_{BB}$$  \hspace{1cm} (14.11)

where:

$$\eta = \frac{R_1}{R_1 + R_2}$$  \hspace{1cm} (14.12)

and the cathode is connected through a resistor $R_3$ to the ground. As the supply voltage is increased from zero, only a small reverse leakage current flows through the PUT as the anode-gate junction is reverse-biased and therefore is in a nonconducting state. When the anode voltage $V_A$ exceeds the gate voltage by 0.7 V such that its value equals $V_p$ where:

$$C = 1/ (2\pi f_LR_B)$$  \hspace{1cm} (14.13)

the anode-gate junction becomes forward-biased and an anode current $I_A$ begins to flow. This value of anode voltage is called the peak voltage
$V_p$, as shown on the anode characteristic in Fig. 14.81. The PUT now rapidly turns ON and the anode voltage falls as the current increases down to the valley point. This corresponds to negative resistance over this portion of the characteristic. Similar to the UJT, at the peak point, the peak emitter voltage $V_p$ is associated with a peak emitter current $I_p$, while at the valley point, the minimum emitter voltage $V_v$ is associated with a minimum emitter current $I_v$. External resistors $R_1$ and $R_2$ in the PUT correspond to the internal resistors $R_{B1}$ and $R_{B2}$ in the UJT. By adjusting these resistor values, the PUT can be programmed to have different values of $V_p$ and $I_p$. The output is usually taken at the cathode with the current $I_A$ developing a voltage drop across resistor $R_3$. Thus, when the PUT is OFF, the output voltage $V_o$ is zero. When the device is triggered ON, the rapid rise in current causes a sudden rise in $V_o$ to a value that can be controlled.

![PUT Diagram](image)

*Fig. 14.80* PUT operating configuration
A relaxation oscillator can also be implemented using a PUT such as the 2N6027. The basic system is shown in Fig. 14.82. When power is applied, the capacitor charges exponentially through resistor $R_4$ with a time constant $R_4C$. As a result, the voltage at the anode rises. When $V_A = V_P$, the PUT is triggered and the capacitor discharges through the PUT with time constant $R_3C$ that is usually much smaller than $R_4C$. As a result, the time to charge is usually much larger than the time to discharge. When the capacitor voltage falls to $V_A = V_V$, the PN junction becomes reverse-biased and the PUT turns OFF. It then returns to its original state at which time capacitor charging again commences and the cycle is repeated. The waveforms at the anode and cathode are shown in Fig. 14.83. The former results from the charging and discharging of the capacitor and is an approximate sawtooth wave. The latter signal results from the current flow through resistor $R_3$ during the discharge process and is a short-duration pulse.
Fig. 14.82 PUT relaxation oscillator
The peak value of the voltage at the anode is $V_p$ while the peak value of the voltage at the cathode depends on the discharge current through the PUT. The time $t_1$ to charge the capacitor $C$ using $V_{BB}$ through resistor $R_4$ from an initial voltage of $V_V \approx 0$ to a final voltage of $V_p$ is given by:

$$t_1 = R_4 C \ln \left( \frac{V_{BB} - V_V}{V_{BB} - V_p} \right) = R_4 C \ln \left( \frac{V_{BB}}{V_{BB} - \eta V_{BB}} \right) = R_4 C \ln \left( \frac{1}{1 - \eta} \right) \quad (14.14)$$

The period is given by $T = t_1 + t_2$ where $t_2$ is the discharge time. Since $t_1 \gg t_2$, then the period is approximately equal to $t_1$, and hence:

$$(14.15)$$
\[ T = R_1C \ln \left( \frac{0.9}{1 - \eta} \right) \]

giving:

\[ |A\!V|_{dB} = 20 \log \left( \frac{h_{fe}R_L}{h_{ie}} \right) \]  \hspace{1cm} (14.16)

**Example 14.17** Using the 2N6027 PUT, design a relaxation oscillator with a frequency of oscillation of 1 kHz and operating from a 9V supply.

**Solution** The 2N6027 gives parameters for \( R_G = R_1//R_2 = 10 \, \text{k} \). Therefore, we use \( R_1 = 27 \, \text{k} \) and \( R_2 = 16 \, \text{k} \) which give \( \eta = 27 \, \text{k} / (27 \, \text{k} + 16 \, \text{k}) = 0.63 \). Typical current values are \( I_P = 4 \, \mu A \) and \( I_V = 150 \, \mu A \).

Now resistor \( R_4 \) must allow the anode current to rise to \( I_P \) when the anode voltage equals \( V_P \) and limit the current to less than \( I_P \) when the anode voltage falls to \( V_V \). From this, we can find the maximum value of \( R_4 \) as \( R_{4mx} = (V_{BB} - V_P)/I_P \) and the minimum value of \( R_4 \) as \( R_{4mn} = (V_{BB} - V_V)/I_V \). The peak voltage \( V_P \) is given by

\[ V_P = \eta V_{BB} + 0.7 = 0.63 \times 9 + 0.7 = 6.37 \, \text{V} \]

and therefore we will use \( V_V \approx 0 \). Then \( R_{4mx} = (9 - 6.37)/4 \times 10^{-6} = 658 \, \text{k} \) and \( R_{4mn} = (9 - 0.0)/0.15 \, \text{mA} = 60 \, \text{k} \). Choosing \( R_4 > 60 \, \text{k} \) ensures that the PUT can reset from the valley point following capacitor discharge while choosing \( R_4 < 658 \, \text{k} \) ensures that the capacitor can charge up to the peak point. An intermediate value \( R_4 = 100 \, \text{k} \) can be chosen. From (14.16),

\[ f = 1/R_4C \ln \left( \frac{1}{1-\eta} \right) = 1/R_4C \ln \left( \frac{1}{1-0.63} \right) \approx 1/R_4C \]

This gives

\[ C = 1/R_4f = 1/100 \times 10^3 \times 10^3 = 0.01 \, \mu \text{F} \]

A small resistor \( R_3 = 100 \, \Omega \) enables a pulse voltage out while not affecting \( V_P \).

Finally, the close relationship between the UJT and the PUT is demonstrated in Fig. 14.84 where the UJT symbol and the UJT equivalent circuit are compared with a PUT drawn as a UJT.
14.11 Applications

In this section, applications of the various devices are presented.

14.11.1 Battery Charger

This SCR application is a battery charger, as shown in Fig. 14.85. In this circuit, a low-voltage transformer supplies power through a thyristor, which results in a half-wave rectified voltage being delivered to a battery through $R_5 = 1 \, \Omega$. This resistor serves as a current limiting resistor. The resistor $R_1$ and the diode $D_3$ provide unidirectional gate current drive that turns ON the SCR on the positive half-cycle of the supply voltage. For the 2N3668 SCR, the trigger current has a maximum value of 40 mA giving $R_1 = \frac{15 \sqrt{2} - 6}{40 \times 10^{-3}} = 380 \, \Omega$ where a discharged battery voltage of 6 V is used in the calculation. The battery is charged during this part of the cycle. The transistor $Tr_1$ is used to stop the charging process when the battery is fully charged. It is switched ON when the voltage at its base exceeds the turn-on value. The battery voltage at which this occurs is set by the potential divider comprising
$R_3 = 8.2\ \text{k}$, potentiometer $VR_1 = 1\ \text{k}$ and $R_4 = 1\ \text{k}$ in conjunction with the diode $D_2$. The turn-on voltage is the sum of the transistor base-emitter voltage and the diode voltage giving $1.4\ \text{V}$. The maximum battery voltage $V_B$ at which the transistor turns ON occurs when the potentiometer wiper is at the lower position and is given by
\[
\frac{1.4}{1\ \text{k}} = \frac{V_B}{(1+1+8.2)\ \text{k}}.
\]
This gives $V_B = 14.3\ \text{V}$. Adjusting the potentiometer will give lower battery voltages. Diode $D_1$ allows one-directional current flow through the transistor. Of course, as the battery voltage increases, the available gate current will fall and eventually will be insufficient to turn ON the SCR. Resistor $R_2 = 100\ \Omega$ and diode $D_4$ allow a small trickle charge to the battery after the SCR turns OFF.

![Battery charger](image)

**Fig. 14.85** Battery charger

*Ideas for Exploration:* (i) Introduces a diode bridge such that battery charging occurs on both half-cycles and not just the positive half-cycle.

### 14.11.2 Temperature Controller Using a TRIAC

This application is a temperature controller using a 555 timer and a TRIAC, as shown in Fig. 14.86. The 555 is connected in the monostable mode with the output driving the gate of a TRIAC which controls AC power to a heater. Potentiometer $VR_1$ along with the NTC (negative
temperature coefficient) thermistor $R_2$ and resistor $R_3$ sets a voltage at the trigger input pin 2. In the steady-state with a temperature above a set point such that the resistance of the thermistor results in a potential at pin 2 which is above the threshold voltage of $V_{CC}/3$, the timing capacitor $C_1$ is clamped at ground potential by the internal transistor connected to pin 7, and the output at pin 3 is low thereby ensuring that the TRIAC is OFF. If the temperature falls below the specified value, the resistance of the thermistor increases resulting in the voltage at the trigger input falling below $V_{CC}/3$. This starts the timing cycle and the output goes high, turning ON the TRIAC and power to the heater. If as a result the temperature rises above the set point and the thermistor resistance falls causing the voltage at pin 2 to rise above $V_{CC}/3$ before the end of the timing cycle, then the output goes low at the end of the cycle thereby switching OFF power to the heater as the supply voltage to the TRIAC goes through zero. If, however, at the end of the cycle the temperature has not exceeded the set point, then the voltage at pin 2 will be less than $V_{CC}/3$ and the 555 keeps the TRIAC ON until the set point temperature is exceeded after which turn-off occurs. At the specified temperature, the thermistor must have a resistance $R_2$ such that $VR_1 + R_2 = 2R_3$. This corresponds to a voltage at pin 2 of $V_{CC}/3$.

Using a thermistor with a base resistance of 5 kΩ (at 25 °C) along with $VR_1 = 2$ kΩ and $R_3 = 3.3$ kΩ allows variation of the set point by adjustment of the potentiometer. Decreasing $VR_1$ results in a higher potential at pin 2 and therefore a lower set point temperature. Increasing $VR_1$ toward its maximum value reduces the voltage at pin 2 and hence increases the set point temperature. The cycle time $T$ is set by $R_1$ and $C_1$ based on $T = 1.1R_1C_1$. For $R_1 = 1$ MΩ and $C_1 = 10$ μF, we get $T = 1.1 \times 10^6 \times 10 \times 10^{-6} = 11$ s. Using a 2N6071 TRIAC which has a gate trigger the current requirement of 5 mA and a gate trigger voltage of 1.4 V and noting that the peak output from the 555 is about 7 V when powered by $V_{CC} = 9$ V, then resistor $R_4 = (7 - 1.4)/5$ mA ≈ 1 kΩ.
**Fig. 14.86** Temperature controller using TRIAC

*Ideas for Exploration:* (i) The 9V supply for the circuit was intended to be a 9V battery. Design a suitable 9V regulated supply using a step-down transformer to power this system, the ground for which would be the neutral line of the mains supply; (ii) use an opto-coupler to completely isolate the 555 circuit from the TRIAC.

### 14.11.3 Universal Motor Speed Controller

This application enables the speed of a universal motor such as used in power drills to be varied. The circuit is shown in Fig. 14.87. On positive half-cycles of the mains voltage, a positive voltage is applied across the anode and cathode of the SCR. The potential divider formed by $R_1 = 6.8$ k and $VR_1 = 2$ k along with diode $D_1$ provides a positive gate voltage to turn the SCR on. This occurs when the gate voltage is approximately 0.7 V relative to the cathode and about 10 mA of current flows into the gate. Potentiometer $VR_1$ controls the voltage applied to the gate and therefore the time during the positive half-cycle when the SCR turns ON. The ON time is variable from almost 180° when the wiper of the potentiometer is close to the upper end in the diagram to 90° when the wiper is close to the anode of diode $D_1$ in which case the line voltage has to reach its maximum in order to turn ON the SCR. This mechanism enables control of the power delivered to the motor. Diode $D_2$ provides
protection for the SCR against high reverse voltages. The switch $SW_1$ is used to bypass the SCR so that the full supply voltage is applied to the motor for full-speed operation.

![Universal motor speed controller](image)

**Fig. 14.87** Universal motor speed controller

**Ideas for Exploration**: (i) Examine circuit performance using different SCRs.

### 14.11.4 Sawtooth Generator

An application of the PUT in a sawtooth generator is shown in Fig. 14.88. The circuit is essentially an integrator with the PUT connected across the capacitor. Initially, with an uncharged capacitor $C$ the PUT is OFF. With a negative voltage $V_{REF}$ at the input of the circuit, current flows from the output of the operational amplifier onto the plates of the capacitor charging it with a polarity, as shown. Since one end of the capacitor is at the inverting input of the op-amp (virtual earth), the rising voltage on the capacitor appears at the output of the op-amp. This voltage increases until the capacitor voltage is $0.7$ V above the control voltage $V_C$ at the gate of the PUT at which time the PUT turns ON. As a result, the capacitor is discharged through the PUT and therefore the output voltage falls. The PUT switches OFF when the current through the device falls below the holding current after which the cycle is repeated. The voltage across the terminals of the PUT when
this occurs is about 1 V. Thus, the output voltage varies between 1 V and $V_C + 0.7$. The slope of the rising output voltage is given by
\[
\frac{dV_o}{dt} = \frac{V_{REF}}{RC}
\]
Using $V_{REF} = -1$ V, $R = 100$ k, and $C = 0.01$ μF, the slope is
\[
\frac{dV_o}{dt} = \frac{1}{10^5 \times 0.01 \times 10^{-6}} = 1000 \text{ V/s}.
\]
If the control voltage is $V_C = 10.3$ V, then the peak output voltage is $10.3 + 0.7 = 11$ V.

![PUT-controlled sawtooth generator](image)

**Fig. 14.88** PUT-controlled sawtooth generator

*Ideas for Exploration:* (i) Determine the frequency of the sawtooth waveform; (ii) since the slope of the waveform is a direct function of the reference voltage, introduce a variable reference voltage in order to convert the system into a voltage-controlled oscillator.

### 14.11.5 Flasher Circuit

Another application of the PUT is the flasher circuit shown in Fig. 14.89. Resistors, $R_1 = 18$ k and $R_2 = 10$ k, set a voltage at the gate of the PUT such that the device is OFF when capacitor $C_1$ is discharged. As $C_1$ charges up through resistor $R_3$, the voltage at $B_2$ exceeds the gate voltage by 0.7 V. This triggers the PUT thereby discharging $C_1$ through the LED which turns ON. When the current through the PUT falls below
the holding current, the device switches OFF and the cycle is repeated. For this circuit \( \eta = \frac{R_1}{R_1 + R_2} = \frac{18}{18 + 10} = 0.64 \). Using this, the frequency is given by

\[
 f = \frac{1}{R_3 C_1 \ln \left( \frac{1}{1-\eta} \right)} = \frac{1}{R_3 C_1 \ln \left( \frac{1}{1-0.64} \right)} \approx \frac{1}{R_3 C_1}.
\]

For a flashing frequency of 1 Hz, using \( C_1 = 10 \, \mu F \), then

\[
 R_3 = \frac{1}{f C_1} = \frac{1}{10 \times 10^{-6}} = 100 \, k.
\]

**Fig. 14.89** PUT flasher circuit

*Ideas for Exploration:* (i) Replace the LED by a buzzer such that the system can be used as a metronome.

**14.11.6 Zero Crossing Detector**

This is an application involving opto-couplers in a mains zero-crossing detector, as shown in Fig. 14.90. It consists of two phototransistor opto-couplers (OC1 and OC2) whose signaling LEDs are connected in series with diodes for protection against reverse voltage. The mains voltage is
applied such that each diode pair conducts on alternate half-cycles. The resistor $R_1$ limits the current through the LEDs to about 2 mA. The collectors of the associated phototransistors are connected together and to resistor $R_2$. The other end of this resistor is connected to the power supply. The emitters of the phototransistors are connected to the ground. As a positive-going input voltage goes through zero, the two opto-couplers turn OFF, and the output is high. When the signal goes positive, diodes $D_1$ and $D_2$ turn ON and thereby turn ON the phototransistor in OC1. This causes the output voltage to fall to near zero. During this time, diodes $D_3$ and $D_4$ are OFF. As the signal goes from a positive value through zero, all diodes again switch OFF and the output again goes high. As the signal goes negative, diodes $D_3$ and $D_4$ turn ON thereby turning ON the phototransistor in OC2. The result is the output voltage goes low. The resulting signal at the output is a set of pulses corresponding to the zero-crossings of the input signal. For mains voltage of 120 V, the value of $R_1$ is given by $R_1 = 120V/2mA = 60$ k. A 56 k value can be used. Resistor $R_2 = 4.7$ k sets the current in the phototransistors when switched ON and allows a range of supply voltages from 5 to 15 V.
**Ideas for Exploration:** (i) Implement this system for a low-voltage ac input $V_s$ by adjusting the value of $R_1$ using $R_1 = V_s/2$ mA; (ii) increase the speed of the system by operating the two phototransistors as a cascode amplifier arrangement using a 2N3904 small-signal transistor.

### 14.11.7 Research Project 1

The circuit shown in Fig. 14.91 is a linear opto-coupled DC amplifier using two op-amps and two opto-couplers. The output of the op-amp A drives both LEDs of the two opto-couplers that are in series with potentiometer $VR_1 = 10$ k. Opto-transistor 1 is connected as an emitter follower with its output driving the inverting input of op-amp A, whereas the opto-transistor 2 is connected as an emitter follower with its output driving the noninverting input of op-amp B. The feedback via opto-transistor 1 ensures that the input signal $V_i$ to op-amp A is delivered to resistor $R_1 = 4.7$ k and since opto-transistor 2 receives the same signal as opto-transistor 1, both LEDs being activated by the same...
current, then the signal $V_i$ will appear across $R_2 = R_1 = 4.7 \, k$ and delivered at the output of op-amp B. The potentiometer is used to adjust the effective loop gain around op-amp A. The input signal can vary between zero and about 5 V but cannot go negative as the LEDs can only accommodate unidirectional currents. Both supplies can be $+12 \, V$.

![Linear opto-coupled DC amplifier](image)

**Fig. 14.91** Linear opto-coupled DC amplifier

**Ideas for Exploration:** (i) Implement this system using the LTV826 comprising two opto-transistors in a package; (ii) vary potentiometer $VR_1$ and see how that affects the performance of the system.

### 14.11.8 Research Project 2

The project to be undertaken is the design of a stairstep generator that can be used in the development of a transistor curve tracer for displaying the output characteristics of a transistor on an oscilloscope.
A stairstep waveform is one that increases in discrete steps with time giving an appearance of physical stairsteps. The basic system is shown in Fig. 14.92. Here, a 555 timer is connected as an astable multivibrator. Capacitor $C_1$ is charged via resistor $R_1$ and diode $D_1$ and discharges via resistor $R_2$ and diode $D_2$. By making $R_2$ appropriately larger than $R_1$, the output of the 555 is a set of short-duration pulses. These pulses charge capacitor $C_3$ through $VR_1$ and $R_3$. These pulses cause the voltage across $C_3$ to increase in steps thereby producing a stairstep waveform. This waveform is buffered by the op-amp which is a rail–rail device so that it can be operated from a single-ended supply while transmitting low voltages to its output. When the stairstep voltage across $C_3$ reaches a threshold value, the unijunction $Tr_2$ fires and discharges this capacitor. This discharge produces a voltage pulse across resistor $R_4$ which turns ON transistor $Tr_1$ and resets the 555. The cycle then starts again with pulses from the 555 delivering charge to capacitor $C_3$ and building a stairstep of voltages. Potentiometer $VR_1$ sets the charge current into the capacitor and therefore varies the size of the steps while $VR_2$ sets the voltage across the UJT and therefore sets the number of steps before discharge occurs.

![Stairstep generator](image)

*Fig. 14.92* Stairstep generator
Ideas for Exploration: (i) Use this stairstep generator to develop a transistor curve tracer. See the article “Transistor and FET Curve Tracer” by Daniel Metzger, Electronics World, Vol. 86, No. 2, p. 52, August 1971, where a system that employs a stairstep generator is discussed.

14.11.9 Research Project 3
This research project is based around the design of a low-power inverter for powering low-power lamps and small appliances. The system is shown in Fig. 14.93 and employs two ICs and a 120 V:9 V (18 V center tapped) step-down transformer rated at 2 A. IC1 is a CD4047 CMOS monostable/astable multivibrator connected as an astable multivibrator. Potentiometer $VR_1 + R_1 = R$ and capacitor $C$ set the frequency of oscillation at $f = 1/4.4RC$. Using $C = 0.1 \mu F$ and $R = 100 \ k$ gives $f = 1/4.4 \times 10^5 \times 0.1 \times 10^{-6} = 22.7$ Hz. Possible values are $VR_1 = 100 \ k$ and $R_1 = 10 \ k$ which will allow the adjustment of the frequency to give 50 or 60 Hz. Two outputs from this IC, one inverted relative to the other, are available. IC2 is a ULN2004 that comprises an array of seven high-voltage Darlington pairs. Each pair is rated at 500 mA and is surrounded by protection diodes. In order to increase the current rating, three of the Darlington pairs are connected in parallel and the common collector is connected to one side of the center-tapped secondary of the step-down transformer. Three of the remaining Darlington pairs in the package are similarly paralleled and their common collector connected to the other side of the secondary of the step-down transformer. The center tap of the transformer is connected to a 12 V supply. Resistors $R_4 = R_5 = 33 \ \Omega$ serve to limit the current through the Darlington pairs. The outputs of the CD4047 drive the bases of the parallel-connected Darlington pairs that are switched alternatively ON and OFF. This action produces a stepped-up voltage in the primary of the transformer. Resistors $R_2 = R_3 = 560 \ \Omega$ again perform a current-limiting function. The power rating of this system is limited by the relatively low current rating of the Darlington pairs. An input current $3 \times 500 \ mA = 1.5 \ A$ gives a maximum output current of $1500 mA \times 9/120 = 113 \ mA$ which corresponds to a little over 1 W.
Fig. 14.93  Low-power inverter

Ideas for Exploration: (i) Replace the Darlington array with individual power Darlington transistors in order to increase the power output of the system. The transformer will also have to be upgraded. See the article “250-Watt Power Inverter” by James Melton, Radio Electronics, Vol. 63, No. 10, p. 75, October 1992.

Problems

1. Design a system using a photocell and an op-amp as a comparator to switch ON a motor when ambient light exceeds a certain level.

2. Design a system using a photocell and a transistor to switch ON an alarm when ambient light rises above a specified level. Indicate the changes needed for the system to indicate the absence rather than the presence of light.

3. Design a light meter to cover the ranges 1–10,000 lx using the photodiode in the zero-biased mode shown in Fig. 14.94 and a 1 mA.

4. Explain the operation of the phototransistor and indicate one method by which the light-induced current can be converted to a useable output voltage.

5. Using the photoresistor opto-isolator along with an op-amp, design a remote gain control amplifier system.
6. Outline the approach by which the phototet opto-coupler can be used in the design of (a) a voltage-controlled Sallen–Key low-pass filter and (b) a voltage-controlled Wien bridge oscillator.

7. A microcontroller with a 0–5 V output is used to activate another digital system from which it must be isolated. Use the configuration, shown in Fig. 14.95, to realize such a system with \( V_{CC1} = V_{CC2} = 5 \) V.

8. A thyristor used in a static power switch has \( I_G = 750 \mu A, V_{GC} = 0.7 \) V, \( V_{AC} = 0.4 \) V, and \( I_H = 15 \) mA. Using \( V_{TRIG} = 4 \) V and \( V_{CC} = 36 \) V, it determines the resistor \( R_G \) in order to trigger the thyristor into conduction and the resulting anode current for a load \( R_L = 700 \) Ω in the circuit of Fig. 14.37.

9. For an operating frequency of 300 Hz, find the capacitor value required to achieve a phase lag of 75° with a resistor of 56 k.

10. Describe the operation of a static TRIAC switch for controlling AC power to a load. Show how phase control can be introduced to allow control over the full half-cycle.

11. Design a system to remotely switch ON a large (8 A) heating load using the phototriac and a TRIAC.

12. Using a Shockley diode having \( V_S = 15 \) V, \( V_H = 1.3 \) V, and \( I_H = 5 \) mA, design a relaxation oscillator to produce a linear waveform with a slope of 100 mV/μs.

13. Explain how a DIAC can be used to improve the turn-on performance of a TRIAC-controlled power switch.

14. A UJT with \( \eta = 0.65 \) is powered by a 12 V supply. If the emitter is at zero potential, it determines the reverse-biased across the pn junction.

15. Using the 2N2926 unijunction transistor, design a relaxation oscillator with a frequency of oscillation of 12 kHz and operating...
oscillator with a frequency of oscillation of 12 kHz and operating from a 15 V supply. Provide a buffered voltage output from the system. For this UJT, $\eta = 0.56 \rightarrow 0.75$, $I_p(mx) = 5 \mu A$ and $I_v(mx) = 4 mA$.

16. Determine the oscillating frequency of the relaxation oscillator, shown in Fig. 14.96, where the UJT has $\eta = 0.63$.

17. Explain how the PUT differs from the UJT.

18. Using the 2N6027 PUT, design a relaxation oscillator with a frequency of oscillation of 5 kHz and operating from a 24 V supply. For the 2N6027, $R_G = R_1//R_2 = 10 \, k\Omega$, and typical current values are $I_p = 4 \mu A$ and $I_v = 150 \mu A$.

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**Fig. 14.94** Circuit for Question 3
**Fig. 14.95** Circuit for Question 7

**Fig. 14.96** Circuit for Question 16
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